Reference Design:

HFRD-15.3

Rev. 7; 11/08

REFERENCE DESIGN

High-Frequency SFP Host Board

(Includes Integrated RS-232 to I^2C Conversion)

maxim integrated™

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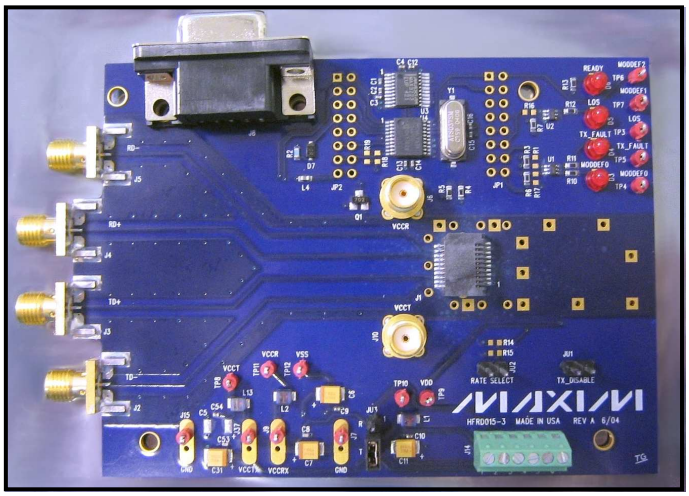
1 Overview

High Frequency Reference Design (HFRD) 15.3 is a Small Form Factor Pluggable (SFP) host board designed on Rogers 4350 material. The host board can be used to test SFP fiber optic / copper transceiver modules in a clean test environment to more accurately define the modules' performance. The host board also includes an RS-232 to I^2C conversion controller to simplify communication and control of the SFP modules from a computer.

HFRD-15.3 provides micro-strip transmission lines and SMA connectors for transmitted and received data. Jumpers and LED's are used for monitoring and changing the low-speed digital I/O. Connections to the module board are made through a 20-pin SFP connector.

HFRD- 15.3



1.1 Features

- SFP MSA Compliant
- Documentation/Test Data
- SMA Connectors for High-Speed data
- Integrated RS-232 to I^2C Converter
- Schematics and Bill of Materials Provided
- Gerber Files Available

2 Obtaining Additional Information

Limited quantities of the SFP transmitter board (HFRD-15.3) are available. For more information about the reference design or to obtain an SFP host board please email to: https://support.maxim-ic.com/ .

3 Reference Design Details

HFRD-15.3 was engineered to test fiber optic / copper transceivers that comply with the Small Form Factor Pluggable (SFP) Multisource Agreement (MSA). The SFP MSA sets guidelines for the package outline, pin function, I/O interface and other aspects of the module design as well as the host board requirements and interface parameters. By complying with the standard, modules are mechanically and functionally interchangeable.

The HFRD-15.3 SFP host board is designed to simulate an ideal environment for SFP module testing using Rogers material and single-ended micro-strip transmission lines. These properties make the host board as transparent as possible, allowing a more accurate assessment of the modules' actual performance. SMA connectors, jumpers and status LEDs are provided to simplify the testing and interfacing of SFP modules.

HFRD-15.3 also integrates an RS-232 to I^2C converter to provide software access and control of the modules memory, diagnostic and status information. Additionally, resistor jumpers can be placed to control / monitor the low speed digital control signals (LOS, TX_DISABLE, etc.) with a computer through the RS-232 serial port and the appropriate software.

The HFRD-15.3 RS-232 to I^2C converter is compatible with software written for the DS3900 (see section 6.2). The HFRD-15.3 reference design can therefore be used with existing software that is often provided by Dallas Semiconductor for their SFP controller ICs. For more information on writing software for use with this reference design, see application note 206: *Using a PC's RS-232 Serial Port To Communicate with 2-Wire Devices*. Note: The microcontroller is pre-programmed with the firmware listed in the application note.

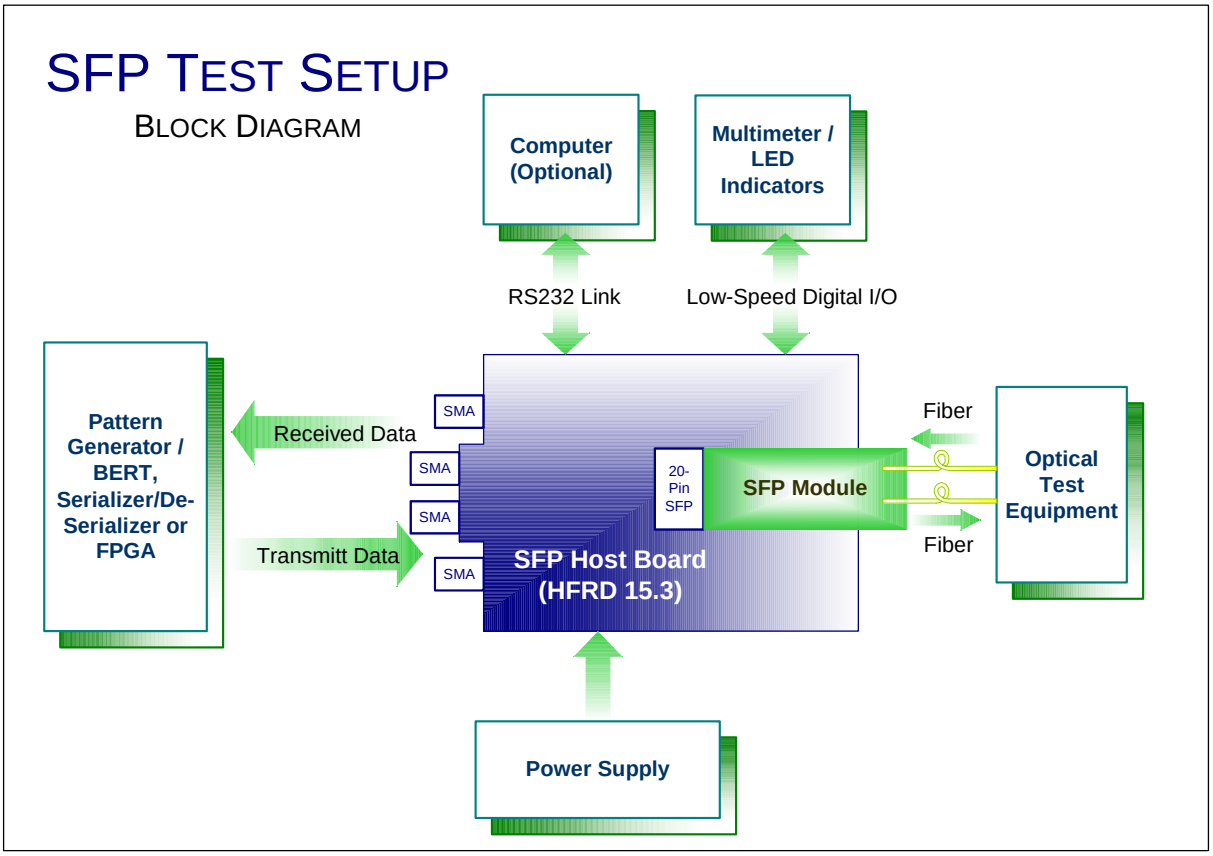


Figure 1. SFP Test Setup (Block Diagram)

4 Typical Reference Design Performance

(Typical values are measured at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	TYP	UNITS
Transmission line Characteristic Impedance	Z	Odd Mode Impedance	50 ±10%	Ω
Differential S11 Magnitude (Notes 1, 2)		f < 2.0GHz	≤ -18	dB
		f < 3.5GHz	≤ -15	
		f < 7.4GHz	≤ -12	
S21 f_{3dB} Point	f_{3dB}	Notes 1, 3	4.7	GHz
S21 f_{6dB} Point	f_{6dB}	Notes 1, 3	8.5	GHz

Note 1: S-Parameter measurements were made using a four-port system.
Note 2: Measured at RD- and RD+ or TD+ and TD-SMA inputs. Measurement includes SFP connector with 50Ω to ground termination on each data line directly after SFP connector (Figure 2).
Note 3: Port 1 is at SFP Host Board connection. Port 2 is at measured at the output of a SFP to SMA converting test board. (Figure 3). The measurement includes bandwidth limitations of the test board that is constructed of approximately 3" of FR-4 material.

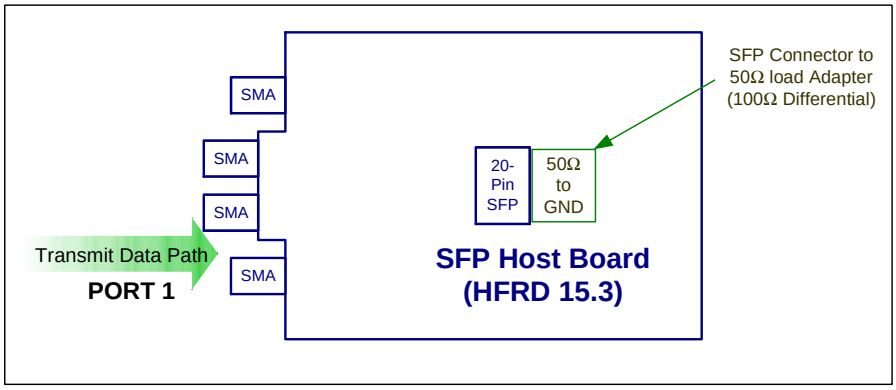


Figure 2. S11 Measurement Setup

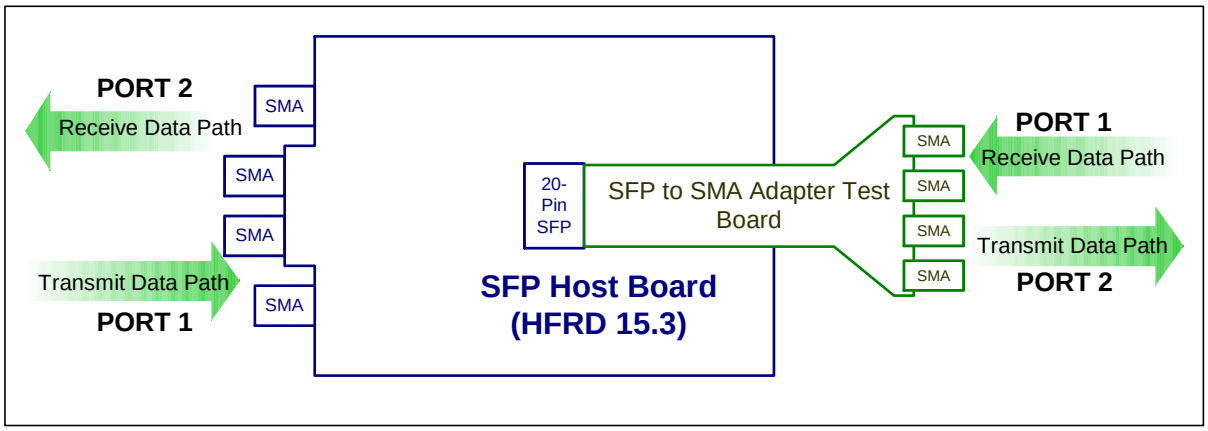


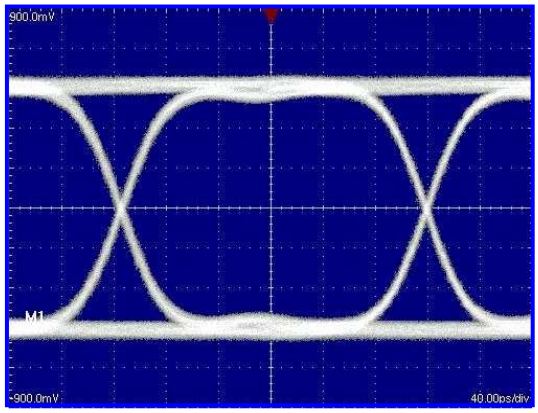
Figure 3. S21 Measurement Setup

5 Reference Design Characteristic Graphs

(Eye diagrams were generated using a pattern generator input signal and an SFP to SMA converter board.)

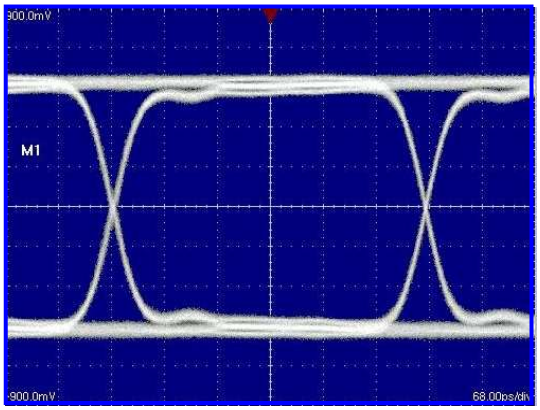
EYE DIAGRAM

(4.25Gbps, Transmit Data Path)



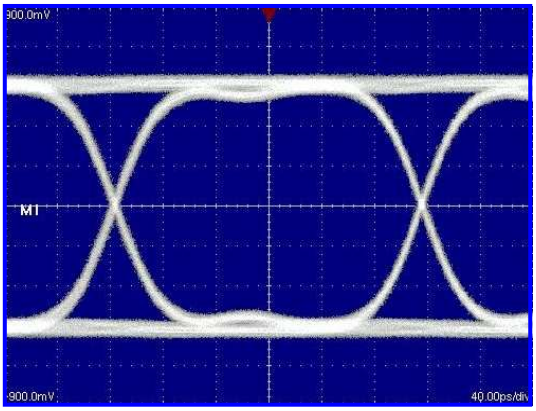
EYE DIAGRAM

(OC-48, Transmit Data Path)



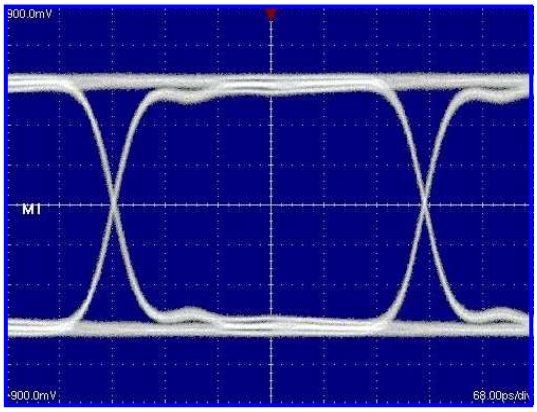
EYE DIAGRAM

(4.25Gbps, Receive Data Path)



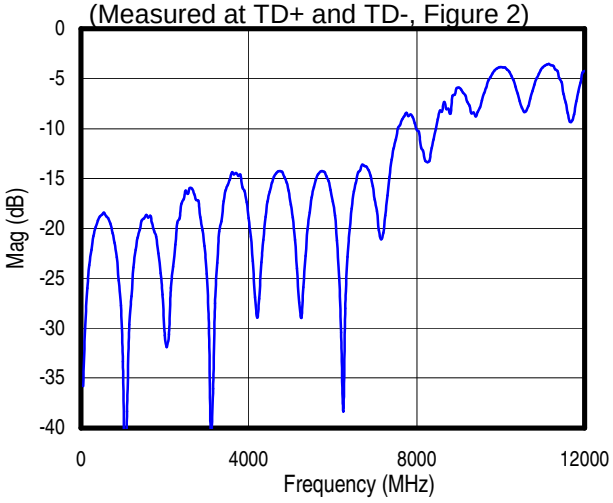
EYE DIAGRAM

(OC-48, Receive Data Path)



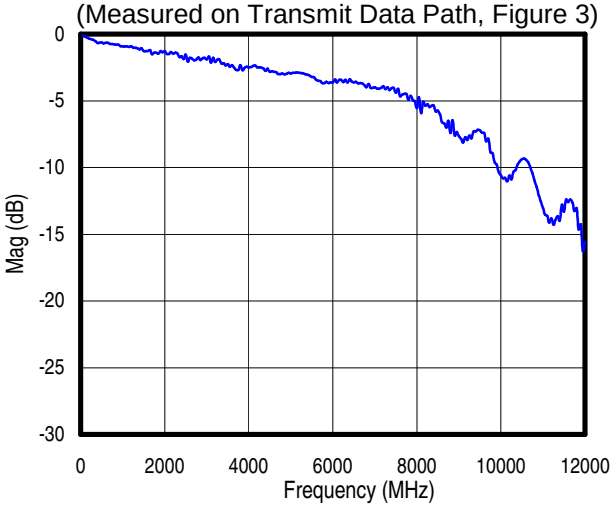
Differential S11 Magnitude

(Measured at TD+ and TD-, Figure 2)



Differential S21 Magnitude

(Measured on Transmit Data Path, Figure 3)



6 Application Information

6.1 Status LEDs

Status LEDs are connected to the low-speed output signals (LOS, TX_FAULT, MODDEF0) from the SFP module. The LED will illuminate when the signal is asserted. A READY LED is also provided to indicate communication has been established between the PC and the RS-232 to I^2C converter. See Sections 7 and 10 for more information.

6.2 DS3900 Compatibility

The DS3900 is a serial to I^2C converter developed by Dallas Semiconductor. The DS3900 is frequently used for programming digital potentiometer and controller ICs that are often used in optical modules. HFRD-15.3 uses similar hardware and the same firmware as the DS3900 for the serial to I^2C conversion. Therefore, the same software that was used with the DS3900 to control digital diagnostic ICs can be used with the HFRD-15.3 SFP host board.

6.3 Layout Considerations

Single-ended transmission lines are designed on the SFP host board. Changing the PCB layer profile (see Section 12) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

6.4 Supply Filter

The host board is required to provide power supply decoupling for transmitter and receiver supply voltages. HFRD-15.3 is designed with the recommend filters as per the SFP MSA.

A +3.3V supply for the digital control logic can be applied by a separate source through TP10 (with no shunt on JP7) or by connecting the digital supply (VDD) to the receiver or transmitter power supply connections using a shunt on JP7. See Sections 7 and 10 for more information.

7 I/O and Control Description

Component	NAME	FUNCTION
J1		SFP Module Connector (See Section 8)
J2	TD-	Transmitted Data Inverted Input, SMA Connector
J3	TD+	Transmitted Data Non-Inverted Input, SMA Connector
J4	RD+	Received Data Non-Inverted Output, SMA Connector
J5	RD-	Received Data Inverted Output, SMA Connector
J6	VCCR	SMA connector provided for injecting / measuring noise in the receiver power supply of the SFP module.
J7, J15	GND	Module / Host Board Ground
J8		DB9 connector. Connects to a PC when using RS-232 digital control of the I^2C bus (MODDEF1 / MODDEF2).
J9	VCCRX	+3.3V Receiver Power Supply Connection
J10	VCCT	SMA connector provided for injecting / measuring noise in the transmitter power supply of the SFP module.
J14		Alternate Power Supply Connections Pins 6, 4 -> GND. Pin 5 -> Unfiltered Transmitter +3.3V Supply, Direct Connection to J37 (VCCTX) Pin 3 -> Unfiltered Receiver +3.3V Supply, Direct Connection to J9 (VCCRX) Pin 2 -> VSS, Connection to GND through L4 Pin 1 -> Unfiltered Digital +3.3V Supply, Direct Connection to TP10
J37	VCCTX	+3.3V Transmitter Power Supply Connection
JU1	TX_DISABLE	Placing a shunt on JU1 enables the SFP module.
JU2	RATE_SELECT	Placing a shunt on JU2 connects the module rate select pin to VCCR.
JU3		Placing a shunt on JU3 from pin 1 to 2 connects the receiver +3.3V supply voltage (VCCRX) to the digital circuitry supply voltage (VDD). Placing a shunt on JU3 from pin 2 to 3 connects the transmitter +3.3V supply (VCCTX) to the digital circuitry supply voltage (VDD).
D3	MODDEF0	LED illuminates when an SFP module is not present.
D4	TX_FAULT	LED illuminates when TX_FAULT asserts.
D5	LOS	LED illuminates when LOS asserts.
D6	READY	Led blinks on and off when the RS-232 to I^2C converter is communicating with a computer that is running software written for the control interface.
TP3	LOS	Monitoring Test Point for LOS signal
TP4	MODDEF0	Monitoring Test Point for MODDEF0 signal
TP5	TX_FAULT	Monitoring Test Point for TX_FAULT signal
TP6	MODDEF2	Monitoring Test Point for MODDEF2 signal
TP7	MODDEF1	Monitoring Test Point for MODDEF1 signal

8 SFP Signal Definitions (20-Pin SFP Connector, J1)

I/O Direction assumes the SFP module as the reference. See SFP MSA section B2: *Pin Definitions* for the official definitions and more detailed information.

Connector Pin (J1)	I/O Type	NAME	Definition
1, 17, 20		VEET	Module Transmitter Ground. May be connected to VEER inside the SFP module.
2	LVTTL OUTPUT	TX_FAULT	
3	LVTTL INPUT	TX_DISABLE	
4	LVTTL INPUT / OUTPUT	MOD-DEF2	2-Wire Serial Interface Bi-Directional Data Line (Note 1)
5	LVTTL INPUT	MOD-DEF1	2-Wire Serial Interface Clock Line (Note 1)
6	LVTTL OUTPUT	MOD-DEF0	Pin is grounded by SFP module to indicate it is present (Note 1)
7	LVTTL INPUT	RATE SELECT	Optional receiver bandwidth selection input. Low or Open -> Reduced Bandwidth, High -> Full Bandwidth
8	LVTTL OUTPUT	LOS	Receiver Loss of Signal Output (Note 1). Output is high when receiver input signal is below the set threshold.
9, 10, 11, 14		VEER	Module Receiver Ground. May be connected to VEET inside the SFP module.
12	OUTPUT	RD-	Inverted Received Data Output, AC-coupled inside the SFP module
13	OUTPUT	RD+	Non-Inverted Received Data Output, AC-coupled inside the SFP module
15		VCCR	+3.3V Receiver Power Supply Connection. May be internally connected to VCCT inside the SFP Module.
16		VCCT	+3.3V Transmitter Power Supply Connection. May be internally connected to VCCR inside the SFP Module.
18	INPUT	TD+	Inverted Transmit Data Input, AC-coupled inside the SFP module
19	INPUT	TD-	Non-Inverted Transmit Data Input, AC-coupled inside the SFP module

Note 1: Open collector output. Must be pulled high (+3.15V to +3.6V) on host board through a 4.7kΩ to 10kΩ resistor.

9 Component List

DESIGNATION	QTY	DESCRIPTION
C1, C9, C10, C12, C13, C54	6	0.1µF ± 10% Ceramic Capacitor (0402)
C2 – C4, C14	4	1µF ± 10% Ceramic Capacitor (0402)
C5	1	Open (B-Case)
C6, C7, C11, C31	4	10µF ± 10% Tantalum Capacitor (B-Case)
C8, C53	2	0.01µF ± 10% Ceramic Capacitor (0402)
C15, C16	2	27pF ± 10% Ceramic Capacitor (0402)
D3 – D6	4	Red LED T1-Package
D7	1	Diode (Mini Type 2) Panasonic MA2YD15
J1	1	20-Pin SFP Connector AMP 1367073-1
J2-J5	4	Side Mount SMA Connector, Tab Contact
J6, J10	2	PCB Mount SMA Connector
J8	1	DB9 Female Connector Norcomp 182-009-212-161
J14	1	6 Position Terminal Block
JP1, JP2	2	2x8 Header, 0.1” spacing
JU1, JU2	2	2-Pin Header
JU3	1	3-Pin Header
L1, L2, L13	3	1µH Inductor (1008)
L4	1	600Ω Ferrite Bead (0603)
Q1	1	MOSFET 2N7002 (SOT23)
R1, R14-R19	7	Open (0603)
R2	1	2.2kΩ ±5% Resistor (0603)
R3 – R7	5	4.7kΩ ±5% Resistor (0603)
R10 – R13	4	300Ω ±5% Resistor (0603)
TP3-TP12, J7, J9, J15, J37	14	Test Point
U1, U2	2	Dual Inverter Fairchild NC7WZ04P6X
U3	1	Microcontroller Microchip PIC16F628-04I/SS
U4	1	MAX3223EAP
Y1	1	3.68MHz Crystal CTS CTX501

10 Schematic

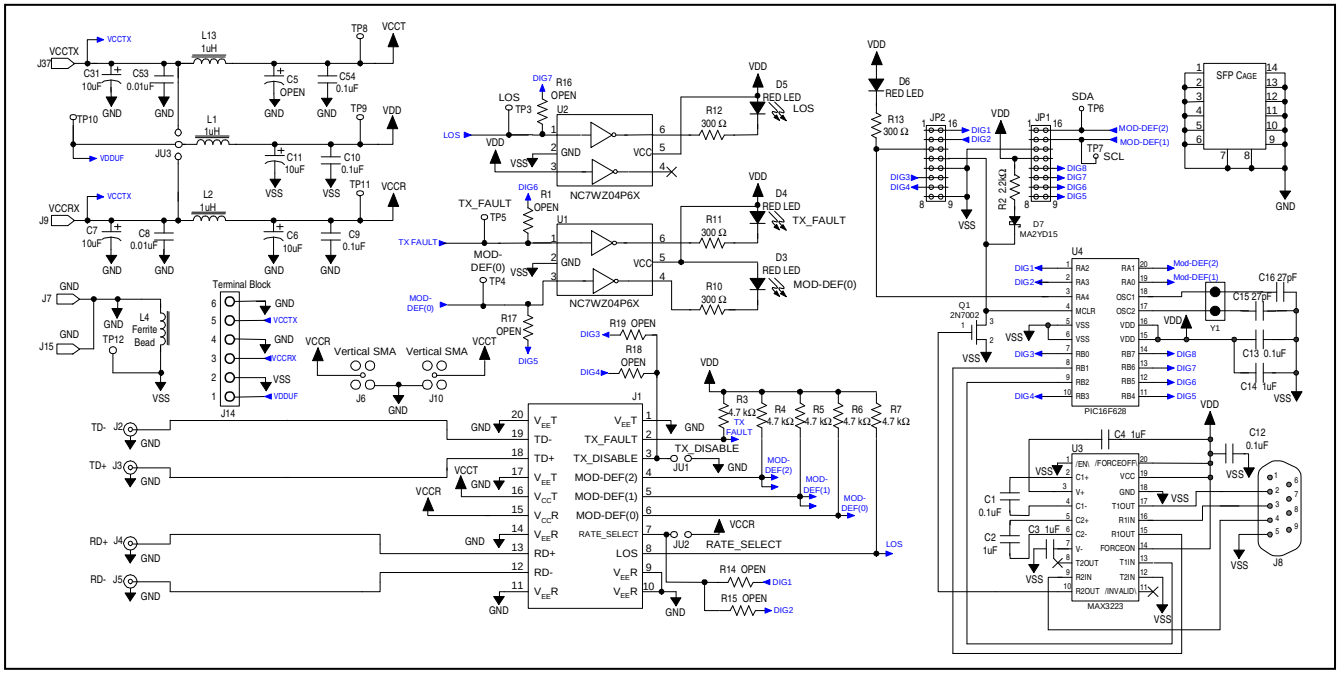


Figure 4. HFRD-15.3 SFP Host Board Schematic

11 Board Dimensions / Layout

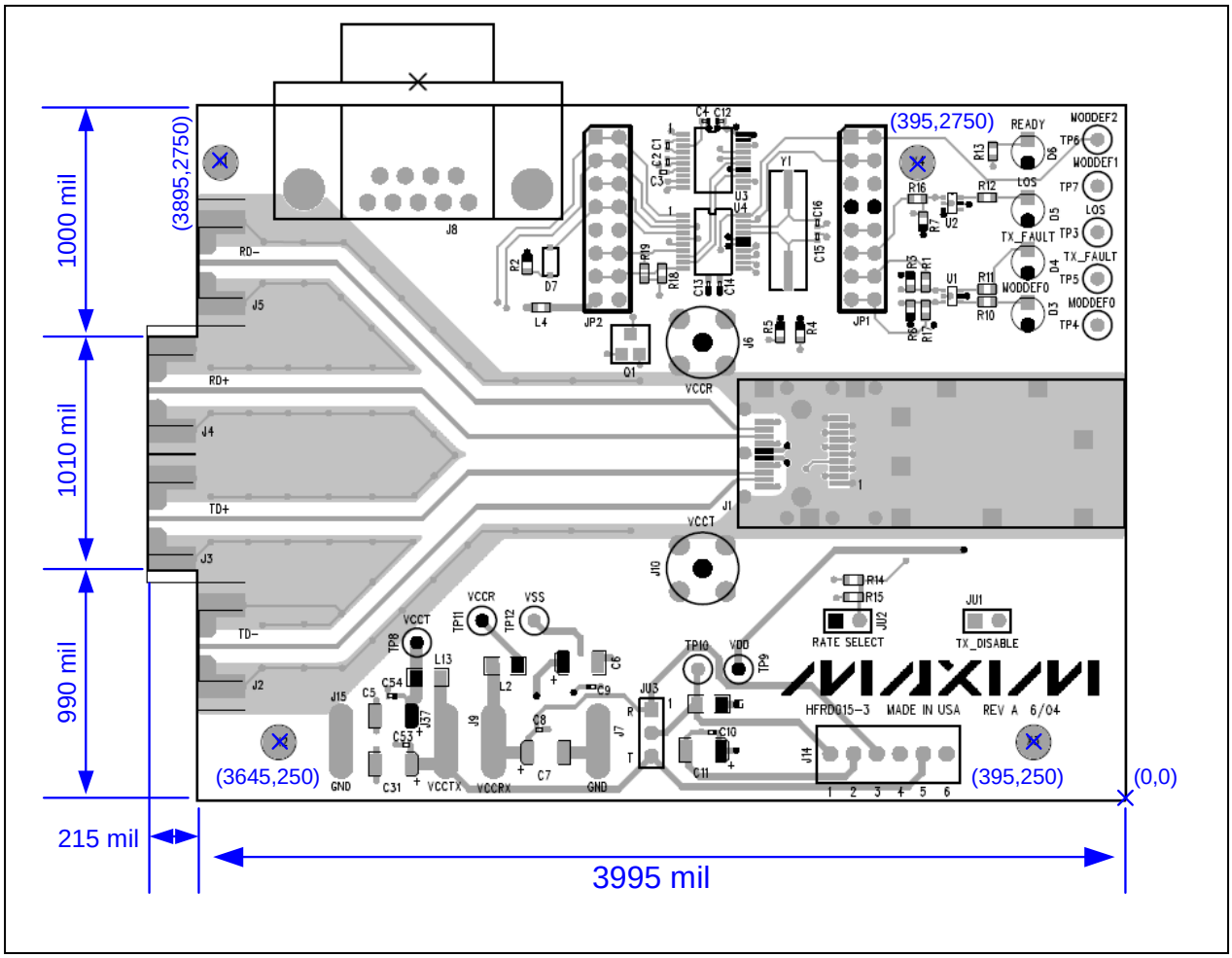


Figure 5. Host Board Dimensions / Layout

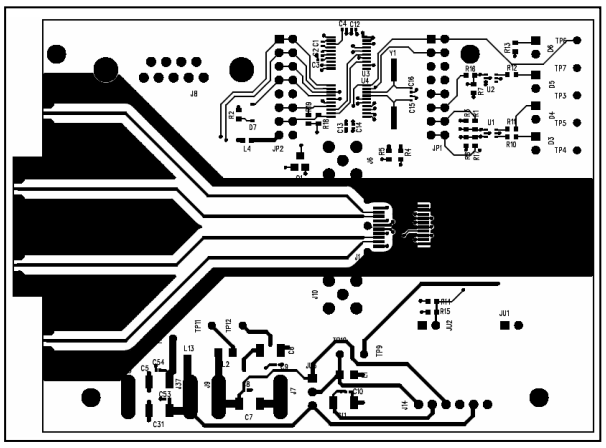


Figure 6. PC Board Layout – Component Side

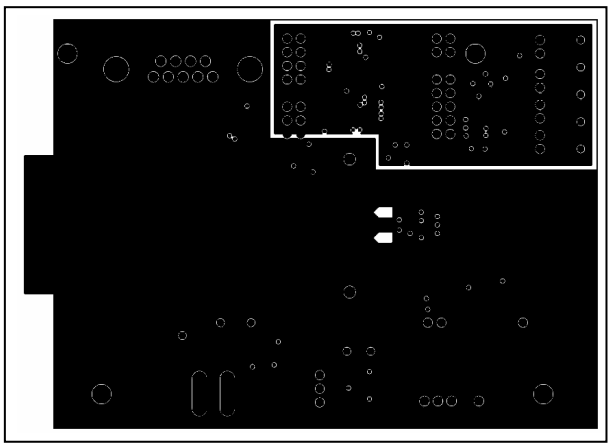


Figure 7. PC Board Layout – Ground Place

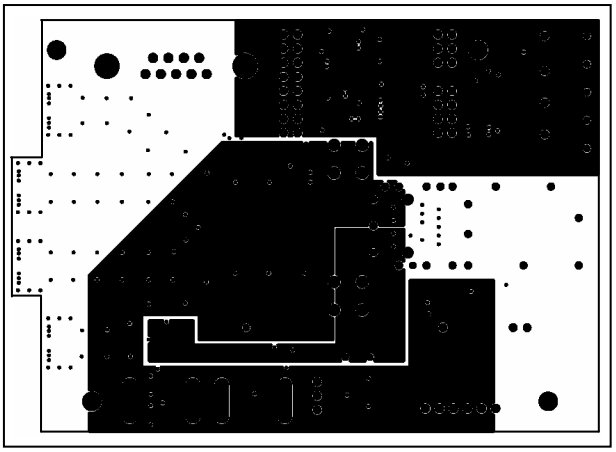


Figure 8. PC Board Layout – Power Plane

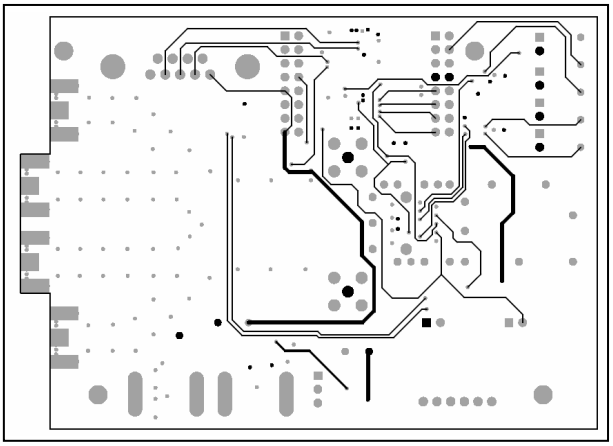


Figure 9. PC Board Layout – Solder Side

12 Layer Profile

The HFRD-15.3 SFP host board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is Rogers with a dielectric constant of ~ 4.3
2. 1oz copper foil

	SINGLE ENDED	COUPLED
A	20mil	10mil
B	>50mil	10mil
C	10mil	10mil
D	As Needed	As Needed

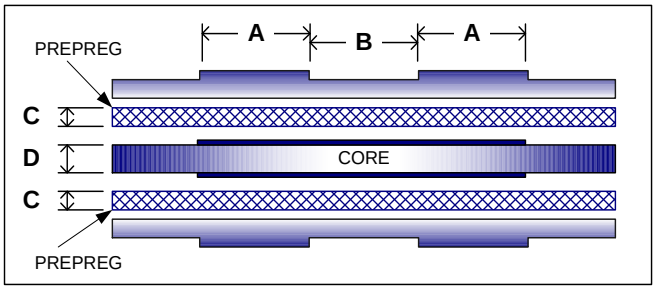


Figure 10. Layer Profile