## Datasheet

DS001033

# NanEyeM

## Miniature Camera Module

v2-00 • 2021-Jul-29

# Content Guide

# 1 General Description

NanEyeM is a miniature sized image sensor for vision applications where size is a critical factor. The ability of the camera head to drive a signal through long cables makes this the ideal component for minimal diameter endoscopes.

With a footprint of a just 1 $mm^2$, it features a 320x320 resolution with a high sensitive 2.4-micron rolling shutter pixel, with large full well capacitance. The sensor has been specially designed for medical endoscopic applications where high SNR is mandatory. The sensor has a high frame rate of about 50 fps to permit SNR enhancement and a smooth, low delay display over a wide range of standard interfaces. On the other side the frame rate can be set as low as 9 fps for usage of extended exposure time and lower power consumption.

The sensor includes a 10-bit ADC and a bit serial LVDS data interface. The sensor is able to drive the signal through a cable length of up to 3 m.

The data line is semi duplex, such that configuration can be communicated to the sensor in the frame brake. The exposure time, dark level, analog gain and frame rate can be programmed over the serial configuration interface.

## 1.1 Key Benefits & Features

The benefits and features of NanEyeM, Miniature Camera Module are listed below:

**Figure 1:**
**Added Value of Using NanEyeM**

| Benefits | Features |
|---|---|
| Designed for the toughest confined space requirements | Footprint of 1 $mm^2$ with cable assembly |
| Smooth and accurate image | Frame rate of 4 – 49 fps @ 320x320 resolution |
| Reach further | Possible to drive a signal through an endoscope of up to 3 m |
| Flexible connection | Possible to switch the serial interface to single ended mode for easier connection to ISPs. |
| Affordable single use application | Designed with a focus on cost efficiency |
| Envision the unseen | 2.4-micron high sensitive pixel with 102.4 k pixel resolution |

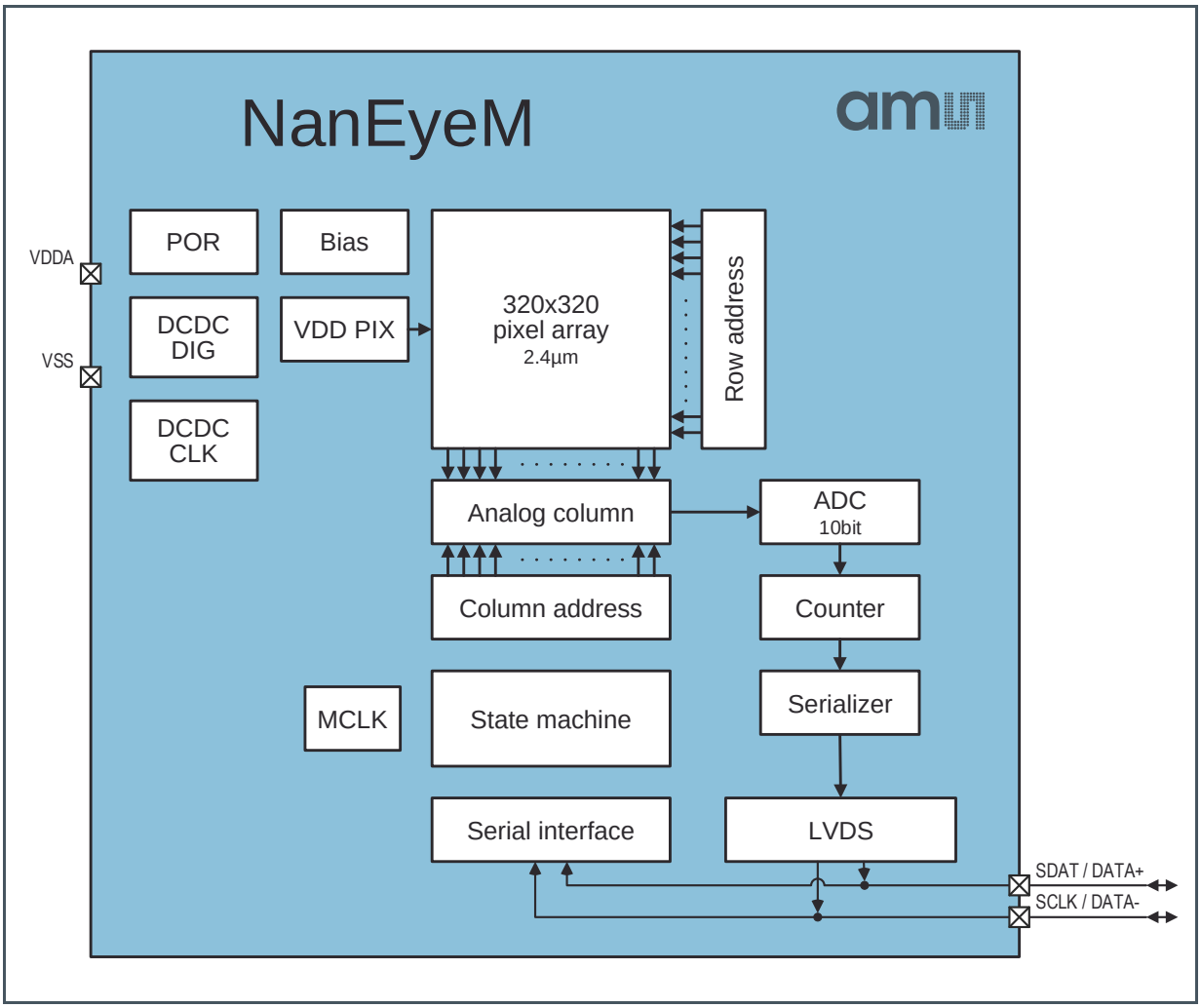
## 1.2 Applications

- Medical Applications
  - Endoscopy
  - Intraoral Scanning

## 1.3 Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**
**Functional Blocks of NanEyeM**



# 2 Ordering Information

| Ordering Code | Package | Optics | Delivery Form | Delivery Quantity |
|---|---|---|---|---|
| **RGB version** | | | | |
| NEM_RGB_2M_FOV120_F4.0 | with 2 m cable | FOV120; F4 | Spool | n/a |
| NEM_RGB_2M_FOV120_F4.0_FF(1) | with 2 m cable | FOV120; F4 | Spool | n/a |
| NEM_RGB_2.5M_FOV120_F4.0 | with 2.5 m cable | FOV120; F4 | Spool | n/a |

(1) Non standard variant, for availability please check with our sales team.

**Information**

As module the device is mounted on a flat ribbon cable measuring up to 2 m in length that connects to the base station. However, if the customer requirements are discussed, it may be possible to assemble a slightly longer cable (up to 3 m).

**Information**

Device tractability is based on the serial numbers labeled on the spools.

**CAUTION**

The module is NOT supplied sterile! Medical use of the system, not integrated into a medical device, may lead to serious harm, illness or death!

# 3 Pin Assignment

## 3.1 Pin Diagram

**Figure 3:**
**Pin Assignment Module Cable (camera front view)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **4-wire cable** | VSS | SCLK / DATA- | SDAT / DATA+ | VDDA | | |

**Figure 4:**
**4-Wire Cable Pinout**

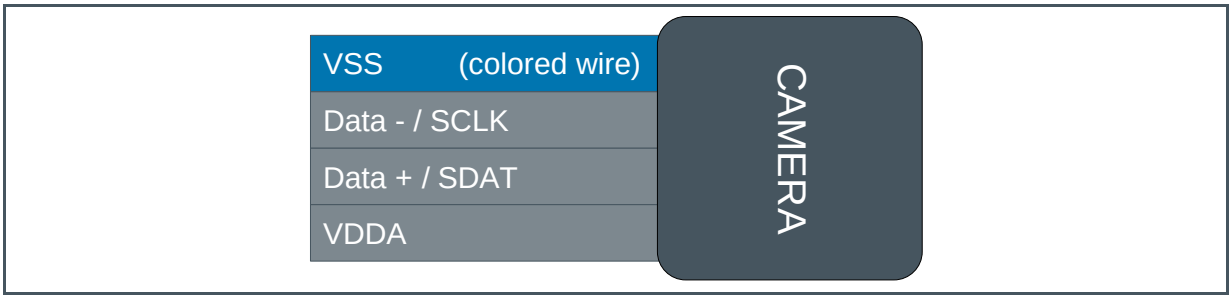
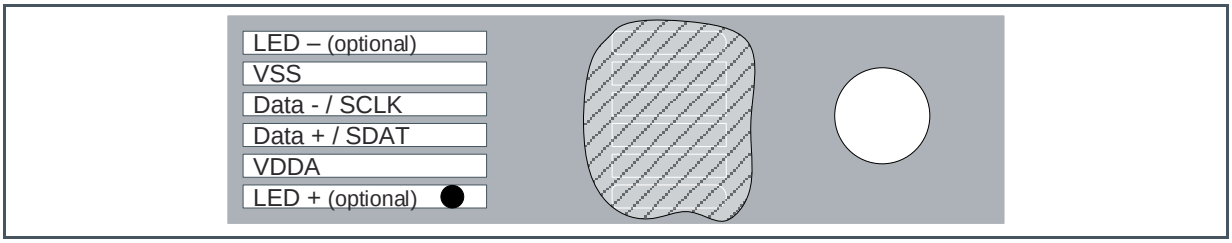



**Figure 5:**
**6-Wire Cable FlexPCB Connector Pinout**



## 3.2 Pin Description

**Figure 6:**
**Pin Description of NanEyeM**

| Pin Number | | Pin Name | Pin Type(1) | Description |
|---|---|---|---|---|
| Cable 4-Wire | Connector 6-Wire | | | |
| | 6 | LED- | AO | LED cathode |
| 1 | 5 | VSS | VSS | Ground supply |
| 2 | 4 | SCLK / DATA- | DIO | Serial clock input, LVDS neg. output |
| 3 | 3 | SDAT / DATA+ | DIO | Serial data input/output, LVDS pos. output |
| 4 | 2 | VDDA | Supply | Positive supply |
| | 1 | LED+ | AI | LED anode |

(1) Explanation of abbreviations:
DIO Digital Input/Output
AI Analog Input
AO Analog Output

# 4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 7**
**Absolute Maximum Ratings of NanEyeM**

| Symbol | Parameter | Min | Max | Unit | Comments |
|---|---|---|---|---|---|
| **Electrical Parameters** | | | | | |
| $V_{DDA}$ | Supply Voltage to Ground | -0.5 | 3.6 | V | |
| $V_{SCLK}$, $V_{SDAT}$ | Input Pin Voltage to Ground | -0.5 | 3.6 | V | |
| **Electrostatic Discharge** | | | | | |
| $ESD_{HBM}$ | Electrostatic Discharge HBM | | ± 2 | kV | JEDEC JS-001-2017 |
| **Temperature Ranges and Storage Conditions** | | | | | |
| $T_A$ | Operating Ambient Temperature Full Module | 15 | 55(1) | °C | Full module incl. cable |
| | Silicon Sensor only | 0 | 70(1) | °C | Good image quality 15 to 55 °C only |
| $RH_{NC}$ | Relative Humidity (non-condensing) | 5 | 85(1) | % | |
| $T_{STRG}$ | Storage Temperature Range | - 40 | 30 | °C | (2) |
| $RH_{NC\_STRG}$ | Long Term Storage Humidity | 0 | 60 | % | |
| $t_{STRG}$ | Storage Time | | 3 | yrs | |
| $MSL_{\_M+CABLE}$ | Moisture Sensitivity Level Lens Module with Cable | | N/A | | Not applicable as only the cable gets soldered not the module |

(1) Long term exposure toward the maximum operating temperature will accelerate device degradation.
(2) UV curing process is in our conviction not causing any harm to the sensor.

# 5 Electrical Characteristics

The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Parameters without tolerance are typical values.

**Figure 8:**
**Electrical Characteristics of NanEyeM**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDDA | Supply Voltage | | 3.2 | 3.3 | 3.4 | V |
| $VN_{RMS}VDDA$ | RMS noise on VDDA | | | | 5 | mV |
| $VN_{PP}VDDA$ | Peak to peak noise on VDDA | | | | 20 | mV |
| $P_{CLK\_STD}$(1) | Internal pixel clock | set by mclk_mode [1:0] and high_speed[0] | | 1.03<br>2.05<br>4.09 | | MHz |
| $P_{CLK\_HS}$(2) | Internal pixel clock high speed | set by mclk_mode [1:0] and high_speed[0] | | 1.31<br>2.59<br>5.22 | | MHz |
| $P_{tot\_3.3}$ | Total power consumption | Idle mode = OFF, MCLK=31 MHz | | 12 | | mW |
| | | Idle mode = ON | | 3.2 | | mW |
| **Digital Upstream Interface** | | | | | | |
| $V_{IL}$ | SCLK,SDAT Low Level input voltage | | -0.3 | | 0.4 | V |
| $V_{IH}$ | SCLK,SDAT High Level input voltage | | VDDA -0.3 | | VDDA +0.3 | V |
| $T_S$ | Setup time for upstream configuration relative to SCLK | | 3 | | | ns |
| $T_H$ | Hold time for upstream configuration relative to SCLK | | 3 | | | ns |
| $f_{SCLK\_LVDS}$ | SCLK frequency in LVDS | | | | 2.5 | MHz |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LVDS Downstream Interface** | | | | | | |
| $V_{CM}$ | Common mode output voltage (DATA+/-) | | 1 | 1.4 | 1.8 | V |
| $I_{DATA+,DATA-}$ | LVDS output signal current, | Set by output_curr[1:0] | | 600 … 2000 | | µA |
| $B_{CLK\_STD}$ | Bit clock for serial data transmission (12x Pclk) | Set by mclk_mode[1:0] and high_speed[0] | | 12<br>25<br>49 | | MHz |
| $B_{CLK\_HS}$ | Bit clock for serial data transmission high speed (12x Pclk) | set by mclk_mode[1:0] and high_speed[0] | | 16<br>31<br>63 | | MHz |
| $J_{DATA}$ | Jitter data clock | | -20 | | 20 | % |
| | LVDS differential peak-peak swing | Zterm=120Ω | | 72…240 | | mV |
| $T_{slew,\ rising}$ | Output slew rate of rising edge | | | 3 | | ns |
| $T_{slew,\ falling}$ | Output slew rate of falling edge | | | 3 | | ns |

(1) _STD –> assuming High Speed bit OFF
(2) _HS -> assuming HS Speed bit ON

## Figure 9:
## Electro-Optical Characteristics of NanEyeM

| Parameter | Value | Remark |
|---|---|---|
| Resolution | 102.4 kP, 320 (H) x 320 (V) | |
| Pixel size | 2.4 µm x 2.4 µm | |
| Optical format | 1/15” | |
| Pixel type | 4T shared, FSI | |
| Shutter type | Rolling Shutter | |
| Color filters | RGB (Bayer Pattern) | |
| Micro lenses | Yes | |
| Lens stack | BF = 8 mm<br>DOF = 4 mm to infinite<br>EFL = 367 µm | Triple element lens |
| Programmable register | Sensor parameter | Exposure time, dark level, frame rate, analog gain and LVDS drive current |
| Programmable gain | 4 steps 0.8x/1x/1.3x/2x | Analog |
| Exposure times | 0.13 – 261 ms | @ default main clock |
| ADC | 10-bit | Column ADC |
| Frame rate | 4 - 38 fps (5 - 49 fps HS mode) | Adjustable via register settings |
| Output interface | 1x LVDS @ 63 Mbit/s | @ 49 Hz |
| Size | 1050 µm x 1050 µm ±60 µm | Module including sensor, lens stack, side wall painting and cable assembly |

**Figure 10:**
**Electro-Optical Parameter**

| Parameter | RGB | Unit |
|---|---|---|
| Responsivity | 8.9 | DN/nJ/cm$^2$ |
| Full well capacity | 6.2 | ke- |
| Conversion gain | 0.137 | DN/e- |
| QE | 42.5 | % |
| Temporal read noise in<br>dark / dark noise | 0.84<br>6.1 | DN<br>e- |
| Dynamic range | 60 | dB |
| SNR (50% sat) | 34 | dB |
| SNR max | 38.4 | dB |
| Dark current @ 60 °C | 9.2 | DN/s |
| DSNU | 0.84 | DN |
| PRNU | 1.3 | % |
| FSD | 860 | DN |

(1) Measured on a RGB sensor at 530 nm illumination, for MCLK=25 MHz setting. The values are all without software correction. The measurement methods used to get these values are those recommended by the European Machine Vision Association standard 1288 for the Machine Vision Sensors and Cameras: http://www.emva.org/standards-technology/emva-1288/

(2) The values show in the table are averaged values across several samples and different operating points (supply, clock speed, gain, etc).

# 6 Typical Operating Characteristics

**Figure 11:**
**QE & Responsibility (RGB)**

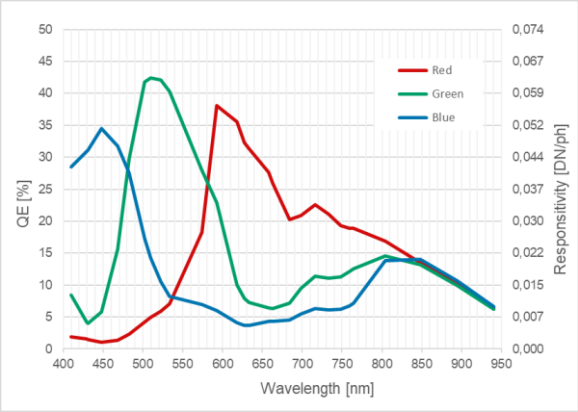



**Figure 12:**
**MTF**

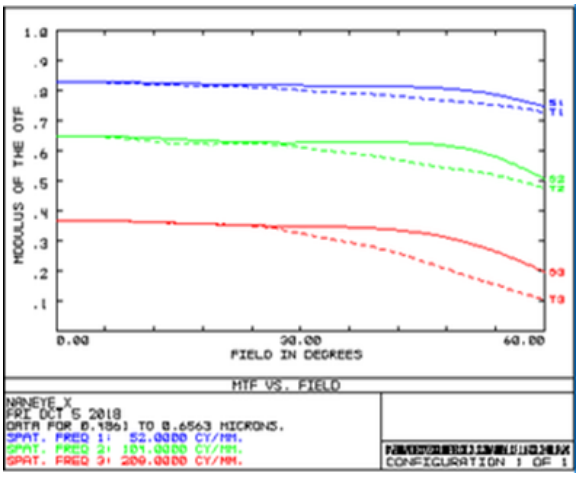
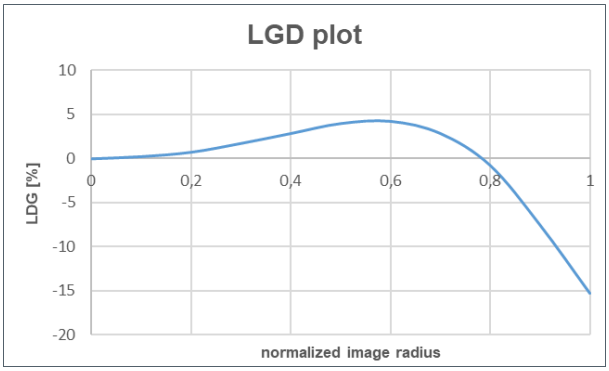



**Figure 13:**
**Distortion**



# 7 Functional Description

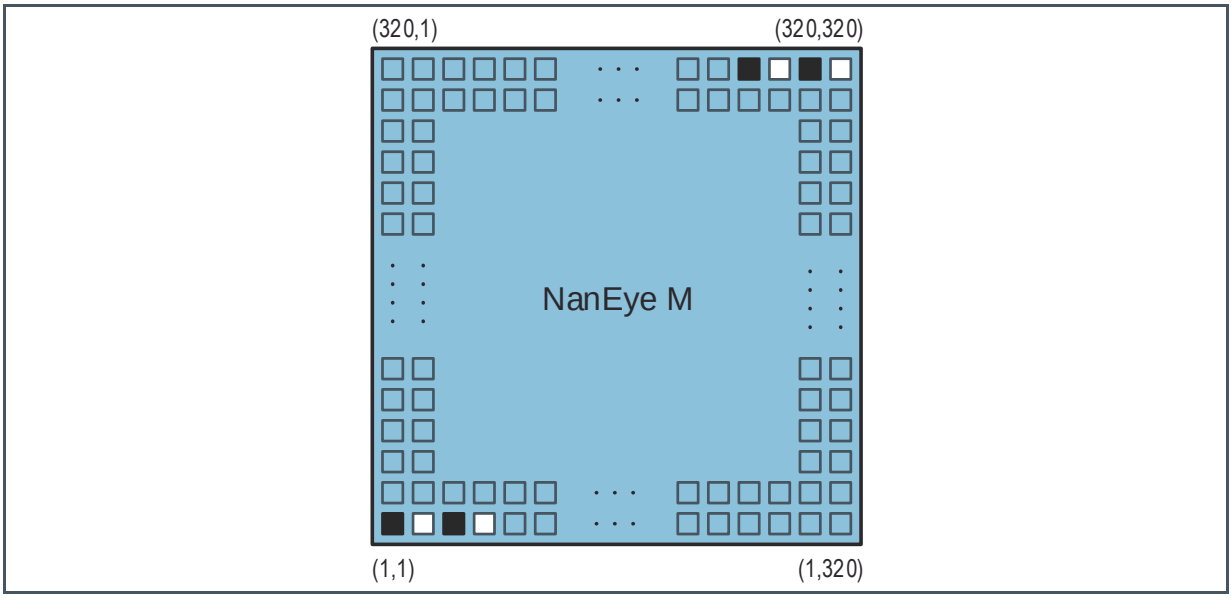
## 7.1 Sensor Architecture

Figure 2 shows the image sensor architecture. The internal state machine generates the necessary signals for image acquisition. The image information received in the pixels (rolling shutter) is read out sequentially, row-by-row. On the pixel output, an analog gain is possible. The pixel values then passes to a column ADC cell, in which analog to digital conversion is performed. The digital signals are then read out over a LVDS or single ended output channel.

### 7.1.1 Pixel Array

The pixel array consists of 320 x 320 square rolling shutter pixels with a pitch of 2.4 µm (2.4 µm x 2.4 µm). The pixel architecture used in this sensor is a 4T type structure, with two pixel vertically shared. This results in an optical area of 768 µm x 768 µm (1.09 mm diameter).

**Figure 14:**
**Pixel Array**




The pixels are designed to achieve maximum sensitivity with low noise (using CDS). Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency.

There are two electrical black pixels and two electrically saturated pixels on the upper right and lower left hand corner, which may be used to check consistency of received data.

Black pixel (1,1) can be used to compensate the black offset by subtraction it from the individual received pixel values.

### 7.1.2 Analog Front End

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC. The column ADC converts the analog pixel value into a digital value. The architecture allows a full linear AD conversion of 10 bits, with a programmable conversion gain. All gain and offset settings can be programmed using the Single Ended Serial interface.

### 7.1.3 LVDS Block

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data. During transfer of the image data, the pixel values are transmitted in bit serial manner with 12 bits and embedded clock using Manchester coding [start bit (1 bit) + data (10 bit) + stop bit (1 bit)]. The sensor has one LVDS output pair.

### 7.1.4 State Machine

The state machine will generate all required control signals to operate the sensor. The clock is derived from an on-chip master clock generator (LVDS mode). The clock speed and so the number of transmitted frames can be set via registers bits. A detailed description of the registers and sensor programming can be found in chapter 7.4.2 and chapter 8 of this document.

### 7.1.5 Single Ended Serial Interface

The single ended serial interface is used to load the registers with data. It is multiplexed with the LVDS interface, data can be send in the frame windows of the receiving image information. The data in these registers is used by the state machine and ADC block while driving and reading out the image sensor. Features like exposure time, gain, offset and frame rate can be programmed using this interface. Chapter 7.4.2 and chapter 8 contain more details on register programming.

The sensor will start up in IDLE MODE, having the single ended serial interface active until the idle mode is deactivated.

### 7.1.6 Optics

The optional optics available for the sensor is a high performance miniature lens module. It will be directly mounted on the image sensor and has its best focus position defined by design, so no mechanical set of focus is needed. The front of the lens module is made of D 263®T eco clear borosilicate glass. The design is made in such way that the surface towards the object is flat, so the

lens performance is not influenced by the medium between the object and lens. Only the opening angle of the lens is reduced when the system operates in water.

## 7.2 Driving the NanEyeM

The NanEyeM image sensor is based on CMOS technology and is a system on chip, which means that all needed clocks and additional supplies are generated on-chip.

### 7.2.1 Supply Voltage

The sensor operates from a single supply voltage VDDA. In addition, a VDDPIX (reset voltage for the pixels) as well as separated supplies for digital blocks are generated internally.

For reference schematic and external components please refer to chapter 9 Application Information.

### 7.2.2 Start-Up Sequence

The sensor is fully self timed and operates in a free running master mode. After power up, the sensor performs an internal power on reset, and then moves to IDLE MODE, having the single ended serial upstream interface active. This gives the possibility to adjust the sensor settings, especially selecting the output mode, before disabling the idle mode and starting the image data transmission.

### 7.2.3 Reset Sequence

No special reset sequence needed.

### 7.2.4 Frame Rate

The frame rate can be adjusted be changing the settings for the master clock (MCLK). There is also a high speed mode available to generate even higher frame rates.

## 7.3 Matrix Readout

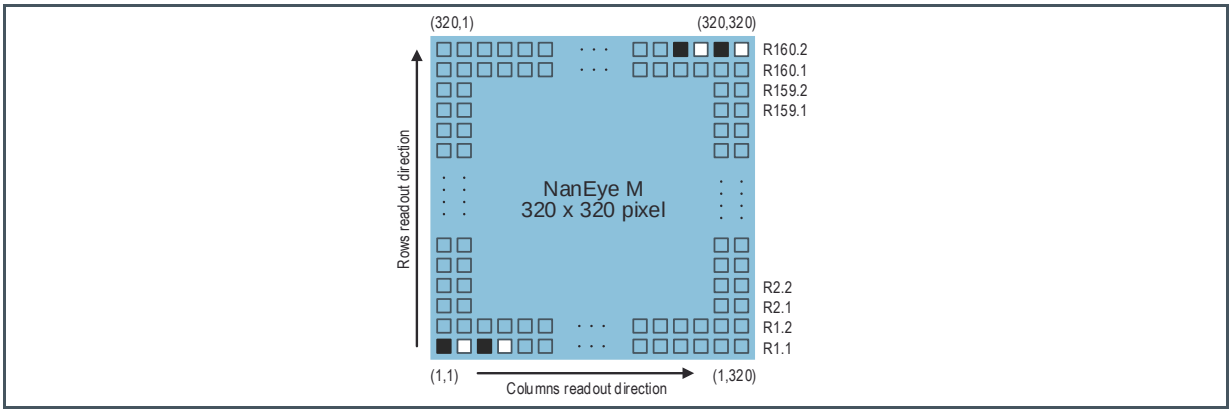
To guarantee a high fill factor a pixel layout with the two vertical electrical shared pixels has been developed.

The matrix readout is according the following sequence:

- Read first row (R1.1), starting in the position (1;1) and finishing in the position(1;320)
- Read second row (R1.2), starting in the position (2;1) and finishing in the position (2;320)
  ...
- Read last row (R160.2), starting in the position (320;1) and finishing in the position (320;320)

Note that (row,column), i.e., (2;1) represents row 2 column 1.

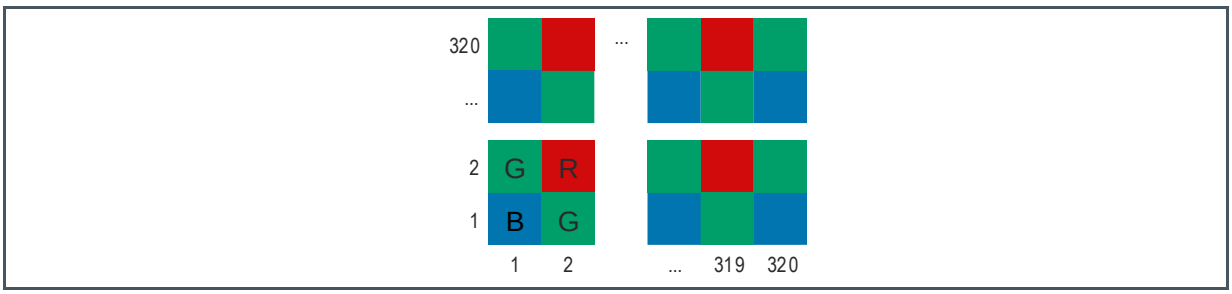
**Figure 15:**
**Shared Pixel Matrix Readout**




### 7.3.1 Color Filters

The color filters used for NanEyeM are applied in a Bayer pattern. The first pixel read-out, pixel (1,1), is the bottom left one and has a blue filter.

**Figure 16:**
**Colored Version Bayer Pattern Matrix**



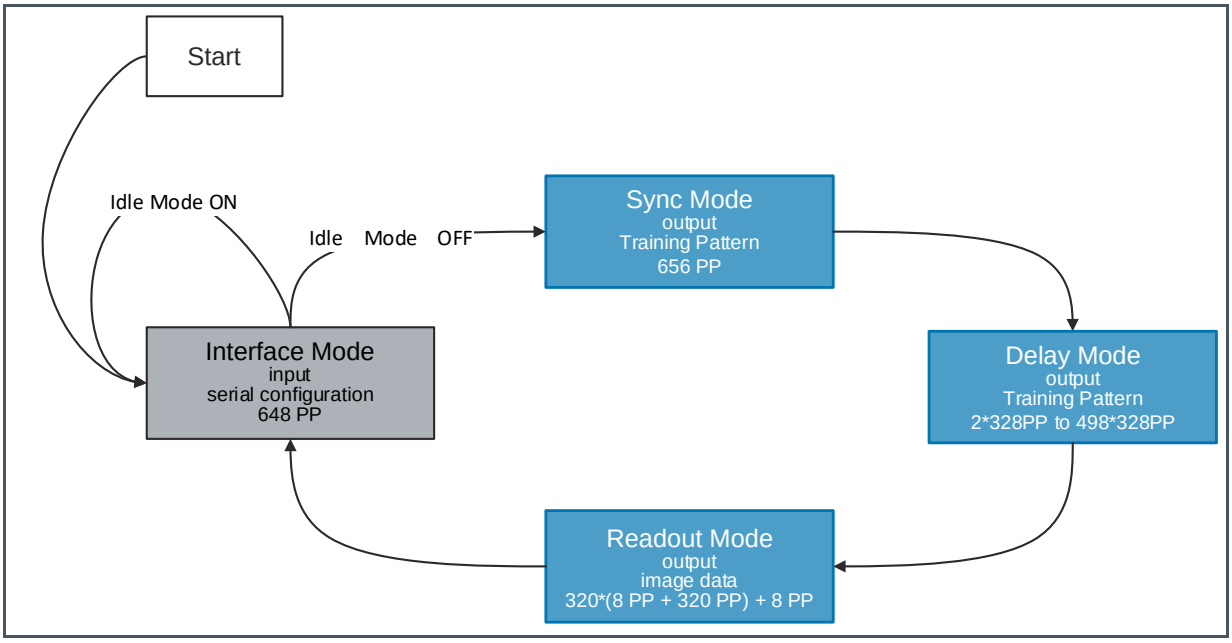
### 7.3.2 Sequence of Operation

The NanEyeM sensor will start in INTERFACE MODE waiting for configuration and request to leave idle mode. After the request, the sensor will go to a loop of 4 modes, which are described below. The frame time is defined by the total duration of these 4 modes:

- INTERFACE MODE: during this mode, which is active during 648 PP (Pixel Period) it is possible to write and update the register configuration. In this mode DATA pins are used as SDAT and SCLK.
- SYNC MODE: during this mode the sensor is transmitting training pattern to allow the sensor synchronization (duration of 656 PP).
- DELAY MODE: during this mode the sensor will keep the previous state during the programmed time while sending the sync pattern. The time can be programmed between 2 to 498 row periods.
- READOUT MODE: during this mode the sensor assumes that the synchronization is done and starts to send image data, the pixel values are transmitted in bit serial manner over an LVDS channel with embedded clock, or single ended depending on the selected transmission mode. Note that before each row a Start of Row identification is sent with the duration of 8 PP and that after the last row an End Of Frame is sent with the duration of 8 PP.

The sensor transmit synchronization pattern at least for the period of four rows, corresponding to the SYNC MODE and to the DELAY MODE (if set to the minimum programmable value). But it can transmit the pattern continuously for a longer time period, according the rows_delay[4:0] value programmed, which can take from 2 to 498 row clock period (2*328PP to 498*328PP).

**Figure 17:**
**Sequence of Operation**




(1) PP refer to Pixel Period.

**Figure 18:**
**Matrix Readout Sequence**

| Phase # | Status | Start bit | Data XOR | Interface Status | Duration | Function |
|---|---|---|---|---|---|---|
| **INTERFACE MODE** | | | | | | |
| SERIAL | Time for serial configuration(1) | N/A | N/A | S_INT IN | 648 PP(2) | Serial Interface |
| **SYNC MODE** | | | | | | |
| SYNC | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 328*2 PP | Re-Synchronization |
| **DELAY MODE** | | | | | | |
| DELAY | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 328*2 PP to 328*498 PP | Programmed Delay |
| **READOUT MODE** | | | | | | |
| RD R1.1 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 1) |
| RD R1.2 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 2) |
| RD R2.1 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 3) |
| RD R2.2 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 4) |
| Readout other rows | | | | | | |
| RD R160.1 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 319) |
| RD R160.2 | Transmission of continuous 0 | 0 | Yes | LVDS OUT | 8 PP | Start of Row |
| | Transmission of 320 pixel values | 1 | Yes | LVDS OUT | 320 PP | Image Data (Row 320) |
| RD EOF | Transmission of continuous 0 | 0 | No | LVDS OUT | 8 PP | End of Frame |

(1) It is recommended to drive the data bus during the entire upstream communication phase, even if no register data is sent to the sensor. This is to avoid pick up of EMI on the lines floating during the communication phase when not driven by the application.

(2) When IDLE MODE is OFF. If IDLE MODE is enabled the sensor remains in this working mode until the IDLE MODE is disabled.

**CAUTION**

- The sensor fully is self timed and cycles between the downstream and the upstream mode. Therefore it is the user's responsibility to tristate the upstream drivers of the serial configuration link prior to the start of data transmission from the sensor.
- Due to the limited current output from the sensor it is not expected that conflicting drive of the data lines will permanently destroy the sensor, however this condition would seriously degrade the data integrity and is not qualified in terms of device reliability and life time.

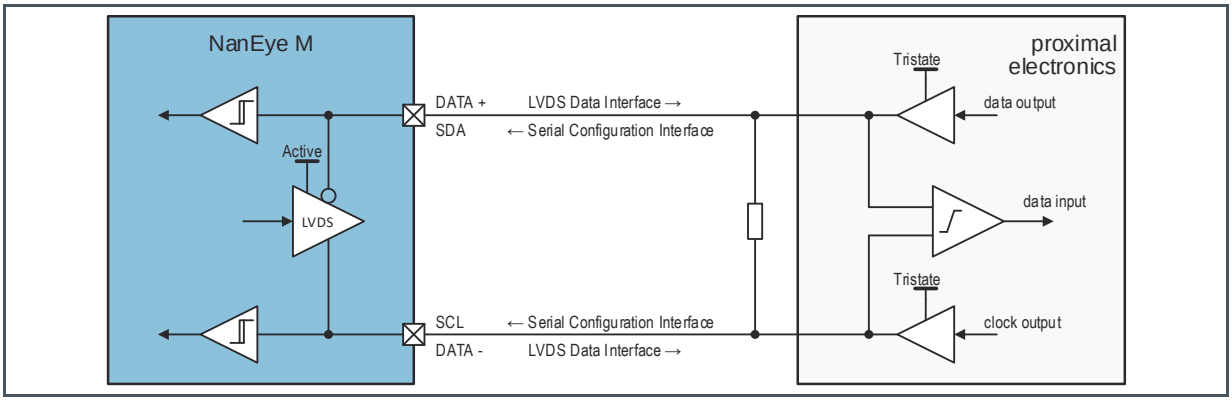
## 7.4 Serial Interface

The chip features a bi-directional data interface. During transfer of the image data, the pixel values are transmitted in bit serial manner over an LVDS channel with an embedded clock. After each frame, the data interface is switched for a defined time to an upstream configuration interface. This needs a synchronization every time it passes from the upstream to a new downstream mode at the image receiver side. The positive LVDS channel holds the serial configuration data and the negative channel holds the serial interface clock.

By register configuration the downstream interface can be chosen to be LVDS type with the serial data EXOR combined with the bit clock (Manchester Code).

For any application where the sensor is used with connection cable between the sensor and the receiver, the use of the LVDS mode is recommended.

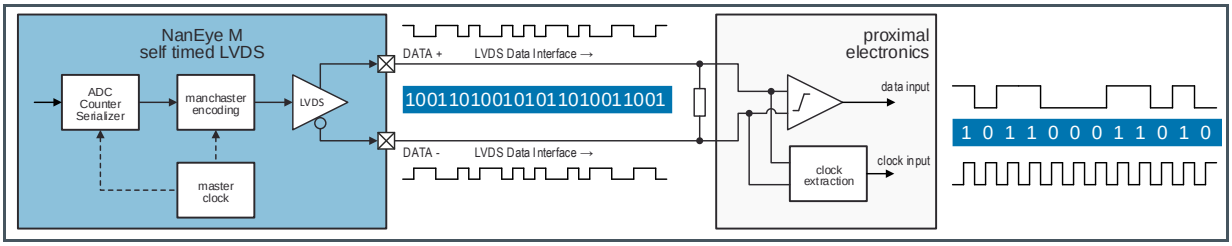
**Figure 19:**
**Data Interface Between Sensor and Proximal Electronics**



### 7.4.1 NanEyeM LVDS Data Interface (Downstream)

The NanEyeM image data on chip is generated as a 10-bit representation. A start and a stop bit is then added to the data. The bit serial data interface then transmits the data with 12 times the pixel frequency.

**Figure 20:**
**LVDS Downstream Mode**




**Data Word**

The data word is EXOR gated with the serial clock before sent bit serial according to the following scheme:

**Figure 21:**
**Data Word Encoding**

| Bit # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | Start | Pixel Data (10 bits) | | | | | | | | | | Stop |
| Content | 1 | MSB | | | | | | | | | LSB | 0 |

An example of this is:

- 10-bit data word: 0110001101
- Including start and stop bits: **1**01100011010**0**
- 12-bit word EXOR with the data clock:
  - 01 01 01 01 01 01 01 01 01 01 01 01 - data clock (main clock)
  - 11 00 11 11 00 00 00 11 11 00 11 00 – 12-bit data @ data clock frequency
  - 10 01 10 10 01 01 01 10 10 01 10 01 - data word result

### Training Pattern Word

The training pattern is transmitted during SYNC MODE and DELAY MODE, and also during READOUT MODE as Start of Row identification. It is a 12-bit word with all 0's, start and stop bit also at 0, EXOR gated with the main clock.

**Figure 22:**
**Training Pattern Word Encoding**

| Bit # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | Start | Start Row | | | | | | | | | | Stop |
| Content | **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

An example of this is:

- 10-bit data word: 0000000000
- Including start and stop bits: **0**00000000000**0**
- 12-bit word EXOR with the data clock:
  - 01 01 01 01 01 01 01 01 01 01 01 01 - data clock (main clock)
  - 00 00 00 00 00 00 00 00 00 00 00 00 – 12-bit at 0's @ data clock frequency
  - 01 01 01 01 01 01 01 01 01 01 01 01 – training pattern word result

### End of Frame Word

The end of frame word is similar to the training pattern, it is a 12-bit word with all 0's, start and stop bit also at 0, but in this particular case it is not EXOR with main clock. It is transmitted in the end of the readout phase (READOUT MODE).

**Figure 23:**
**End of Frame Word Encoding(1)**

| Bit # | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | Start | Start Row | | | | | | | | | | Stop |
| Content | **0** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) No EXOR with main clock!

An example of this is:

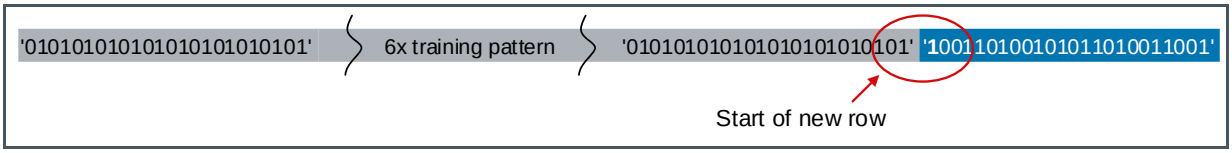
- 10-bit data word: 0000000000
- Including start and stop bits: **0**00000000000**0**
- 12-bit word **no** EXOR with the data clock:
  - 01 01 01 01 01 01 01 01 01 01 01 01 – data clock (main clock)
  - 00 00 00 00 00 00 00 00 00 00 00 00 – 12-bit at 0's @ data clock frequency
  - 00 00 00 00 00 00 00 00 00 00 00 00 – end of frame word result

### Start of Row Identification

Note that the start of row identification consist in sending the training pattern (010101010101010101010101) 8 times.

After 8 times transmitting the training pattern the data transmission for a particular row starts. Note that is possible to identify a new row easily by detecting two ones after the eight training pattern words. The ones appearance results from the last bit of the start line and the first bit of the image data (start bit XOR with data clock) as is shown below:

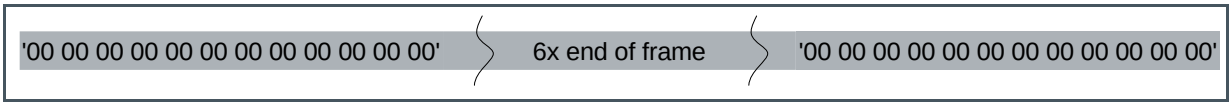
**Figure 24:**
**Start of Row Identification**




### End of Frame Identification

The End of Frame identification is sent after the last row and before the Serial Phase, it is the End of Frame word repeated 8 times.

**Figure 25:**
**End of Frame Identification**




### Re-Sync Identification

The Re-sync identification is sent during the SYNC MODE after the INTERFACE MODE (serial upstream configuration phase) in order to restart the sensor synchronism. It will send the training pattern word during 656 PP.

### DELAY MODE Identification

During DELAY MODE the training word is sent 2*328 to 498*328 times. The number of repetitions can be programmed with rows_delay[4:0].

### 7.4.2 Serial Configuration Interface (Upstream)

The serial interface is active for 648 PP (INERFACE MODE) and consists of two 16-bit write only registers. The registers can be updated between frames by the serial data line - SDAT and by the serial clock line – SCLK external controlled signal. The registers are written by sending a 4-bit update code, followed by a 3-bit register address (only register 000 and 001 are implemented), 16-bit register data and a bit fixed to “0”.

Sending data to the sensor must not be done with the first clock pulse provided to the sensor. It is required to send at least one activation clock pulse upfront. It needs to be avoided to send configuration data in the last PP of the INTERFACE MODE.

All data is written MSB to LSB. Data is captured on the rising edge of SCLK. It is recommended to change SDAT on the falling edge of SCLK to guarantee maximum set-up and hold times.

The content of the input shift register is updated to the effective register, once a correct update code (1001) has been received and shifted by 24 serial clocks. The input shift register is reset to all 0's, 1 SCLK clock after the code detection.

The below table indicates the sequence of writing update code, register address and register data.

**Figure 26:**
**Register Update Sequence**

| # Rising Edge of SCL after Reset | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | … | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | Update Code | | | | Register Address(1) | | | Register Content (16-bit) | | | | | Reset |
| Content | 1 | 0 | 0 | 1 | **0** | **0** | **X** | MSB | | | | LSB | 0 |

(1) Register address 000 for Configuration_0 register
Register address 001 for Configuration_1 register

A correct sequence must have 24 SCLK, where:

- The first 4 SCLK are for detection of a correct code (must be 1001).
- The next 3 SCLK will indicate the register to be written (000 or 001).
- The next 16 SCLK will pass the data information (from MSB to LSB).
- Finally the last SCLK will pass the bit “0” that is used to separate words.

To signalize the end of the INTERFACE MODE, the device transmit a specific word in the last PP:

- LVDS : 00 00 00 00 00 00 00 01 01 01 01 01

## 7.5 Sensor Programming

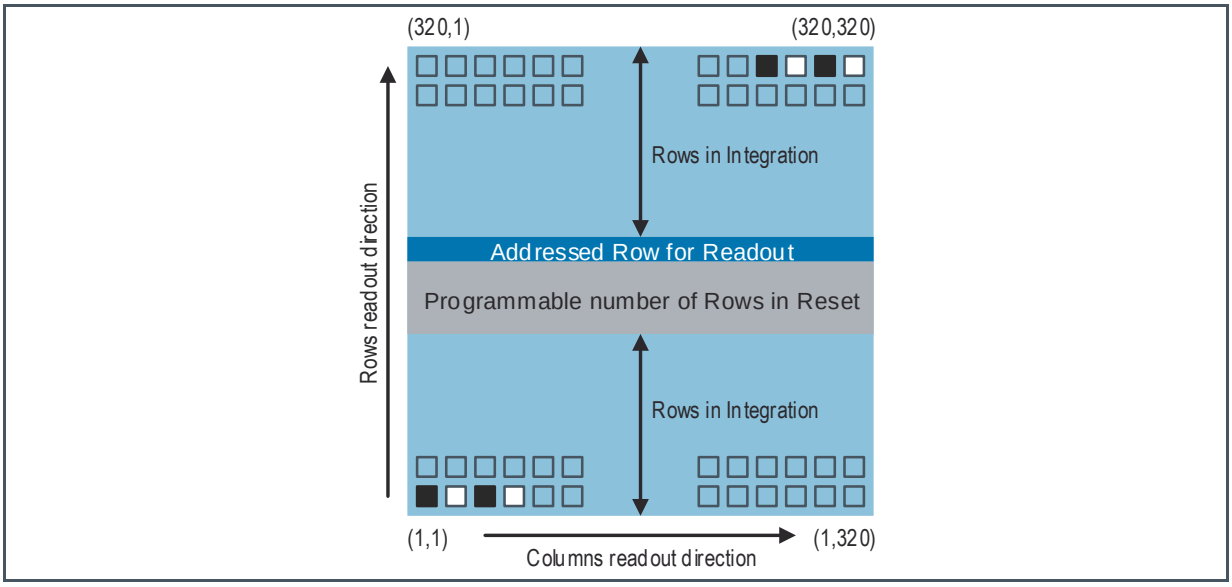
This section explains how the NanEyeM can be programmed using the on-board registers.

### 7.5.1 Exposure Time Control

Exposure time is defined based on the amount of rows in reset set by user and the frame rate, which is dependent on the main clock frequency and the delay mode setting. The NanEyeM sensor features a rolling shutter, which means one row is selected for readout while a defined number of previous rows are in reset, and all the others rows are in integration.

Configuring the DELAY MODE at the beginning of each frame, can be used to increase the integration time.

**Figure 27:**
**Row Readout Operation**




The frame time is defined by a full cycle in the state-machine including the matrix readout as well as the time between frames for INTERFACE, SYNC and DELAY MODE.

**Equation 1: Frame Time**

$$t_{frame} = t_{rows\_btw\_frame} + t_{rows\_matrix}$$

The effective exposure time thus is given by the formula:

### Equation 2: Exposure Time

$$t_{exp} = t_{rows\_btw\_frame} + t_{rows\_matrix} - t_{rows\_in\_reset} - t_{rows\_in\_readout}$$

$t_{exp}$ = The effective exposure time
$t_{rows\_btw\_frames}$ = Time for of rows between frames
$t_{rows\_matrix}$ = Time for active pixel matrix readout
$t_{rows\_in\_reset}$ = Time of rows in reset
$t_{rows\_in\_readout}$ = Time of rows in readout

### Equation 3: Time for Rows between Frame

$$t_{rows\_btw\_frame} = t_{rows\_spi} + t_{rows\_sync} + t_{rows\_delay}$$

$$t_{rows\_spi} = 648\ PP$$
$$t_{rows\_sync} = 2 * 328\ PP = 656\ PP$$
$$t_{rows\_delay} = (16 * rows\_delay[4:0] + 2) * 328\ PP$$

### Equation 4: Time for Active Pixel Matrix Readout

$$t_{rows\_matrix} = 320 * 328\ PP + 8\ PP = 104968\ PP$$

Determined by the size of the pixel matrix with 328 PP per each row.

### Equation 5: Time for Rows in Reset

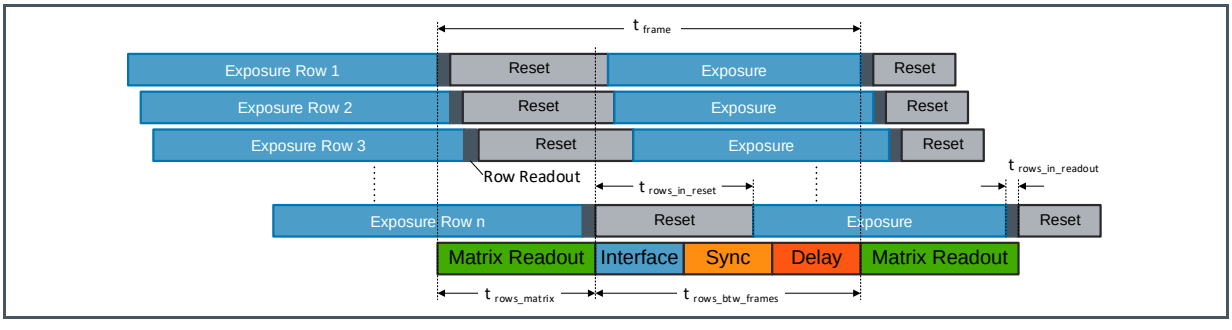
$$t_{rows\_in\_reset} = (2 * rows\_in\_reset[7:0] + 2) * 328\ PP$$

rows_in_reset[7:0] maximum value is equal to the total number of sensor rows.

### Equation 6: Time for Row in Readout

$$Trow_{in\_readout} = 2 * 328\ PP = 656\ PP$$

### Figure 28:
### Row Readout Timing Diagram



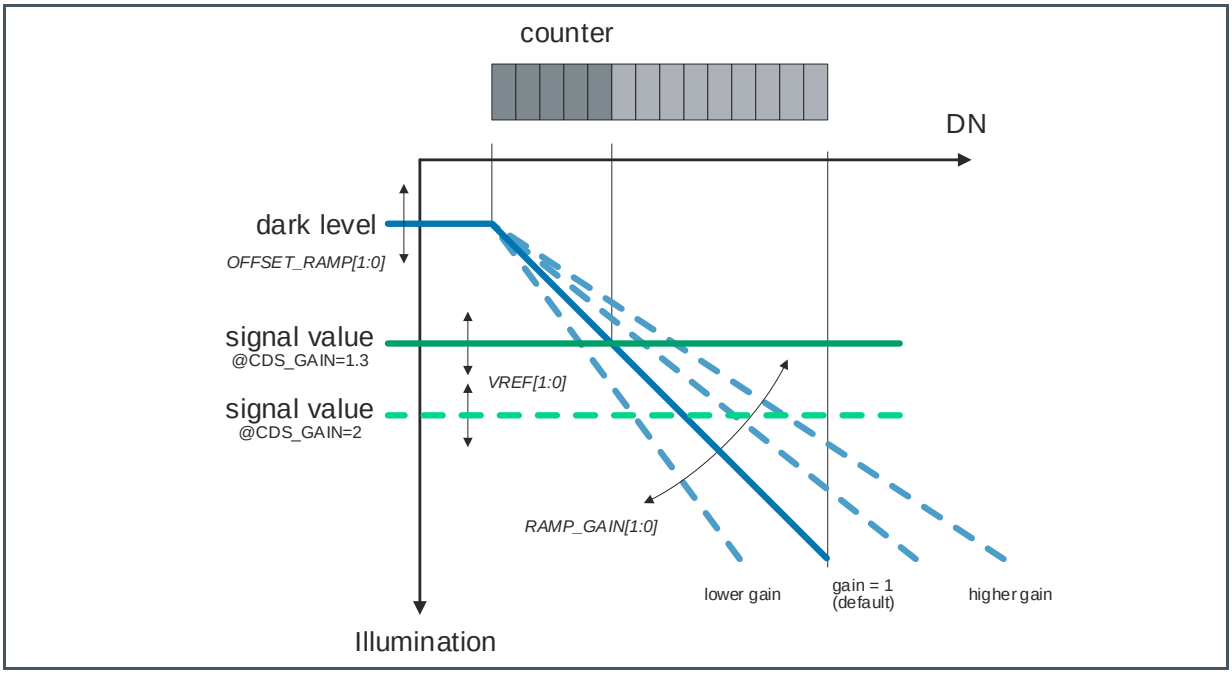
### 7.5.2 Offset and Analog Gain

It is a 10-bit full linear ADC. The architecture of the ADC allows programming several parameter:

- Voltage Reference for signal (vref[1:0])
- Ramp Gain (ramp_gain[1:0])
- Ramp Offset Voltage (offset_ramp[1:0])
- CDS gain (cds_gain[0])
- CDS current (bias_curr_increase[0])

See the configurable values in 8 Register Description.

**Figure 29 :**
**ADC Settings**



# 8 Register Description

## 8.1 Detailed Register Description

**Figure 30:**
**Configuration_0 Register**

| Addr: 00h | | Configuration_0 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 15:8 | rows_in_reset[7:0] | 80h | WO | Sets the number of rows in reset:<br>$rows_{in\_rst}$ = 2*rows_in_reset[7:0]+2<br>**Default: 258** |
| 7:6 | vrst_pix[1:0] | 10b | WO | Sets the pixel reset voltage:<br>0: 2.2 V<br>1: 2.4 V<br>**2: 2.6 V** (recommended)<br>3: 3.3 V |
| 5:4 | ramp_gain[1:0] | 01b | WO | Sets the analog ADC ramp gain:<br>See Figure 31. |
| 3:2 | offset_ramp[1:0] | 01b | WO | Sets the ramp offset (dark level) value<br>0: 1.9 V<br>**1: 2 V**<br>2: 2.1 V<br>3: 2.2 V (recommended) |
| 1:0 | output_curr[7:0] | 01b | WO | Sets the LVDS output current<br>0: 600 µA / 3.9 mA<br>**1: 1200 µA / 5.8 mA**<br>2: 1800 µA / 7.7 mA<br>3: 2000 µA / 9.6 mA |

**Figure 31:**
**ADC Ramp Gain Settings**

| MCLK [MHz] | ramp_gain[1:0] | Ramp Gain | MCLK [MHz] | ramp_gain[1:0] | Ramp Gain |
|---|---|---|---|---|---|
| 12 | 00 | 0.79 | 16 | 00 | 0.79 |
| | 01 | 0.99 | | 01 | 0.99 |
| | 10 | 1.32 | | 10 | 1.32 |
| | 11 | 1.97 | | 11 | 1.97 |
| **25** | 00 | 0.80 | 31 | 00 | 0.81 |
| | **01** | **1.00** | | 01 | 1.01 |
| | 10 | 1.33 | | 10 | 1.35 |
| | 11 | 2.00 | | 11 | 2.03 |
| 49 | 00 | 0.83 | 63 | 00 | 0.83 |
| | 01 | 1.03 | | 01 | 1.04 |
| | 10 | 1.38 | | 10 | 1.39 |
| | 11 | 2.07 | | 11 | 2.10 |

**Figure 32:**
**Configuration_1 Register**

| Addr: 01h | | Configuration_1 | | |
|---|---|---|---|---|
| **Bit** | **Bit Name** | **Default** | **Access** | **Bit Description** |
| 15:11 | rows_delay[4:0] | 00h | WO | Sets the number of rows period in delay mode<br>$rows_{delay}$ = 16*_rows_delay[4:0]_+2<br>**Default: 2** |
| 10 | bias_curr_increase[0] | 0b | WO | **0: Nominal bias current**<br>1: ~2x bias current, reduces settling time for high speed applications |
| 9 | cds_gain[0] | 1b | WO | 0: CDS gain 1.3 (recommended)<br>**1: CDS gain 2** |
| 8 | output_mode[0] | 1b | WO | 0: Do not use<br>**1: LVDS** |
| 7:6 | mclk_mode[1:0] | 01b | WO | Sets main clock frequency: See Figure 33<br>0: Main clock 2x<br>**1: Default**<br>2: Main clock /2<br>3: Main clock /2 |
| 5:4 | vref[1:0] | 01b | WO | Sets the reference voltage for CDS:<br>0: 1.9 V<br>**1: 2 V**<br>2: 2.1 V (recommendet)<br>3: 2.2 V |
| 3:2 | cvc_curr[1:0] | 10b | WO | Sets the CVC current:<br>See Figure 34.<br>Recommended to set to 01b. |
| 1 | idle_mode[0] | 1b | WO | Sets the sensor to work in idle mode with lower power consumption<br>0: Idle mode disabled<br>**1: Idle mode enabled** |
| 0 | high_speed[0] | 0b | WO | Sets clock to high speed mode: See Figure 33. **0: MCLK high speed mode off**<br>1: MCLK high speed mode enabled |

**Figure 33:**
**Main Clock Configurations & Frame Rates**

| high_speed[0] | mclk_mode[1:0] | Description | Interface Speed MCLK [MHz] | Frame Rate [fps] |
|---|---|---|---|---|
| **0** | 00 | Main clock 2x | 49.1 | 38 |
| | **01** | **Default** | **24.7** | **19** |
| | 1x | Main clock /2 | 12.3 | 9 |
| 1 | 00 | Main clock 2x | 62.6 | 49 |
| | 01 | Default HS | 31.1 | 24 |
| | 1x | Main clock /2 | 15.7 | 12 |

**Figure 34:**
**CVC Current Settings**

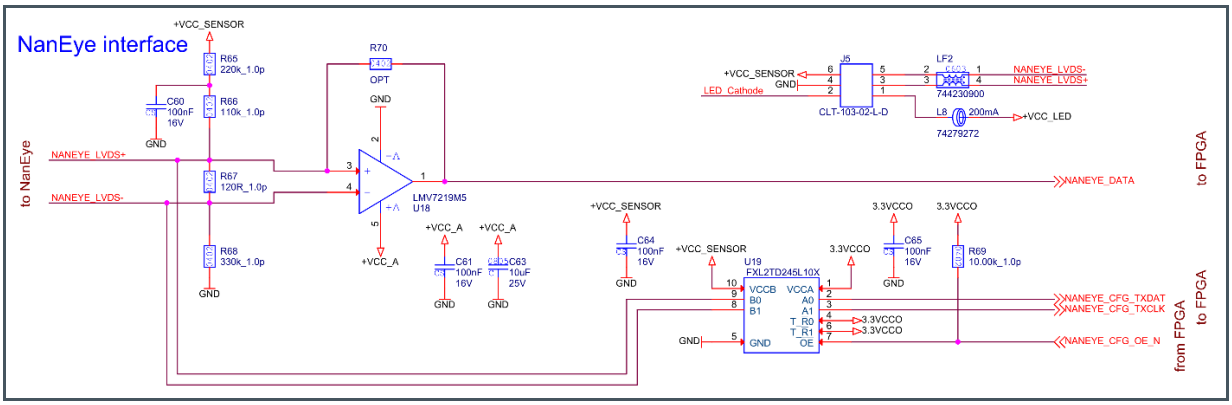
| MCLK [MHz] | CVC_CURR[1:0] | CVC Current [µA) | MCLK [MHz] | CVC_CURR[1:0] | CVC Current [µA) |
|---|---|---|---|---|---|
| 12 | 00 | 0.36 | 16 | 00 | 0.46 |
| | 01 | 0.79 | | 01 | 1..03 |
| | 10 | 0.98 | | 10 | 1.29 |
| | 11 | 1.44 | | 11 | 1.88 |
| **25** | 00 | 0.69 | 31 | 00 | 0.90 |
| | 01 | 1.58 | | 01 | 2.05 |
| | **10** | **1.98** | | 10 | 2.59 |
| | 11 | 2.93 | | 11 | 3.85 |
| 49 | 00 | 1.54 | 63 | 00 | 1.75 |
| | 01 | 3.18 | | 01 | 4.14 |
| | 10 | 4.06 | | 10 | 5.30 |
| | 11 | 6.07 | | 11 | 7.95 |

# 9 Application Information

## 9.1 Recommended LVDS Receiver Electronics

The direct interface of the LVDS data to an FPGA or DSP differential input is not guaranteed. It is recommended to use a LVDS detections circuit based on a fast comparator, which fixes the LVDS signals common mode.

**Figure 35:**
**NanEye Interface Schematic (for information only)**




In order to increase the robustness of the de-serialization under the presence of significant jitter, which should be expected from the on chip oscillator, the data is EXOR combined with the data clock.

To reliably de serialize the incoming data, the receiver side should sample the data at least with 750 MHz ( > 10x of the MCLK frequency) to properly detect the phase of the transitions.

When defining the drive strength of the up stream drivers in the proximal circuitry it has to be considered that the serial clock and the serial data will couple to each other over the bit lines termination resistor. To reduce noise coupling to the analog electronics the LVDS output current is configured between 600 µA to 2 mA (by serial interface), which will guarantee a save detection and de-serialization based on very low voltage swing LVDS receiver.

Driving the serial configuration data should be carefully designed along with the cables inductance to avoid signal over shoot at the chip side. It is recommended to use slew rate controlled drivers with a low slew rate. No distal termination of the data lines is implemented on chip.

## 9.2 Supply Generation

Having an LDO to generate a dedicated low noise supply is recommended. It has to be kept in mind that the cable has about 7 Ω per meter length. So for different cable length and clock speeds used it should be verified that the supply voltage at the sensor is within the required range.

## 9.3 External Components

**Figure 36:**
**External Components LVDS**

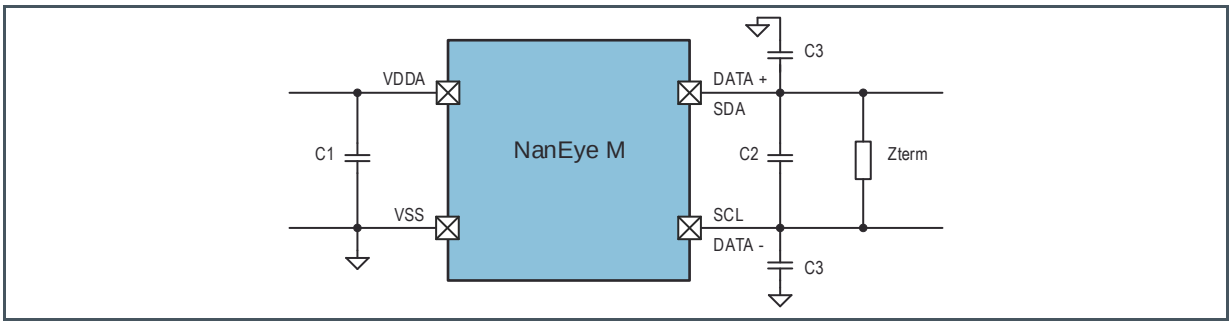
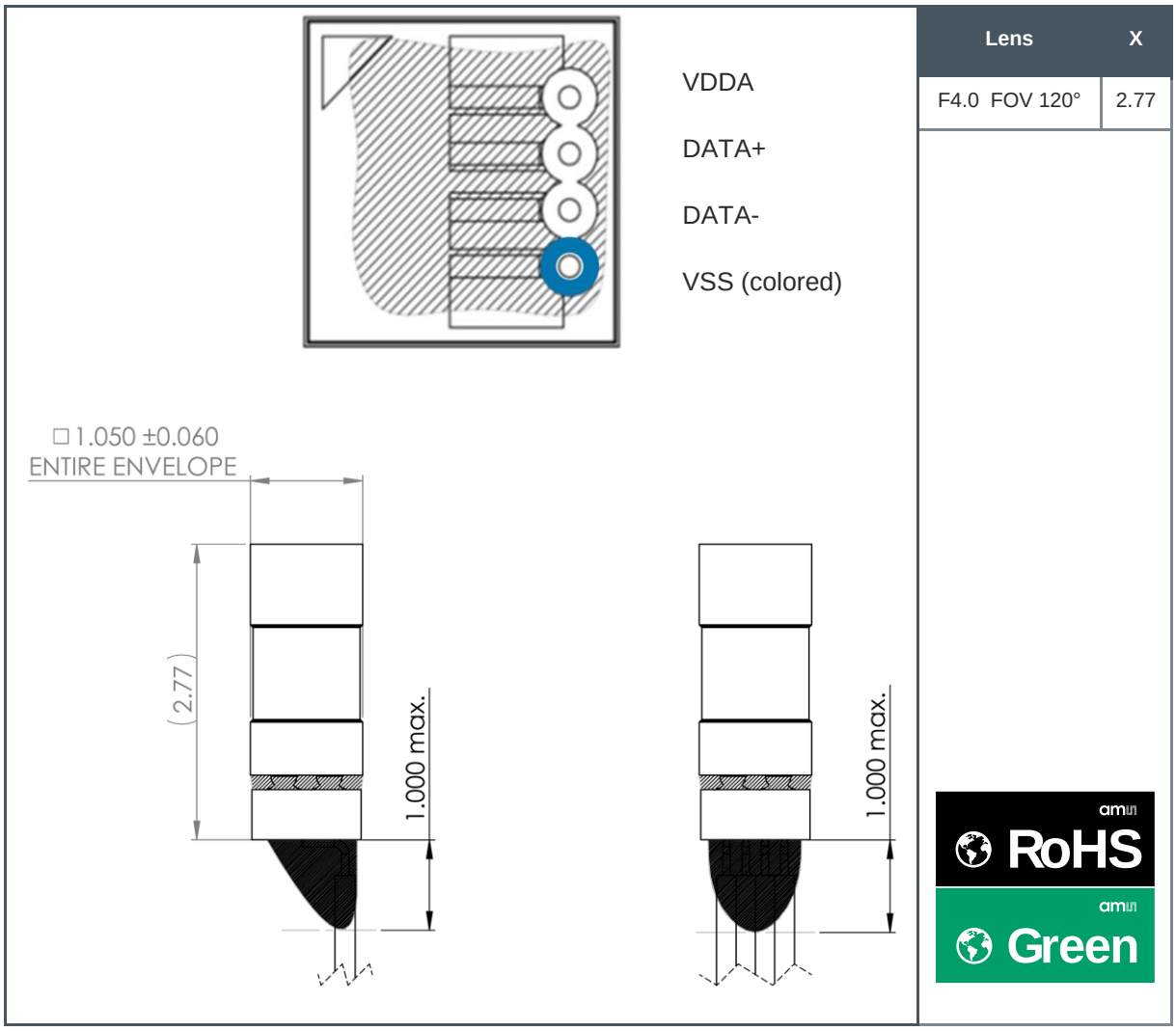



**Figure 37:**
**External Components Recommendations**

| Component | Description | Nominal Value | Unit |
|---|---|---|---|
| C1 | Power supply decoupling | >100 | nF |
| C2 | Differential load on LVDS lines (parasitics) | <3 | pF |
| C3 | Single ended load on LVDS lines (parasitics) | <5 | pF |
| Zterm | Impedance of LVDS termination | 120 | Ω |

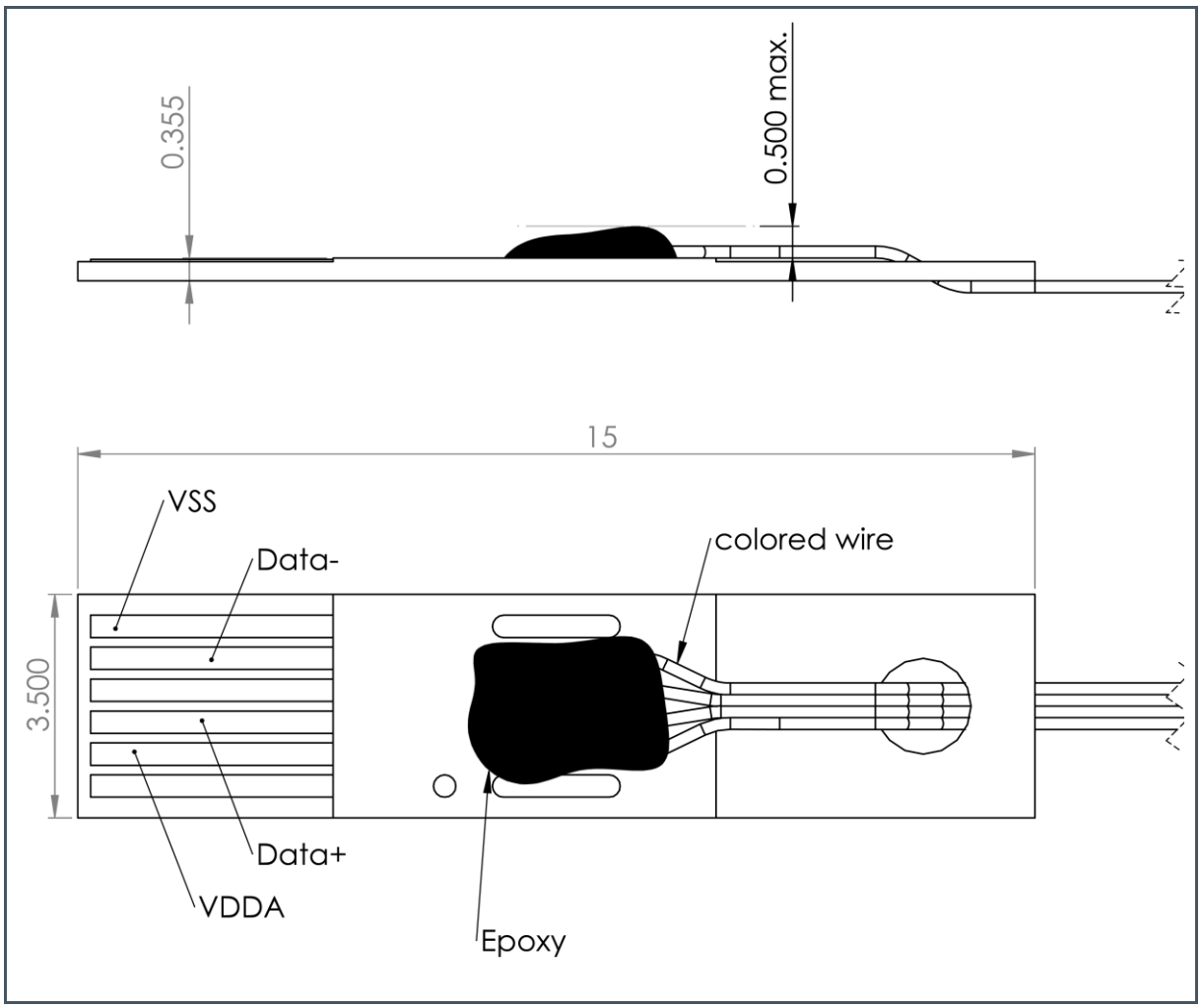
# 10 Package Drawings & Markings

**Figure 38:**
**NanEyeM with Lens and Cable Soldered (Bended) Package Outline Drawing**




(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

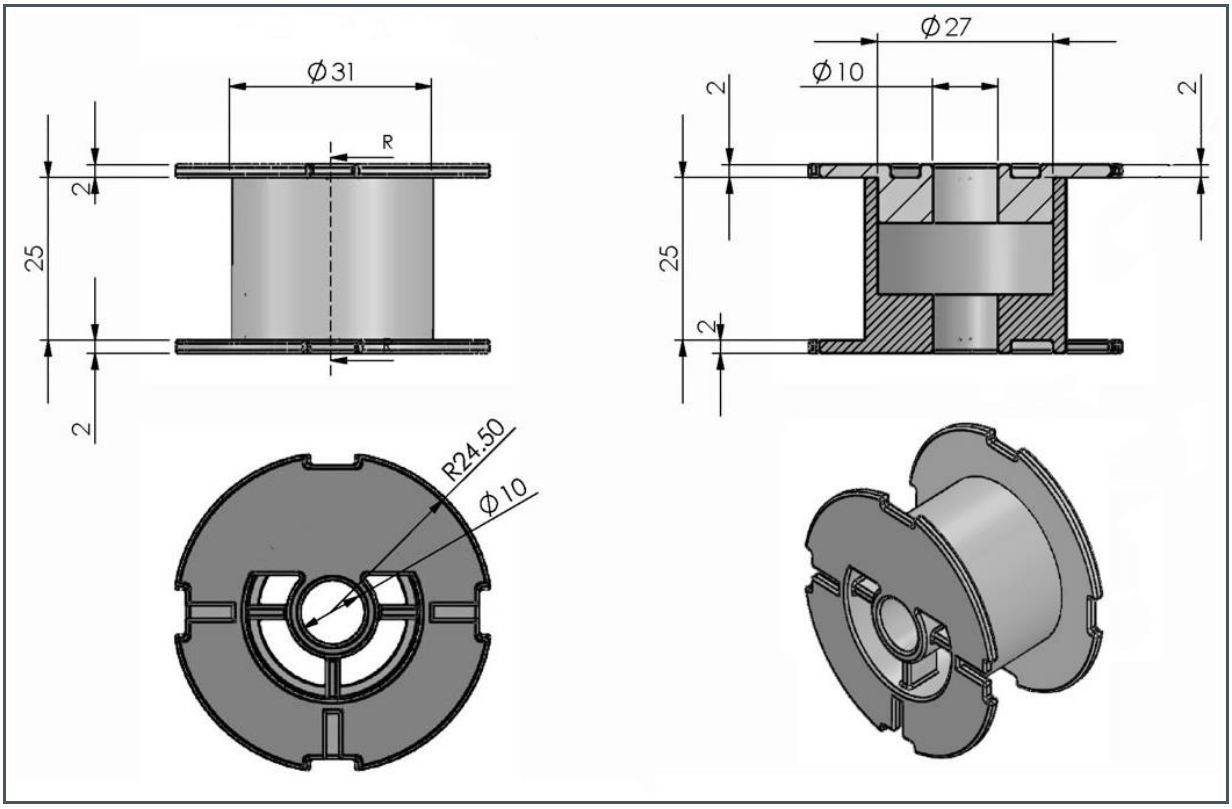
**Figure 39:**
**NanEye FlexPCB Connector**




(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

# 11 Tape & Reel Information

**Figure 40:**
**Spool Dimensions for Module plus Cable Shipments**




(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This drawing is subject to change without notice.

# 12 Appendix

## 12.1 Evaluation System

Optionally with the NanEyeM module, **ams** provides a base station and software to run the device on a PC in real-time with all necessary image corrections. The complete system consists of the module, the USB interface box and the PC software.

# 13 Revision Information

| Document Status | Product Status | Definition |
|---|---|---|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
| Preliminary Datasheet | Pre-Production | Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice |
| Datasheet | Production | Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade |
| Datasheet (discontinued) | Discontinued | Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs |

| Changes from previous version to current revision v2-00 | Page |
|---|---|
| Removed CONFIDENTIAL status | all |
| Changed fps range (including delay option) | 3,10 |
| Added new order codes | 5 |
| Removed 6-wire cable option | 6 |
| Added lens stack parameters | 10 |
| Added frame time definition | 17, 25 |
| Corrected cable orientation in package drawing | 34 |
| | |
| | |
| | |

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

# 14 Legal Information



**Headquarters**
ams AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

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