AS1323

1.6µA Quiescent Current, Single Cell, DC-DC Step-up Converter

General Description

The AS1323 high-efficiency step-up DC-DC converter was designed specifically for single-cell, battery-powered devices where lowest quiescent current and high efficiency are essential.

The compact device is available in three fixed-voltage variants with Vout of 2.7V, 3.0V, and 3.3V. It is perfect for a wide variety of applications where low quiescent currents and small form factors are critical.

Integrated boot circuitry ensures start-up even with very-high load currents.

The true output disconnect feature completely disconnects the output from the battery during shutdown.

The device is available in a TSOT23-5 pin package.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS1323, 1.6µA Quiescent Current, Single Cell, DC-DC Step-up Converter are listed below:

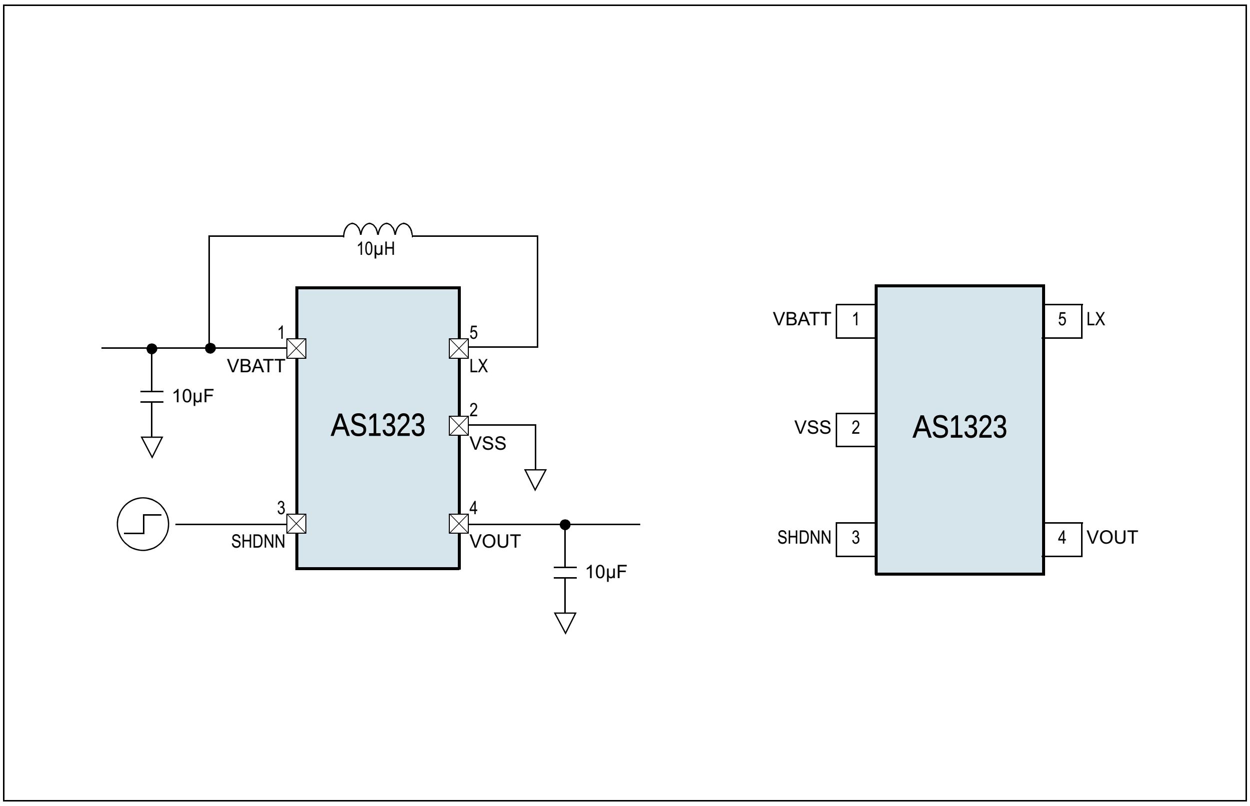
Figure 1:
Added Value of Using AS1323

Benefits	Features
Extended battery life	• 1.6µA Quiescent Current • Shutdown Current 0.1µA • Efficiency Up to 85%
Suitable to wide variety of applications	• Input Voltage Range: 0.75 to 2V • Fixed Output Voltages: 2.7, 3.0 and 3.3V • Output Voltage Accuracy: ±3% • Up to 100mA Output Current • Output Disconnect in Shutdown • Guaranteed 0.95V Start-Up Voltage
Enables cost effective PCB design	• No External Diode or FETs Needed • TSOT23-5 Package

Applications

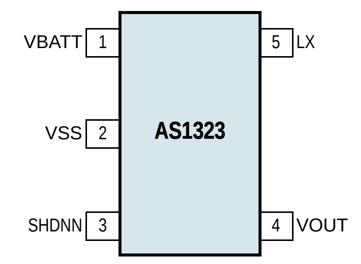
The devices are ideal for single-cell portable devices including mobile phones, MP3 players, PDAs, remote controls, personal medical devices, wireless transmitters and receivers, and any other battery-operated, portable device.

Figure 2:
Typical Operating Circuit



Pin Assignment

Figure 3:
Pin Diagram (Top View)



Pin Description

Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	VBATT	**Battery Supply Input and Coil Connection**
2	VSS	Negative Supply and Ground
3	SHDNN	**Shutdown Input**. 0 = Shutdown mode. 1 = Normal operating mode.
4	VOUT	**Output**. This pin also supplies bootstrap power to the device.
5	LX	**Inductor Connection**. This pin is connected to the internal N-channel MOSFET switch drain and P-channel synchronous rectifier drain.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VBATT, SHDNN, LX to VSS	-0.3	+5	V	
Maximum Current VOUT, LX		1	A	
Thermal Resistance Θ_{JA}		207.4	ºC/W	on PCB
Electro-Static Discharge	±2		kV	HBM
Operating Temperature Range	-40	85	ºC	
Storage Temperature Range	-65	150	ºC	
Junction Temperature		150	ºC	
Package Body Temperature		260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative Humidity non-condensing RH_{NC}	5	85	%	
Moisture Sensitivity Level MSL	1			

Electrical Characteristics

DC Electrical Characteristics

TAMB = -40°C to 85°C, VBATT = 1.2V, VOUT = $VOUT_{(NOM)}$, SHDNN = VOUT, RLOAD = ∞, unless otherwise noted. Typical values are at TA = 25°C.(unless otherwise specified). Limits are 100% production tested at TAMB = 25ºC. Limits over the operating temperature range are guaranteed by design.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN_{MIN}	Minimum Input Voltage			0.75		V
VIN	Operating Input Voltage	TAMB = 25ºC	0.95		2	V
VIN_{SU}	Minimum Start-Up Input Voltage	TAMB = 25ºC, RLOAD = 100Ω		0.75	0.95	V
VOUT	Output Voltage	AS1323-27	2.619	2.7	2.781	V
		AS1323-30	2.91	3.0	3.09	
		AS1323-33	3.201	3.3	3.399	
RLOAD	Load depended drop of VOUT	VBATT = 1.5V; I_{LOAD} = 45mA		30	40	mV
RDS-ON	N-Channel ON-Resistance			0.5	1.0	Ω
	P-Channel ON-Resistance			0.75	1.5	Ω
ILIMIT	N-Channel Switch Current Limit	Programmed at 400mA		400		mA
tON	Switch Maximum ON-Time			6		µs
	Synchronous Rectifier Zero-Crossing Current			10		mA
IOP-OUT	Operating Current into VBATT	VBATT = 1.5V, VOUT = 3.3V, TAMB = 25ºC		6		µA
IQ-OUT	Quiescent Current to VOUT			1.6	3	µA
IQ-BAT	Quiescent Current into VBATT	VBATT = 1.5V, TAMB = 25ºC		0.3	1	µA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ISDI-OUT [(1)]	Shutdown Current to VOUT				200	nA
ISDI-BAT	Shutdown Current into VBATT	VBATT = 1.5V, TAMB = 25ºC		100		nA
VIL	SHDNN Voltage Threshold, Low		150			mV
VIH	SHDNN Voltage Threshold, High				900	mV
ISDI	SHDNN Input Bias Current	TAMB = 25ºC, VSDI = VOUT		100	300	nA

Note(s) and/or Footnote(s):

1. VOUT is completely disconnected (0V) during shutdown.
2. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Typical Operating Characteristics

VOUT= 3.3V; TA = 25 °C; CIN = COUT = 10µF, L = 10µH, ILOAD = 10mA; VBATT = 1.5V; unless otherwise specified.

Figure 7:
Efficiency vs. Output Current; VOUT = 3.3V

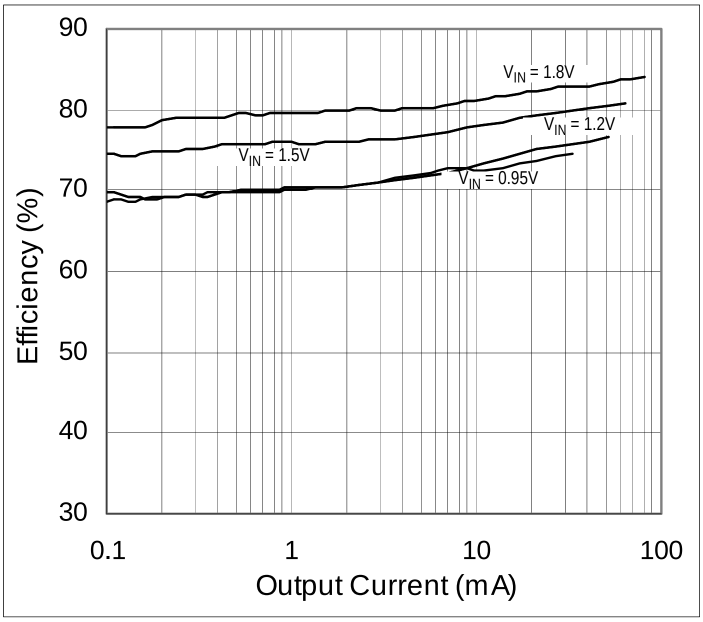


Figure 8:
Efficiency vs. Output Current; VOUT = 3.0V

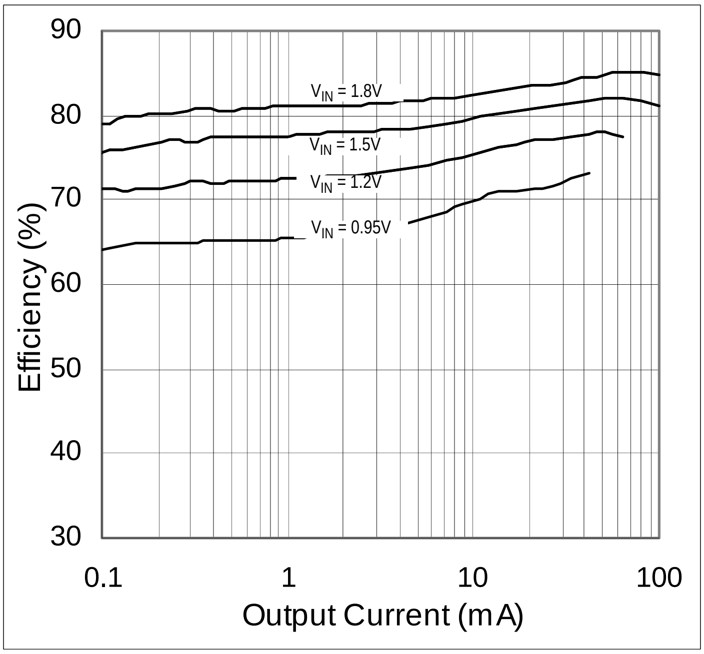


Figure 9:
Efficiency vs. Output Current; VOUT = 2.7V

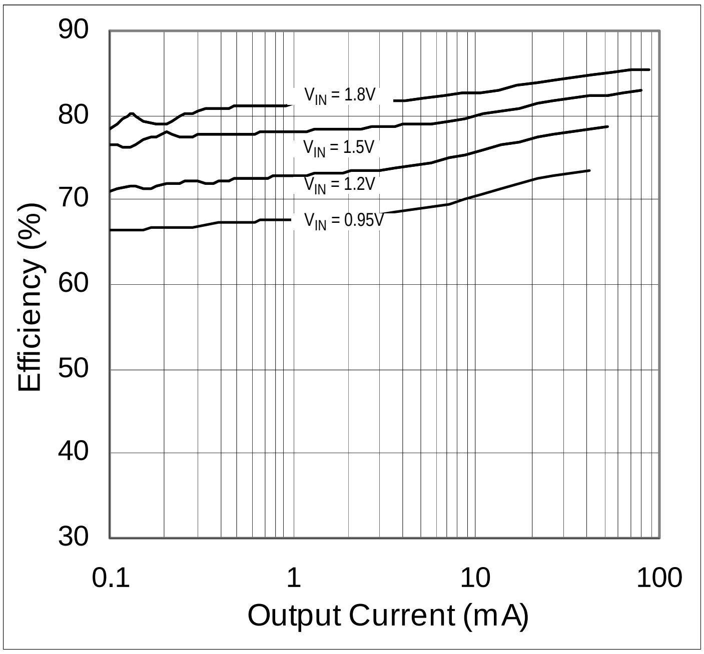


Figure 10:
Efficiency vs. Input Voltage

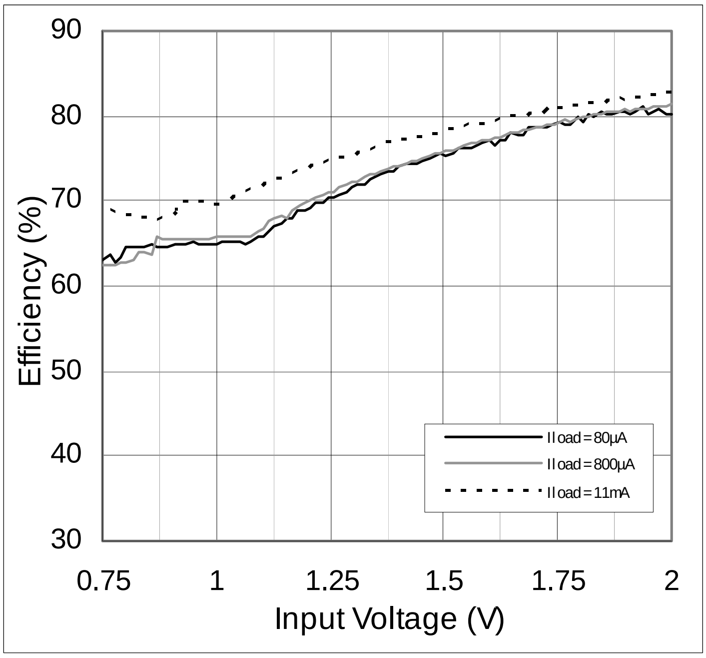


Figure 11:
Output Voltage vs. Temperature

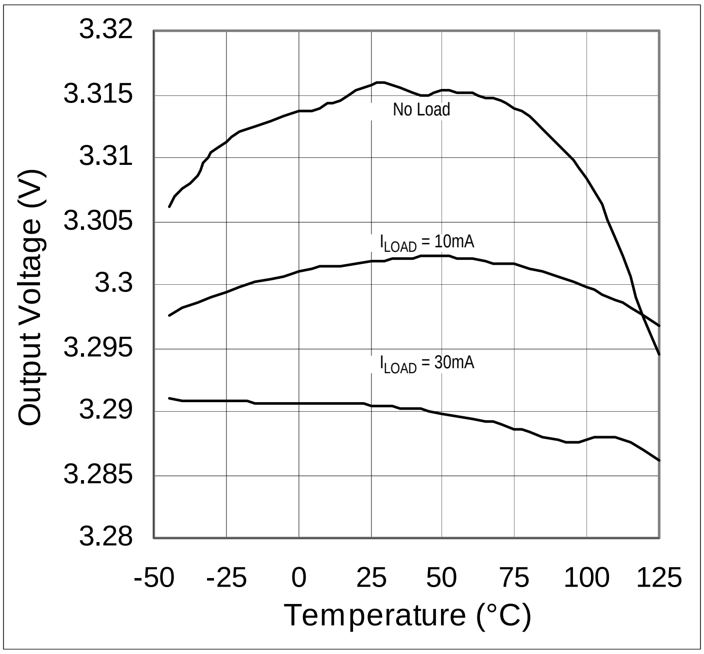


Figure 12:
Output Voltage vs. Output Current

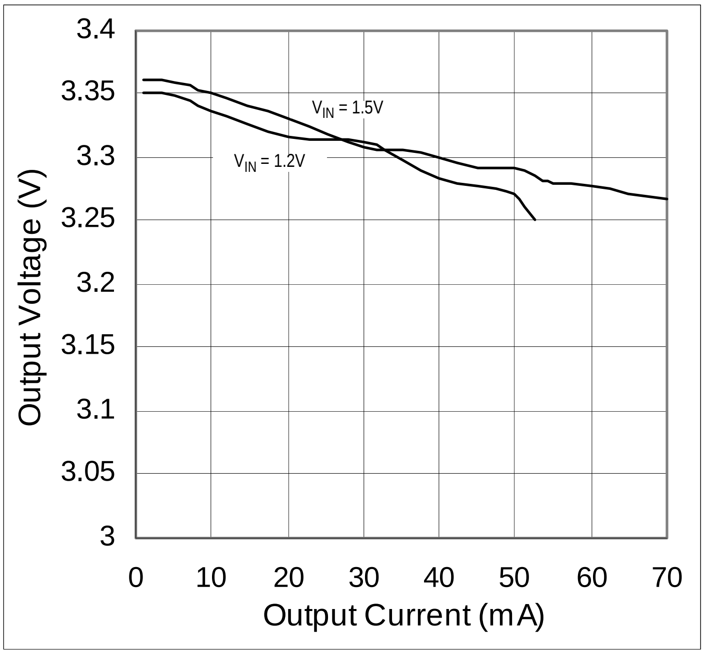


Figure 13:
Output Voltage vs. Input Voltage

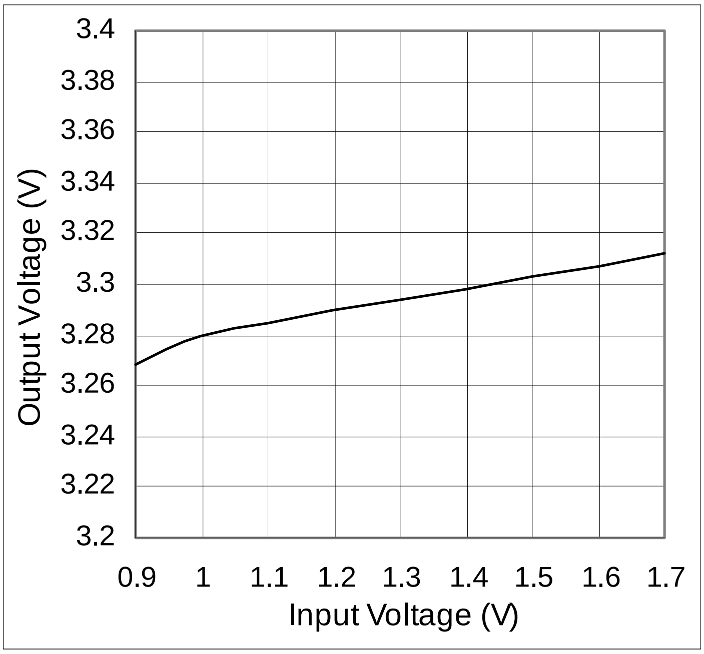


Figure 14:
Shutdown Current vs. Temperature

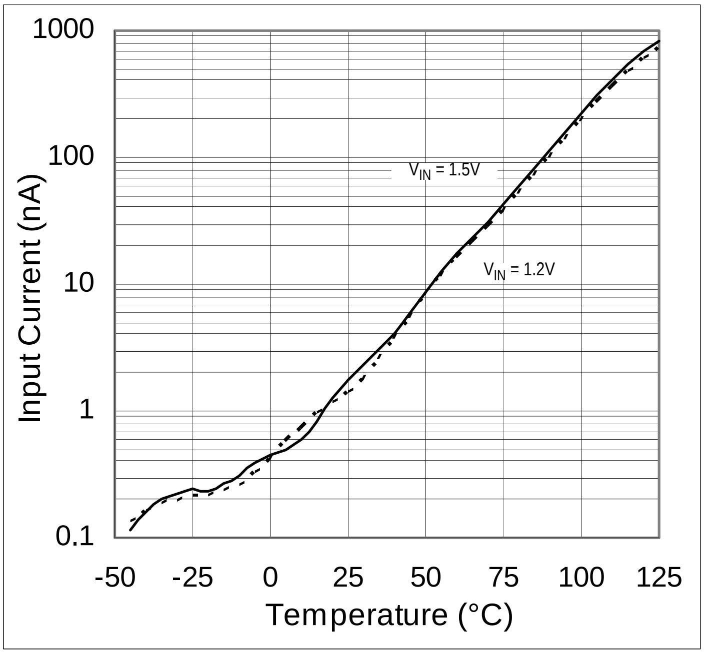


Figure 15:
Minimum Input Startup Voltage vs. Temperature

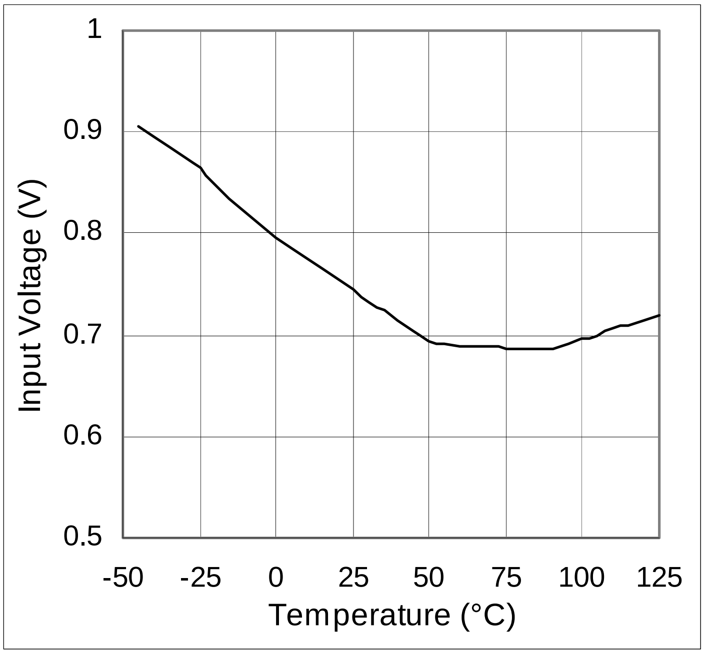


Figure 16:
Output Voltage vs. Input Voltage; VOUT = 2.7V

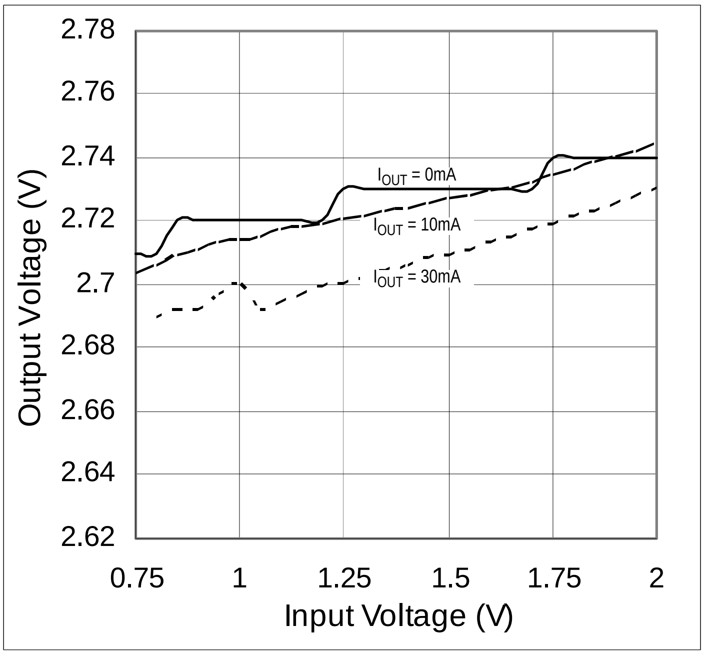


Figure 17:
Output Voltage vs. Input Voltage; VOUT = 3.0V

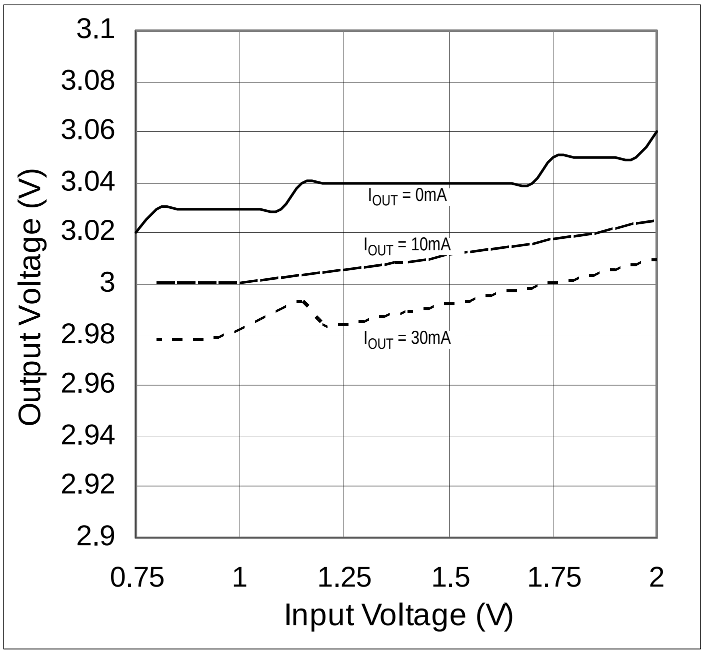


Figure 18:
Output Voltage vs. Input Voltage; VOUT = 3.3V

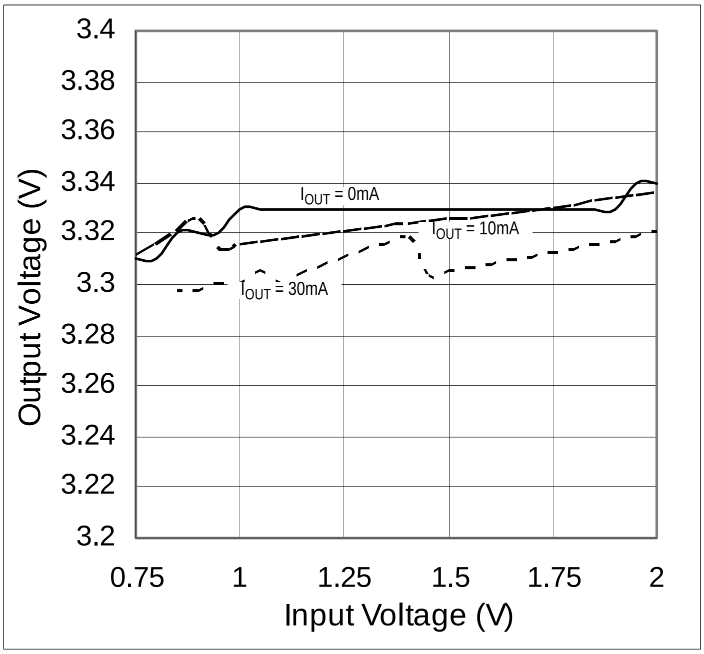


Figure 19:
Output Current vs. Input Voltage

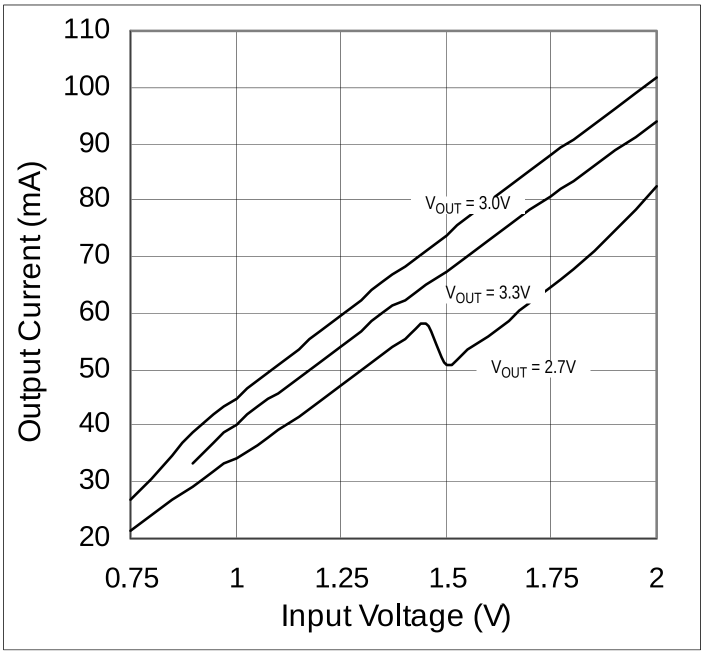


Figure 20:
SHDNN Threshold vs. Input Voltage

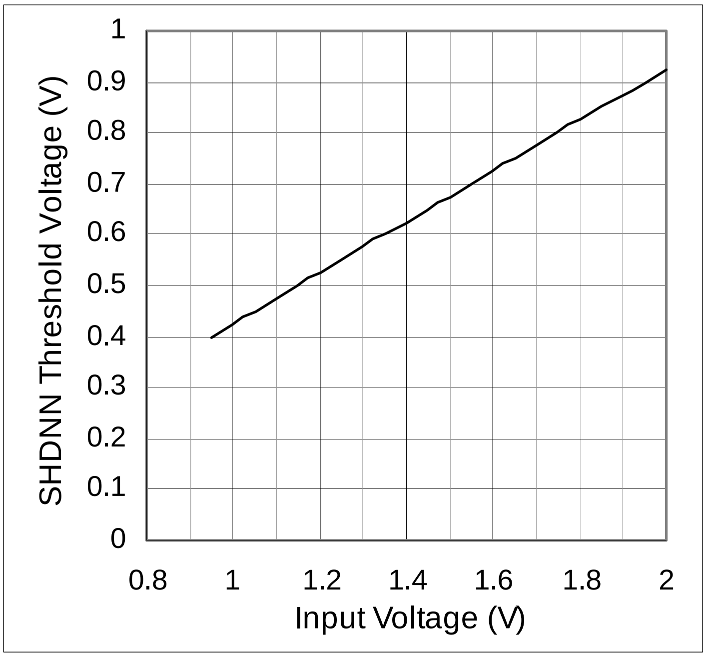


Figure 21:
Switching Waveform; VOUT = 2.7V

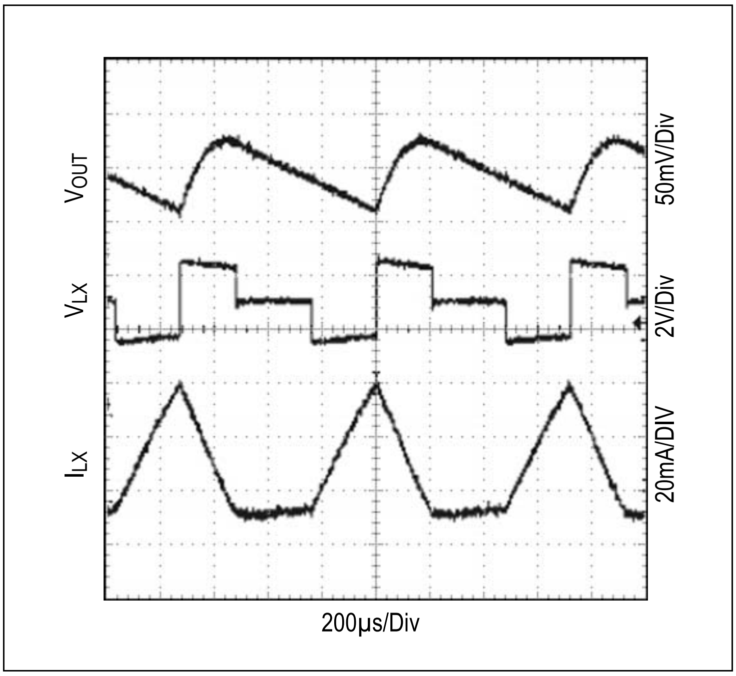


Figure 22:
Switching Waveform; VOUT = 3.0V

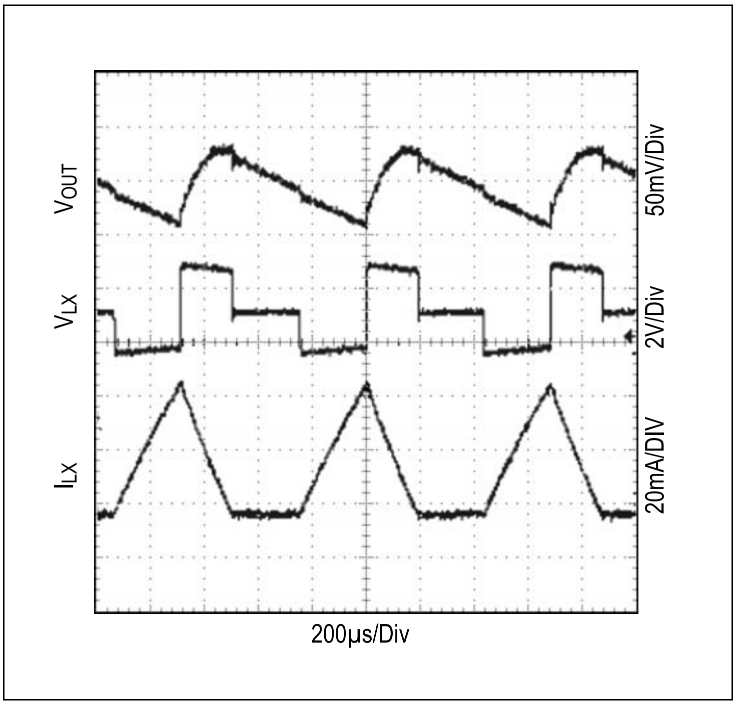
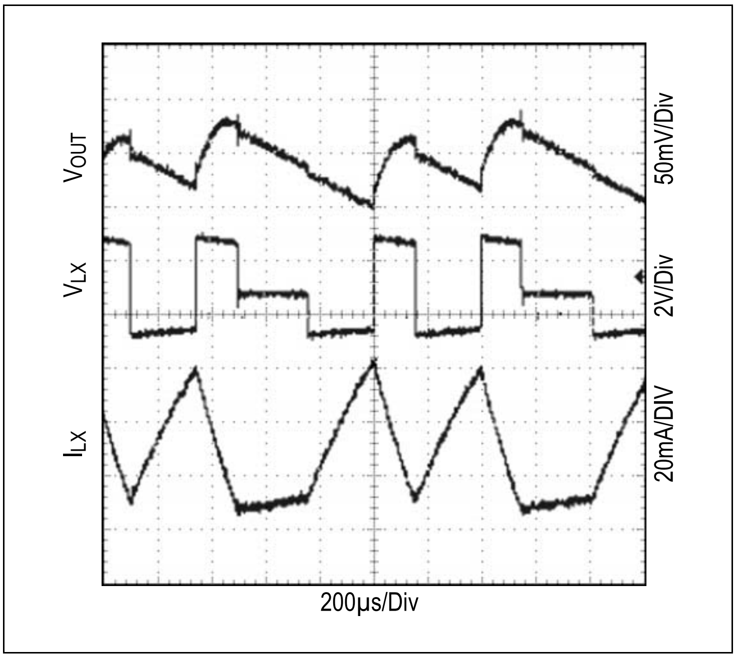


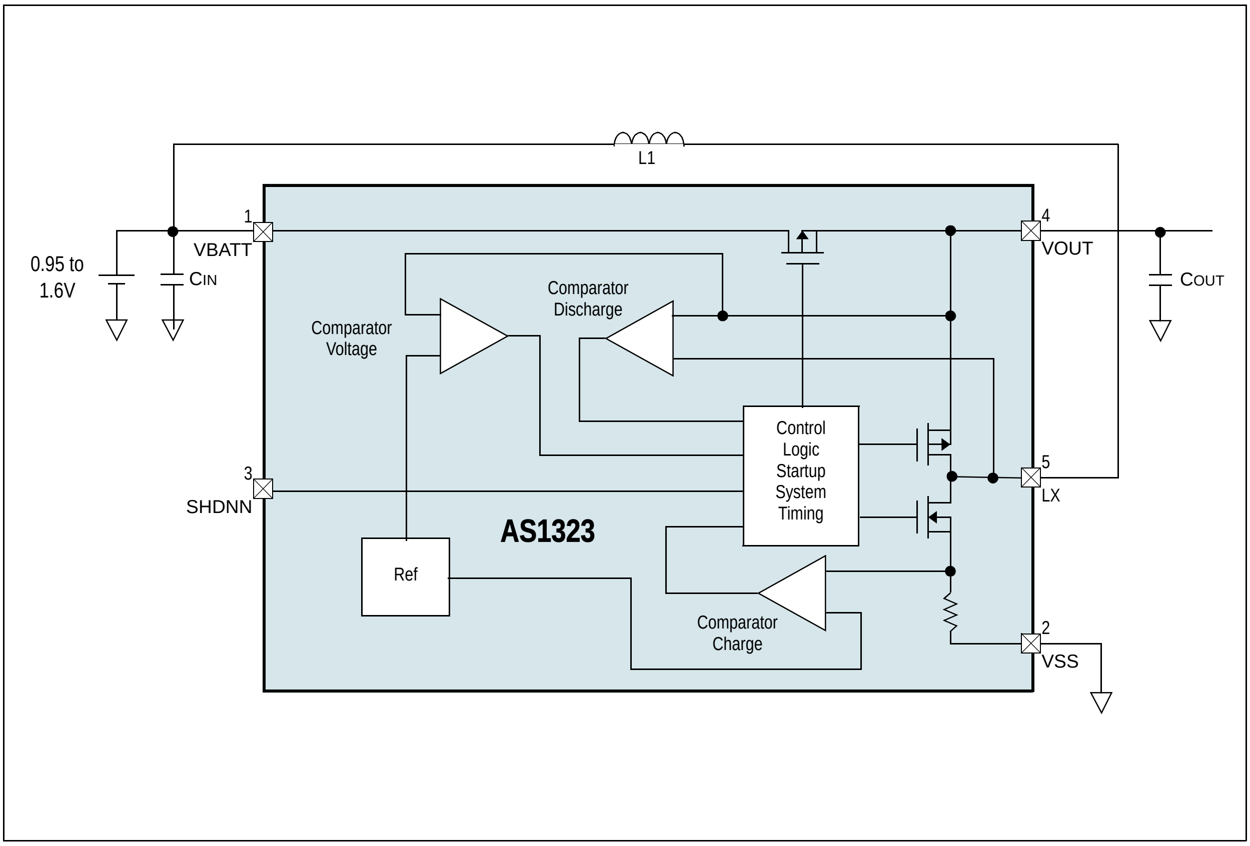
Figure 23:
Switching Waveform; VOUT = 3.3V



Detailed Description

The AS1323 is a compact, high-efficiency, step-up DC-DC converter guaranteed to start up with voltages as low as 0.95V, and operate with an input voltage down to 0.75V. Consuming only 1.6µA of quiescent current, the device includes an integrated synchronous rectifier that eliminates the need for an external diode and improves overall efficiency by minimizing losses (see Synchronous Rectification). The AS1323 also features an active-low shutdown circuit that supply current to 0.1µA.

Figure 24:
AS1323 Block Diagram



PFM Control

A forced discontinuous, current-limited, pulse-frequency modulation (PFM) control scheme provides ultra-low quiescent current and high efficiency over a wide output current-range. Rather than using an integrated oscillator, the inductor current is limited by the 400mA N-channel current limit or by the 6µs switch maximum ON-time. After each device-ON cycle, the inductor current must ramp to zero before another cycle can start. When the error comparator senses that the output has fallen below the regulation threshold, another cycle can begin.

Synchronous Rectification

The integrated synchronous rectifier eliminates the need for an external Schottky diode, reducing cost and PCB space. During normal operation, while the inductor discharges, the P-channel MOSFET turns on and shunts the MOSFET body diode. Consequently the rectifier voltage drop is significantly reduced improving efficiency without the need for external components.

Low-Voltage Startup Circuit

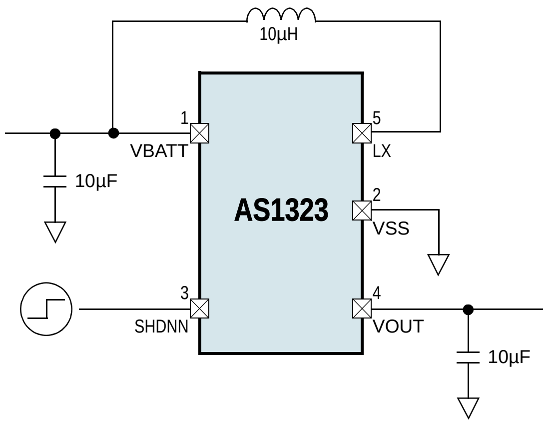
The AS1323 contains a unique low-voltage startup circuit which ensures start-up even with very high load currents. The minimum start-up voltage is independent of the load current. This device is powered from pin VBATT, guaranteeing startup at input voltages as low as 0.95V.

Shutdown

The AS1323 enter shutdown when the SHDNN pin is driven low. During shutdown, the output is completely disconnected from the battery. Shutdown can be pulled as high as 3.6V, regardless of the voltage at pins VBATT or VOUT. For normal operation, connect SHDNN to the input.

Application Information

Figure 25:
Typical Application Diagram



Inductor Selection

The control scheme of the AS1323 allows for a wide range if inductor values. A 10µH inductor should be sufficient for most applications (see Figure 25).

Smaller inductance values typically offer smaller physical size for a given series resistance, allowing the smallest overall circuit dimensions. Applications using larger inductance values may startup at lower battery voltages, provide higher efficiency and exhibit less ripple, but they may reduce the maximum output current. This occurs when the inductance is sufficiently large to prevent the maximum current limit (ILIMIT) from being reached before the maximum ON-time (t_{ON}) expires (see Figure 6).

For maximum output current, the inductor value should be chosen such that the controller reaches the current-limit before the maximum ON-time is triggered:

(EQ1) $$L > \frac{V_{BATT} \cdot t_{ON}}{I_{LIMIT}}$$

t_{ONMAX} is 6µs (typ)
ILIMIT is 400mA (typ)

For larger inductor values, the peak inductor current (IPEAK) can be determined by:

(EQ2) $$I_{PEAK} = \frac{V_{BATT} \cdot t_{ON}}{L}$$

The inductor's incremental saturation current rating should be greater than the peak switching current. However, it is generally advisable to bias the inductor into saturation by as much as 20%, although this will slightly reduce efficiency.

Maximum Output Current

The maximum output current (I_{OUTMAX}) is a function of IPEAK, VIN, VOUT, and the overall efficiency (η) as indicated in the formula for determining I_{OUTMAX}:

(EQ3) $$I_{OUTMAX} = \frac{1}{2} \cdot I_{PEAK} \cdot \left(\frac{V_{BATT}}{V_{OUT}}\right) \cdot \eta$$

Capacitor Selection

Choose input and output capacitors to supply the input and output peak currents with acceptable voltage ripple. The input filter capacitor (C_{IN}) reduces peak currents drawn from the battery and improves efficiency. Low equivalent series resistance (ESR) capacitors are recommended.

Note(s): Ceramic capacitors have the lowest ESR, but low ESR tantalum or polymer capacitors offer a good balance between cost and performance.

Output voltage ripple has two components: variations in the charge stored in the output capacitor with each COIL pulse, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

(EQ4) $$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

(EQ5) $$V_{RIPPLE(ESR)} = IPEAK\ R_{ESR(COUT}$$

(EQ6) $$V_{RIPPLE(C)} \approx \frac{1}{2} \cdot \left(\frac{L}{(V_{OUT} - V_{BATT}) \cdot C_{OUT}}\right) \cdot (I_{PEAK}^2 - I_{OUT}^2)$$

Where: IPEAK is the peak inductor current.

For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. For example, a 10µF ceramic capacitor and a 10µH inductor typically provide 75mV of output ripple when stepping up from 1.2V to 3.3V at 50mA. Low input-to-output voltage differences require higher output capacitor values.

Capacitance and ESR variation of temperature should be considered for best performance in applications with wide operating temperature ranges.

PC Board Layout Considerations

The AS1323 has been specially designed to be tolerant to PC board parasitic inductances and resistances. However, to achieve maximum efficiency a careful PC board layout and component selection is vital.

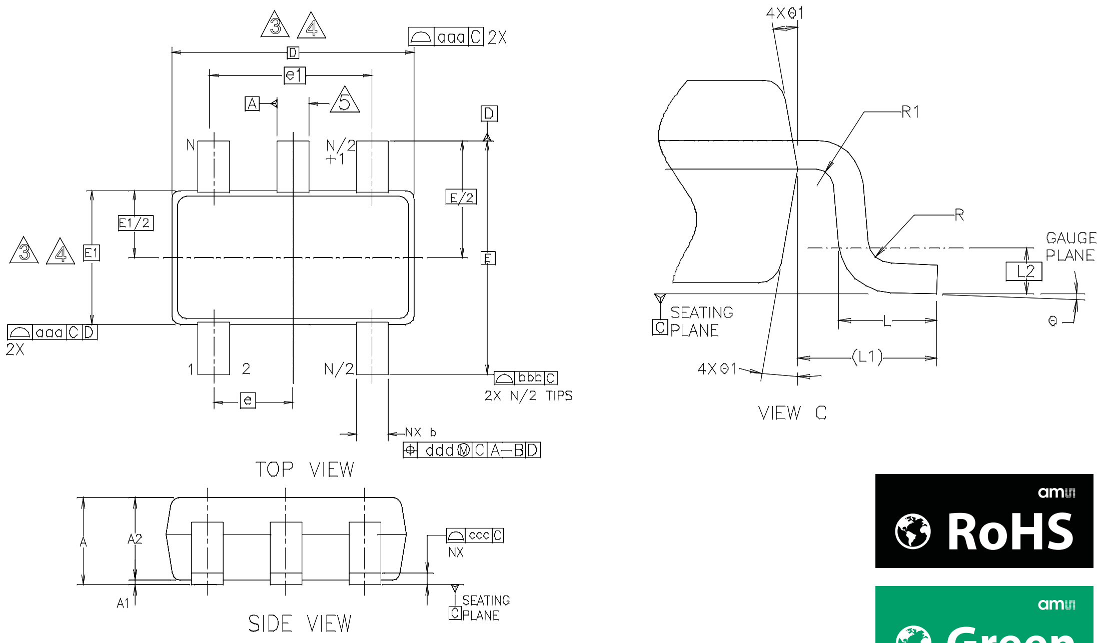
Note(s): For the optimal performance, the IC's VSS and the ground leads of the input and output capacitors must be kept less than 5mm apart using a ground plane. In addition, keep all connections to COIL as short as possible.

The system robustness guarantees a reliable operation even if those recommendations are not fully applied.

Package Drawings & Markings

The device is available in an TSOT23-5 package.

Figure 26:
TSOT23-5 Package



Symbol	Min	Typ	Max	Notes
A			1.00	
A1	0.01	0.05	0.10	
A2	0.84	0.87	0.90	
b	0.30		0.45	
b1	0.31	0.35	0.39	
c	0.12	0.15	0.20	
c1	0.08	0.13	0.16	
D		2.90BSC		3,4
E		2.80BSC		3,4
E1		1.60BSC		3,4
e		0.95BSC		
e1		1.90BSC		

Symbol	Min	Typ	Max	Notes
L	0.30	0.40	0.50	
L1		0.60REF		
L2		0.25BSC		
N		5		
R	0.10			
R1	0.10		0.25	
q	0º	4º	8º	
θ1	4º	10º	12º	
Tolerances of Form and Position				
aaa		0.15		
bbb		0.25		
ccc		0.10		
ddd		0.20		

Note(s) and/or Footnote(s):

1. Dimensions are in millimeters.
2. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15mm per side. Dimensions D and E1 are determined at datum H.
3. The package top can be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but include any mismatches between the top of the package body and the bottom. D and E1 are determined at datum H.

Figure 27:
AS1323 Marking

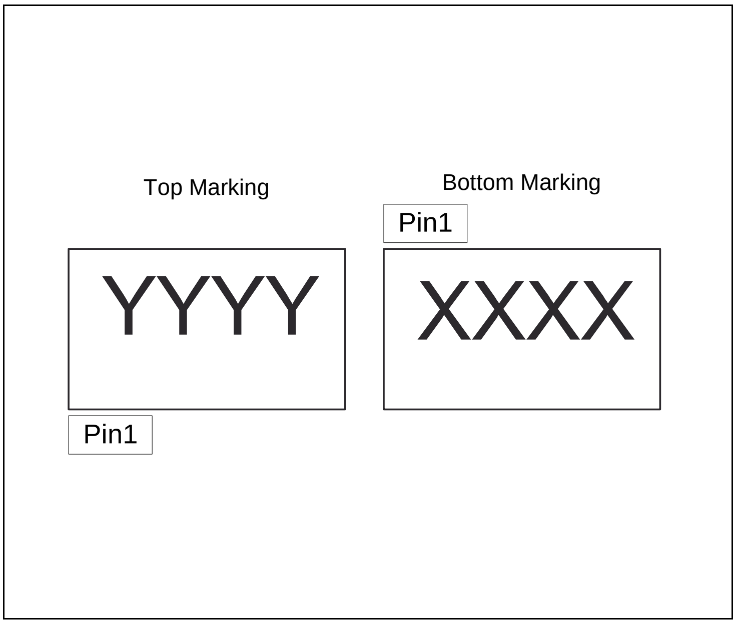


Figure 28:
Packaging Markings:

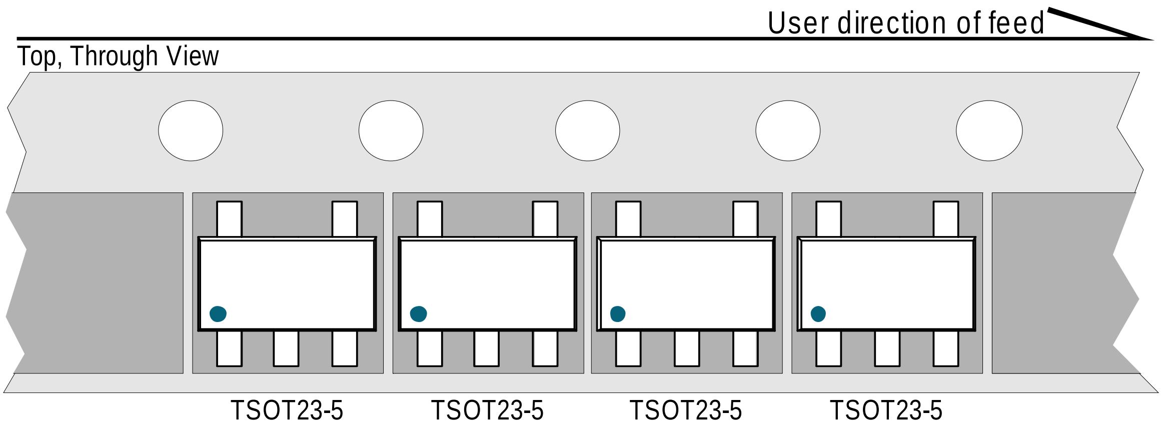
YYYY	XXXX
Marking code	Trace code

Note(s) and/or Footnote(s):

1. See Figure 30 for ordering codes of different AS1323 variants.

Tape and Reel Pin1 Orientation

Figure 29:
Tape & Reel Pin1 Orientation



Ordering & Contact Information

The device is available as the standard products shown in the figure below.

Figure 30:
Ordering Information

Ordering Code	Marking	Output	Description	Delivery Form	Package
AS1323-BTTT-27	ASJN	2.7V	1.6µA Quiescent Current, Single Cell, DC-DC Step-up Converter	Tape and Reel	TSOT23-5
AS1323-BTTT-30	ASMP	3.0V	1.6µA Quiescent Current, Single Cell, DC-DC Step-up Converter	Tape and Reel	TSOT23-5
AS1323-BTTT-33	ASMQ	3.3V	1.6µA Quiescent Current, Single Cell, DC-DC Step-up Converter	Tape and Reel	TSOT23-5

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.05 (2010-May) to current revision 1-11 (2014-Dec-16)	Page
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated General Description section	1
Updated Figure 5	4
Added Figure 20	13
Updated description of Inductor Selection	18
Updated Marking Information and Packaging Code	22

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide