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# FDMS2572

## N-Channel UltraFET Trench® MOSFET

150V, 27A, 47mΩ

### Features

- Max  $r_{DS(on)}$  = 47mΩ at  $V_{GS} = 10V$ ,  $I_D = 4.5A$
- Max  $r_{DS(on)}$  = 53mΩ at  $V_{GS} = 6V$ ,  $I_D = 4.5A$
- Low Miller Charge
- Optimized efficiency at high frequencies
- UIS Capability (Single pulse and Repetitive pulse)
- RoHS Compliant

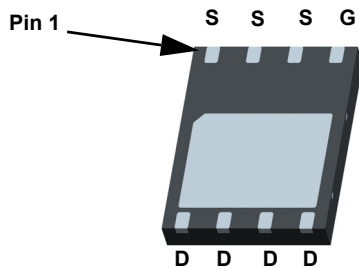


### General Description

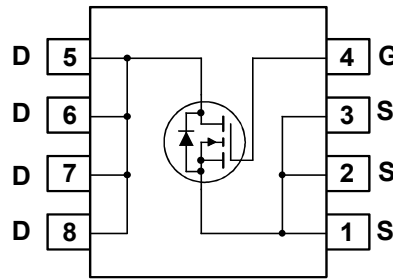
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $r_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

### Application

- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier



Power 56 (Bottom view)



### MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ C$	27	A
	-Continuous (Silicon limited) $T_C = 25^\circ C$	27	
	-Continuous $T_A = 25^\circ C$ (Note 1a)	4.5	
	-Pulsed	30	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	150	mJ
$P_D$	Power Dissipation $T_C = 25^\circ C$	78	W
	Power Dissipation $T_A = 25^\circ C$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2572	FDMS2572	Power 56	13"	12mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		180		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-9.8		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 4.5\text{A}$		36	47	m $\Omega$
		$V_{GS} = 6\text{V}, I_D = 4.5\text{A}$		39	53	
		$V_{GS} = 10\text{V}, I_D = 4.5\text{A}, T_J = 125^\circ\text{C}$		69	103	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 4.5\text{A}$		14		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1960	2610	pF
$C_{oss}$	Output Capacitance			130	175	pF
$C_{rss}$	Reverse Transfer Capacitance			30	45	pF
$R_g$	Gate Resistance	$f = 1\text{MHz}$	0.1	1.3	2.6	$\Omega$

### Switching Characteristics

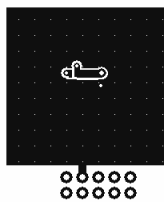
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{V}, I_D = 1.0\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		11	20	ns
$t_r$	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns
$t_f$	Fall Time			31	50	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to $10\text{V}$	$V_{DD} = 75\text{V}$ $I_D = 4.5\text{A}$	31	43	nC
$Q_{gs}$	Gate to Source Gate Charge			9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 2.2\text{A}$ (Note 2)		0.7	1.0	V
$t_{rr}$	Reverse Recovery Time	$I_F = 4.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$		67	101	ns
$Q_{rr}$	Reverse Recovery Charge			130	195	nC

#### Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5$  in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper

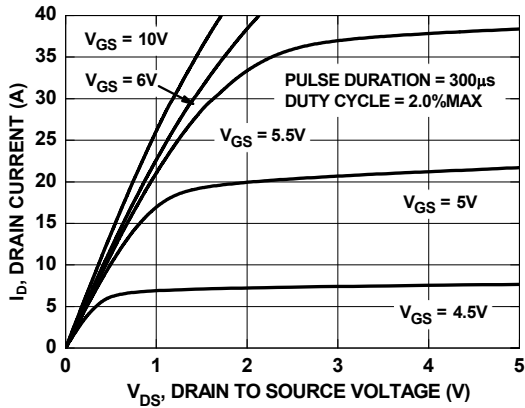


b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

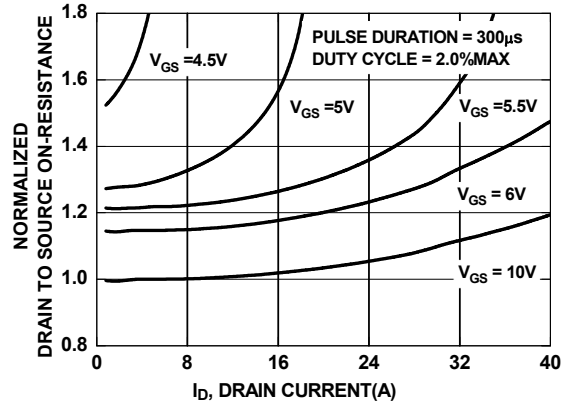
2: Pulse Test: Pulse Width  $< 300\mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3:  $E_{AS}$  of 150 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 10\text{A}$ ,  $V_{DD} = 150\text{V}$ ,  $V_{GS} = 10\text{V}$ .

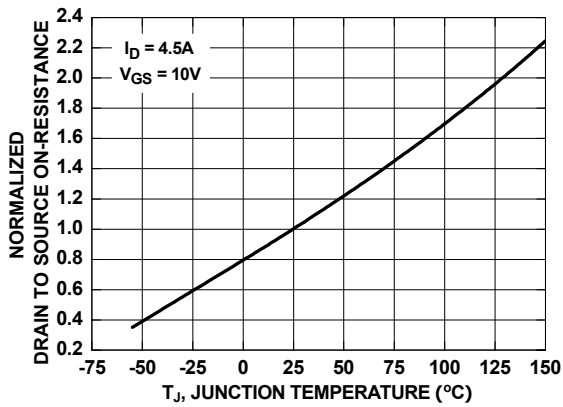
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



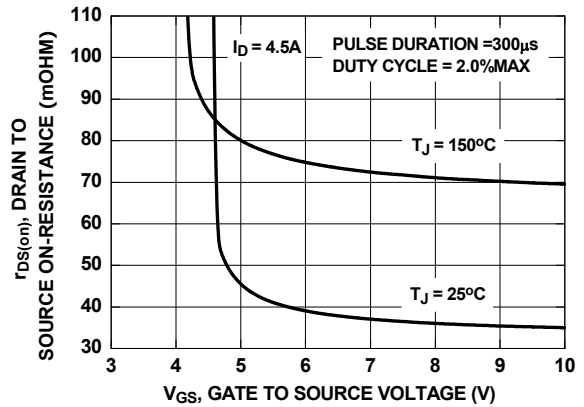
**Figure 1. On-Region Characteristics**



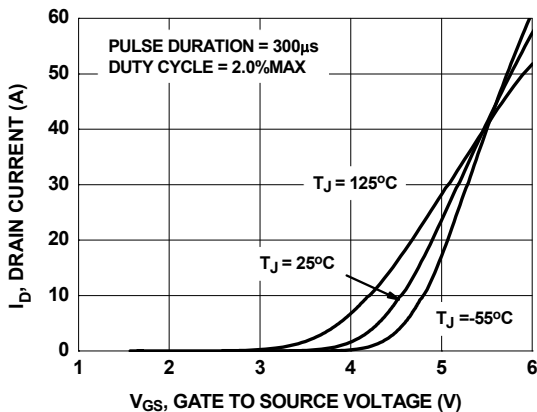
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



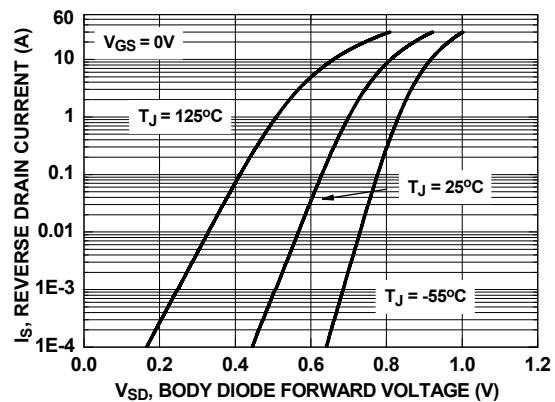
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

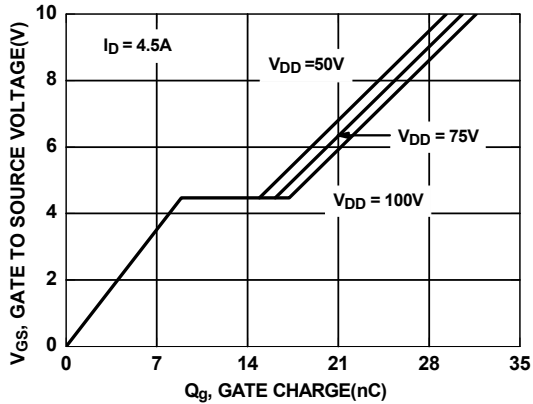


**Figure 5. Transfer Characteristics**

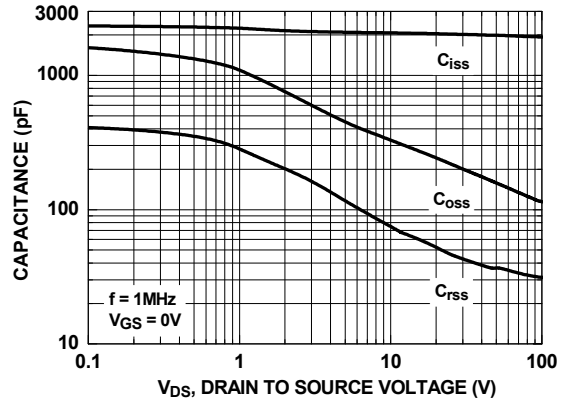


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

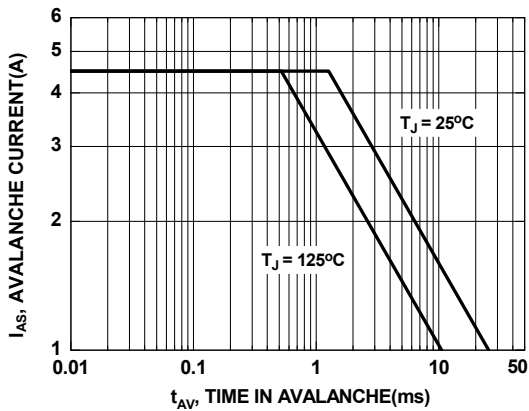
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



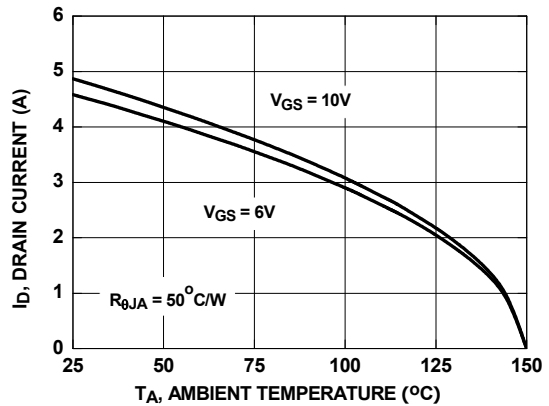
**Figure 7. Gate Charge Characteristics**



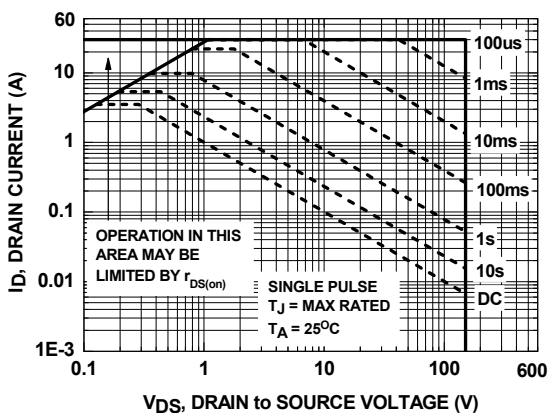
**Figure 8. Capacitance vs Drain to Source Voltage**



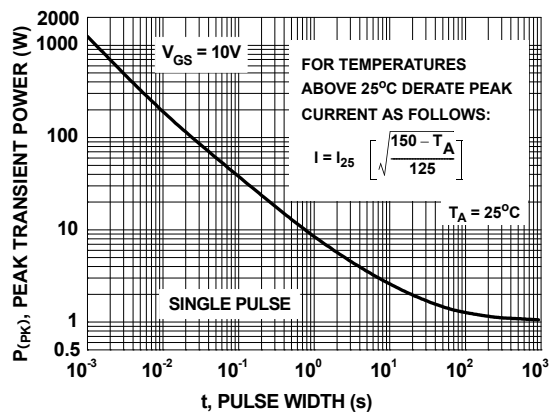
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

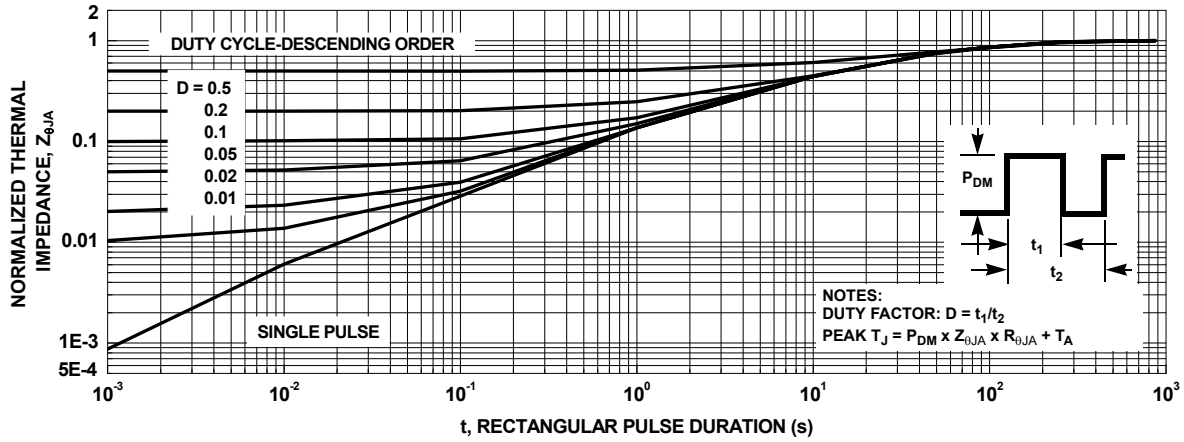


**Figure 11. Forward Bias Safe Operating Area**

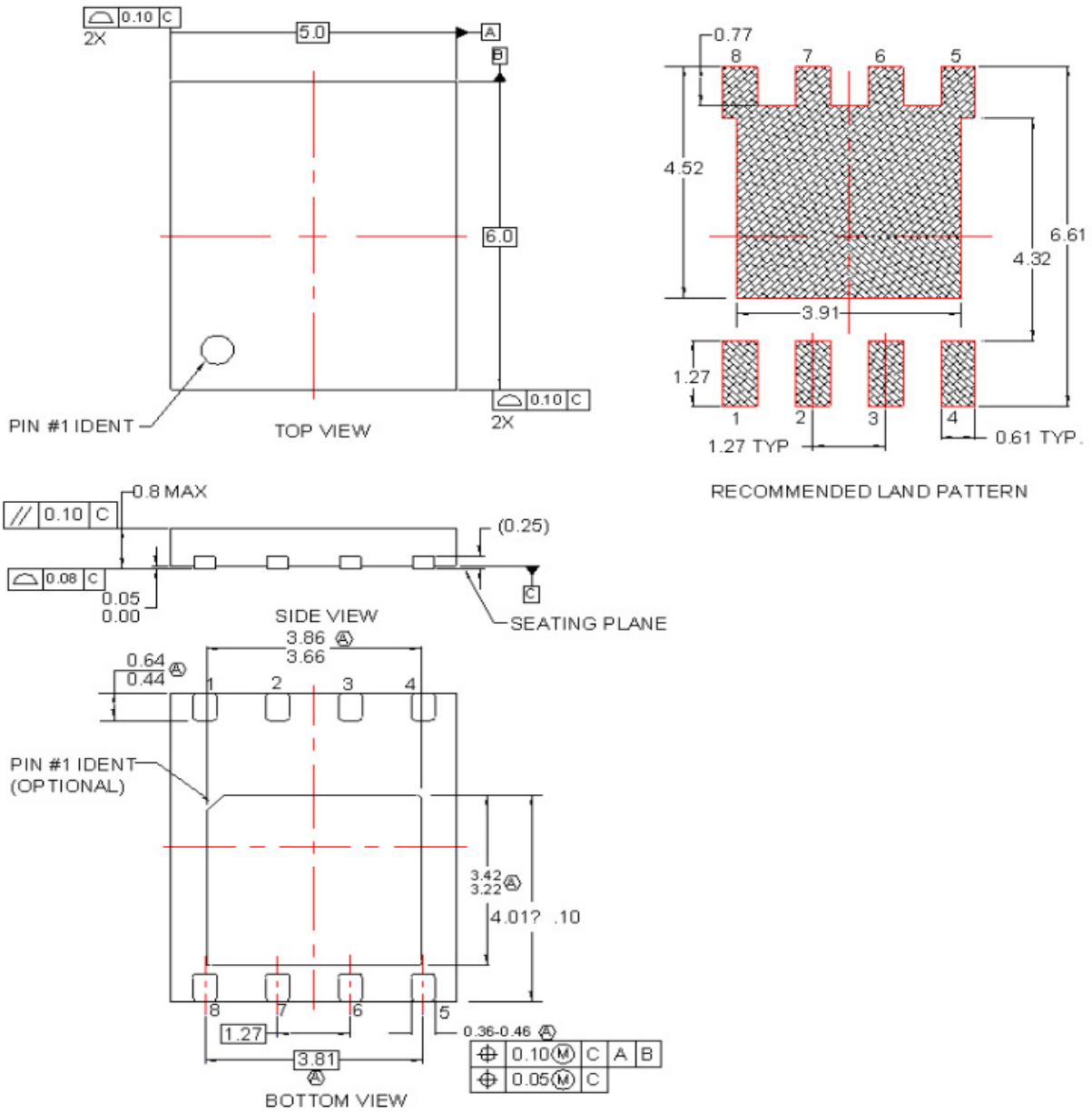


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



**NOTES:**





- (A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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