PI6CB332001A

20-Output PCIe 4.0/5.0 Clock Buffer With On-chip Termination

Features

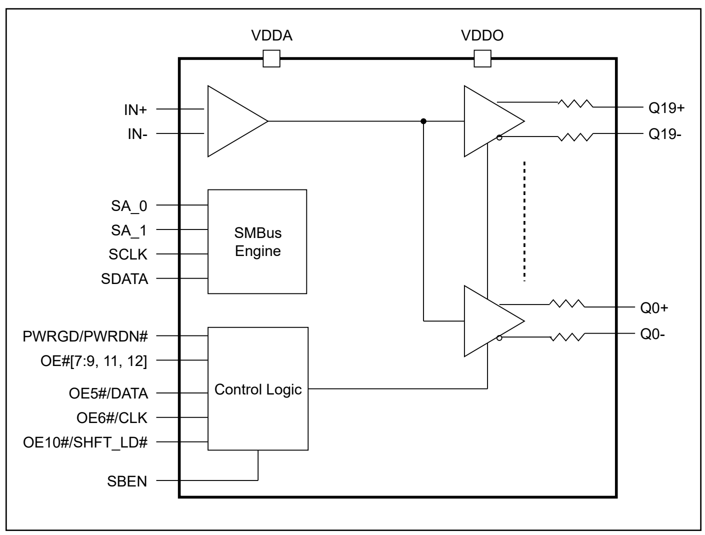
- Supports Intel's DB2000QL spec
- 3.3V supply voltage
- HCSL input: 100MHz (typ), up to 400MHz
- 20 differential low-power HCSL outputs with on-chip termination
- Two output enable control modes
  - Traditional 8 OE# pins with power down tolerance and 20 SMBus bits
  - Simple 3-wire Side-Band interface real-time control
- SMBus interface support
- Spread spectrum tolerant
- Very low jitter outputs
  - Differential additive phase jitter: DB2000Q <30fs RMS
  - Differential additive phase jitter: PCIe 4.0 <30fs RMS
  - Differential additive phase jitter: PCIe 5.0 <20fs RMS
  - PCIe 1.0/2.0/3.0/4.0/5.0 compliant
- Differential output-to-output skew <50ps
- Low propagation delay: <3ns
- Industrial temperature support: -40°C to 85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen- and Antimony-Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 80-lead 6x6mm dual-row aQFN

Description

The PI6CB332001A is a 20-output, very low-power, PCIe 1.0/2.0/3.0/4.0/5.0 clock buffer. The device is capable of distributing the reference clocks for UPI, SAS, SATA, and other applications. It takes a reference input to fanout twenty 100MHz low-power differential HCSL outputs with on-chip terminations. The on-chip termination can save 80 external resistors and make layout easier. OE pins combined with SMBus bits, as well as a 3-wire side band interface, provide easier power management for each output. All OE pins are power down tolerant, which allows the OE pins to be driven by external signals when the device is in a power down or reset condition. The device must reset and power up properly if these pins are driven to any valid voltage prior to the assertion of VDD or PWRGD#.

The device uses Diodes' proprietary design to achieve very low jitter that meets PCIe 1.0/2.0/3.0/4.0/5.0 requirements.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12
A	Q17+	Q16-	Q16+	Q15-	Q15+	Q14-	Q14+	Q13-	Q13+	Q12-	Q12+	Q11-
B	Q17-	VDDO	NC	SA_0	NC	VDDO	NC	SA_1	NC	OE12#	VDDO	Q11+
C	Q18+	NC									OE11#	Q10-
D	Q18-	NC									NC	Q10+
E	Q19+	SBEN									OE10#/SH-FT_LD#	OE9#
F	Q19-	NC									NC	Q9-
G	IN+	NC									NC	Q9+
H	IN-	VDDA									OE8#	Q8-
J	Q0+	NC									NC	Q8+
K	Q0-	NC									OE7#	Q7-
L	Q1+	VDDO	NC	SDATA	SCLK	NC	NC	OE5#/DATA	NC	OE6#/CLK	VDDO	Q7+
M	Q1-	Q2+	Q2-	Q3+	Q3-	PWRGD/PWRDN#	Q4+	Q4-	Q5+	Q5-	Q6+	Q6-

EPAD is GND

Pin Description

Pin Number	Pin Name	Type		Description
A1	Q17+	Output	HCSL	Differential true clock output
A2	Q16-	Output	HCSL	Differential complementary clock output
A3	Q16+	Output	HCSL	Differential true clock output
A4	Q15-	Output	HCSL	Differential complementary clock output
A5	Q15+	Output	HCSL	Differential true clock output
A6	Q14-	Output	HCSL	Differential complementary clock output
A7	Q14+	Output	HCSL	Differential true clock output
A8	Q13-	Output	HCSL	Differential complementary clock output
A9	Q13+	Output	HCSL	Differential true clock output
A10	Q12-	Output	HCSL	Differential complementary clock output

Pin Description Cont.

Pin Number	Pin Name	Type		Description
A11	Q12+	Output	HCSL	Differential true clock output
A12	Q11-	Output	HCSL	Differential complementary clock output
B1	Q17-	Output	HCSL	Differential complementary clock output
B2	VDDO	Power		Power supply for outputs, nominal 3.3V
B3	NC			No connect
B4	SA_0	Input	CMOS	SMBus address bit. This is a tri-level input that works in conjunction with SA_1 pin, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
B5	NC			No connect
B6	VDDO	Power		Power supply for outputs, nominal 3.3V
B7	NC			No connect
B8	SA_1	Input	CMOS	SMBus address bit. This is a tri-level input that works in conjunction with SA_0 pin, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to VDD/2. See the SMBus Address Selection table.
B9	NC			No connect
B10	OE12#	Input	CMOS	Active low input for enabling Q12 pair. 1 =disable outputs, 0 = enable outputs. The pin has internal pull down
B11	VDDO	Power		Power supply for outputs, nominal 3.3V
B12	Q11+	Output	HCSL	Differential true clock output
C1	Q18+	Output	HCSL	Differential true clock output
C2	NC			No connect
C11	OE11#	Input	CMOS	Active low input for enabling Q11 pair. 1 =disable outputs, 0 = enable outputs. The pin has internal pull down
C12	Q10-	Output	HCSL	Differential complementary clock output
D1	Q18-	Output	HCSL	Differential complementary clock output
D2	NC			No connect
D11	NC			No connect
D12	Q10+	Output	HCSL	Differential true clock output
E1	Q19+	Output	HCSL	Differential true clock output
E2	SBEN	Input	CMOS	Input that enables the Side-Band Interface for controlling output enables. This pin disables the output enable pins when asserted. It has an internal pull-down resistor. 0 = OE pins and SMBus enable bits control outputs, Side-band interface disabled. 1 = Side-Band Interface controls output enables, OE pins and SMBus enable bits are disabled

Pin Description Cont.

Pin Number	Pin Name	Type		Description
E11	OE10#/SHFT_LD#	Input	CMOS	Active low input for enabling output 10 or SHFT_LD- pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side-Band Mode: 1 = enable Side-Band Interface shift register, 0 = disable Side-Band Interface shift register. A falling edge transfers Side-Band shift register contents to output register
E12	OE9#	Input	CMOS	Active low input for enabling Q9 pair. 1 =disable outputs, 0 = enable outputs. The pin has internal pull down
F1	Q19-	Output	HCSL	Differential complementary clock output
F2	NC			No connect
F11	NC			No connect
F12	Q9-	Output	HCSL	Differential complementary clock output
G1	IN+	Input	HCSL	Differential true clock input
G2	NC			No connect
G11	NC			No connect
G12	Q9+	Output	HCSL	Differential true clock output
H1	IN-	Input	HCSL	Differential complementary clock input
H2	VDDA	Power		Power supply for inputs and analog circuits, nominal 3.3V
H11	OE8#	Input	CMOS	Active low input for enabling Q8 pair. 1 =disable outputs, 0 = enable outputs. The pin has internal pull down
H12	Q8-	Output	HCSL	Differential complementary clock output
J1	Q0+	Output	HCSL	Differential true clock output
J2	NC			No connect
J11	NC			No connect
J12	Q8+	Output	HCSL	Differential true clock output
K1	Q0-	Output	HCSL	Differential complementary clock output
K2	NC			No connect
K11	OE7#	Input	CMOS	Active low input for enabling Q7 pair. 1 =disable outputs, 0 = enable outputs. The pin has internal pull down
K12	Q7-	Output	HCSL	Differential complementary clock output
L1	Q1+	Output	HCSL	Differential true clock output
L2	VDDO	Power		Power supply for outputs, nominal 3.3V
L3	NC			No connect
L4	SDATA	I/O	CMOS	SMBus data pin
L5	SCLK	Input	CMOS	SMBus clock pin
L6	NC			No connect
L7	NC			No connect

Pin Description Cont.

Pin Number	Pin Name	Type		Description
L8	OE5#/DATA	Input	CMOS	Active low input for enabling output 5 or the data pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side-Band mode: Data pin
L9	NC			No connect
L10	OE6#/CLK	Input	CMOS	Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side Band mode: Clocks data into the Side-Band Interface shift register on the rising edge
L11	VDDO	Power		Power supply for outputs, nominal 3.3V
L12	Q7+	Output	HCSL	Differential true clock output
M1	Q1-	Output	HCSL	Differential complementary clock output
M2	Q2+	Output	HCSL	Differential true clock output
M3	Q2-	Output	HCSL	Differential complementary clock output
M4	Q3+	Output	HCSL	Differential true clock output
M5	Q3-	Output	HCSL	Differential complementary clock output
M6	PWRGD/ PWRDN#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor
M7	Q4+	Output	HCSL	Differential true clock output
M8	Q4-	Output	HCSL	Differential complementary clock output
M9	Q5+	Output	HCSL	Differential true clock output
M10	Q5-	Output	HCSL	Differential complementary clock output
M11	Q6+	Output	HCSL	Differential true clock output
M12	Q6-	Output	HCSL	Differential complementary clock output
	EPAD	Power		Connect to Ground

SMBus Address Selection Table

SA_1	SA_0	Address
L	L	D8
L	M	DA
L	H	DE
M	L	C2
M	M	C4
M	H	C6
H	L	CA
H	M	CC
H	H	CE

Output Control - SBEN=0

Inputs		OE# Pins and Register Bits		Side Band Interface		
PWRGD/ PWRDN#	IN+/IN-	SMBUS Enable Bit	OE# Pin	MASKx Byte[10:8]	Dx	Q+/Q- [19:0]
0	X	X	X	X	X	Low/Low
1	Running	0	X	X	X	Low/Low
		1	0	X	X	Running
		1	1	X	X	Low/Low
1	Stopped	1	0	X	X	Stopped
		1	1	X	X	Low/Low

Output Control - SBEN=1

Inputs		OE# Pins and Register Bits		Side Band Interface		
PWRGD/ PWRDN#	IN+/IN-	SMBUS Enable Bit	OE# Pin	MASKx Byte[10:8]	Dx	Q+/Q- [19:0]
0	X	X	X	X	X	Low/Low
1	Running	X	X	0	0	Low/Low
		X	X	0	1	Running
		X	X	1	X	Running
1	Stopped	X	X	0	0	Low/Low
		X	X	0	1	Stopped
		X	X	1	X	Stopped

Output Enable Control on PI6CB332001A

The 20-output PI6CB332001A has two methods for enabling and disabling outputs. The first is the traditional method of OE# pins and SMBus output enable bits. The second method is a simple 3-wire serial interface referred, to as the Side-Band Interface (SBI). Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN pin high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output enable interface.

Both the SBI and the traditional interface feed the common output enable/disable synchronization logic, ensuring the glitch-free enabling and disabling of outputs, regardless of the method used.

Traditional Method

Outputs 5 through 12 have dedicated output enable pins, and each of the 20 outputs have dedicated SMBus output enable bits in Byte0, Byte1, and Byte2 of the SMBus register set.

Side-Band Interface

This interface consists of DATA, CLK, and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the Output register.

When the SBI is enabled, OE[7:9, 11, 12]# are disabled, and DATA, CLK, and SHFT_LD# are enabled on OE5#, OE6# and OE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) and becomes active. When set to one, the mask register forces its respective output to 'enabled.' This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read-back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled and power is applied, the SBI becomes active even if the PWRGD/PWRDN# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of PWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. Figure 1 provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift bits to disable their respective output. See Figure 1.

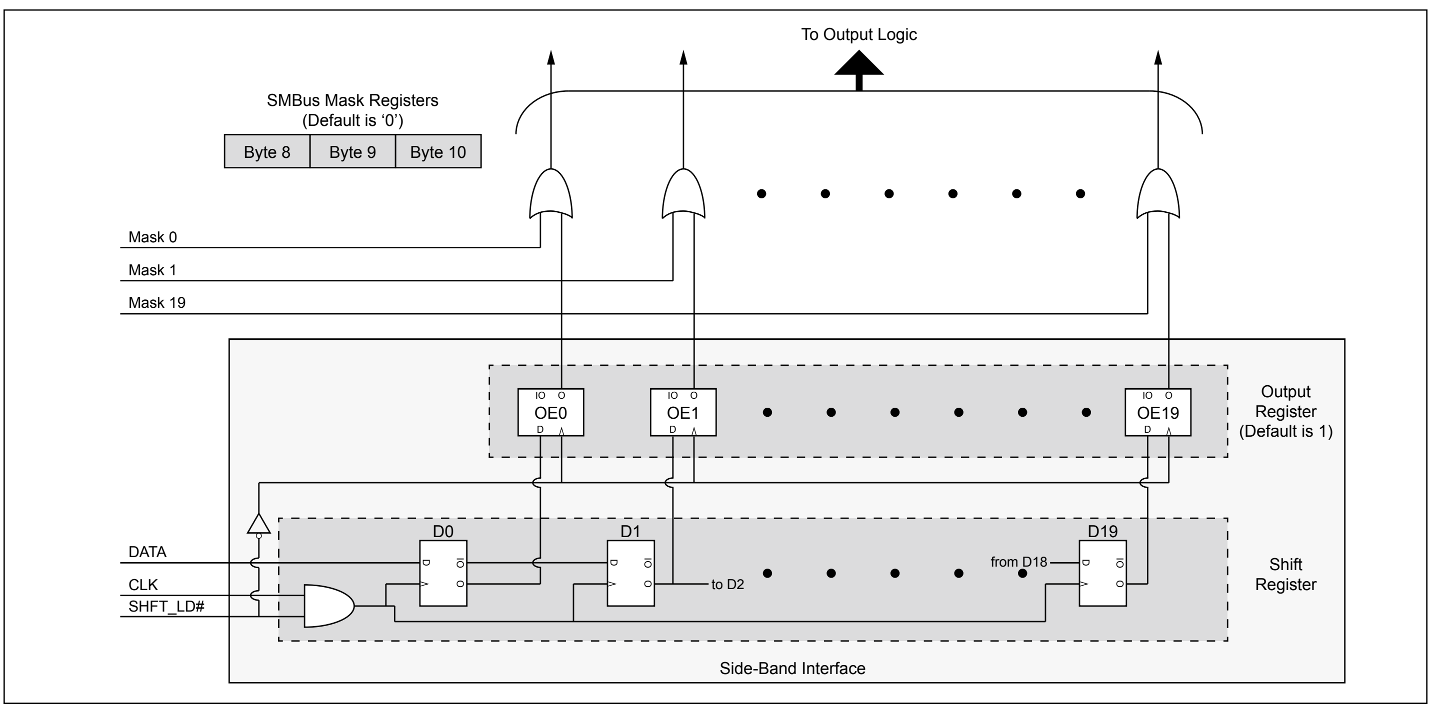


Figure 1. Side Band Interface Control Logic Description

Figures 2 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock for output 19, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

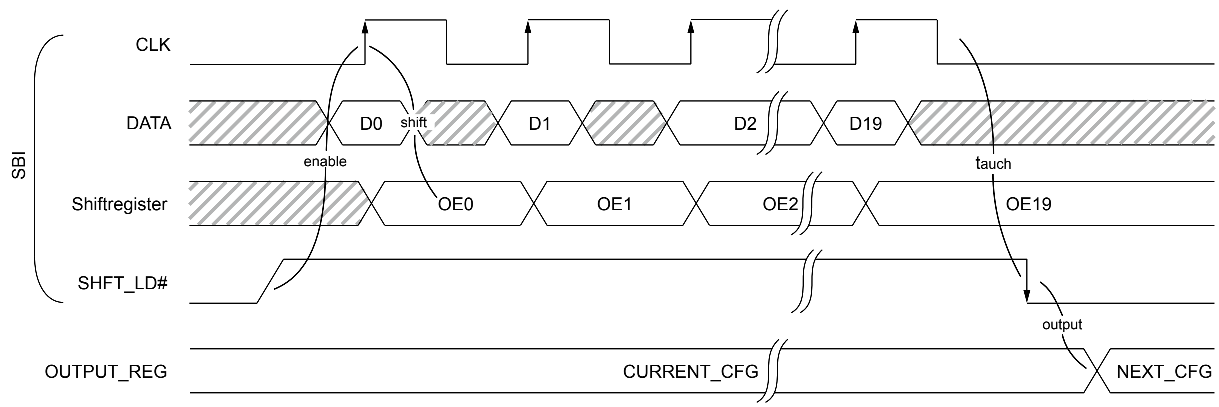


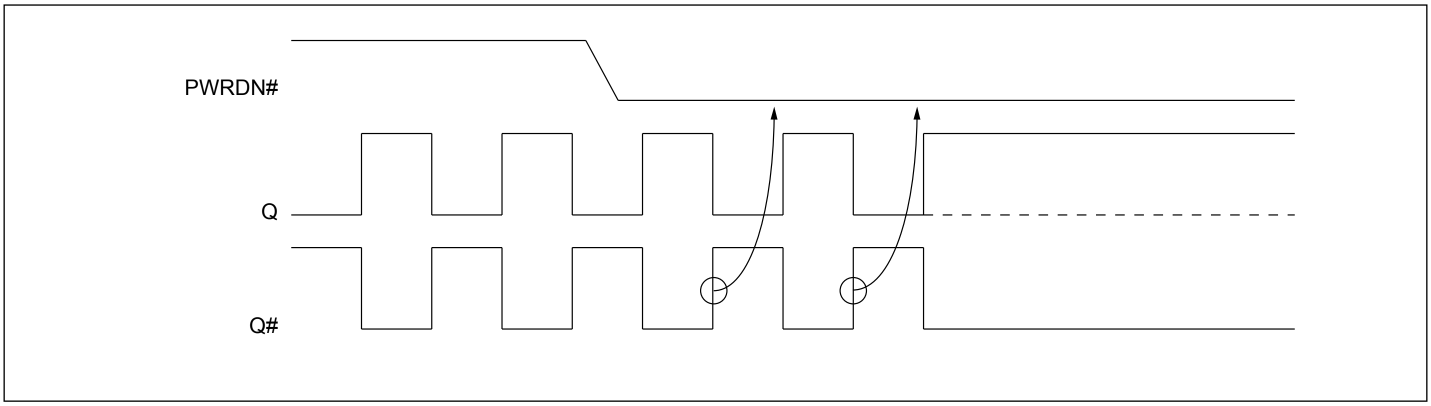
Figure 2. Side Band Interface Functional Timing

The SBI interface supports clock rates up to 10MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LD# pin to each devices allows its use as a chip-select pin. When the SHFT_LD# pin is low, the PI6CB332001A ignores any activity on the CLK and DATA pins.

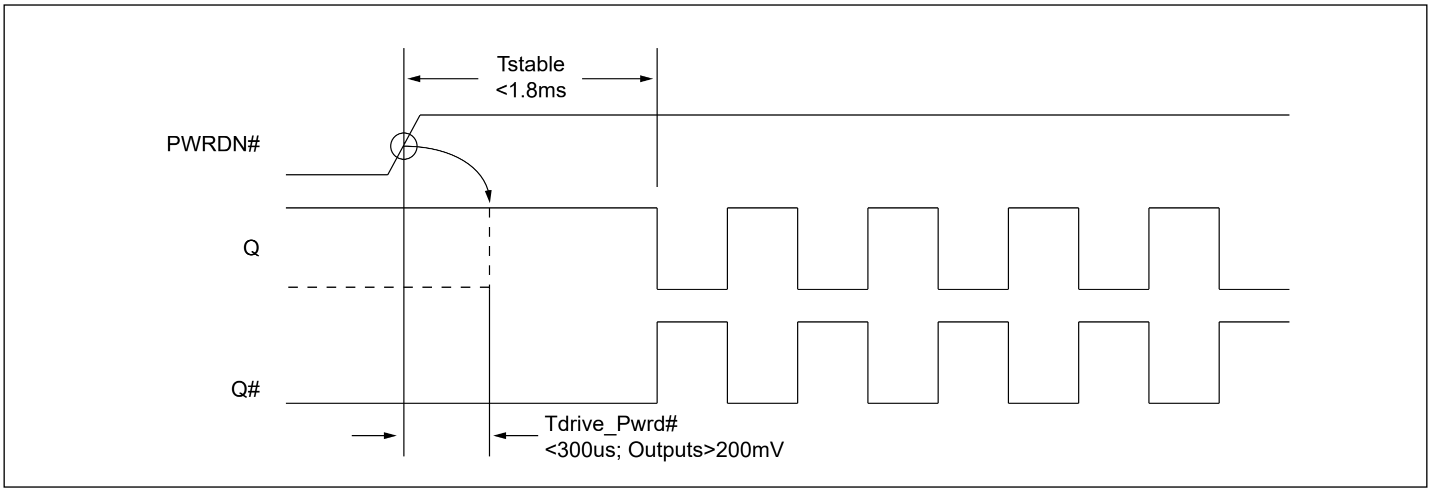
Power Management Table

PWRGD/PWRDN#	Q+	Q-
0	Low	Low
1	Normal	Normal

PWRDN# Assertion



PWRGD Assertion



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential, V_{DDxx}	−0.5V to +4.0V
Input Control Pins Voltage	−0.5V to V_{DD}+0.5V
CLK+/- pins	-0.5V to 2.5V
SMBus, Input High Voltage	3.9V
ESD Protection (HBM)	2000V
Junction Temperature	125 °C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DD}, V_{DD_A}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	V_{DD} + V_{DDA}, All outputs active @100MHz		160	200	mA
I_{DD_PD}	Power Supply Power Down(1) Current	V_{DD} + V_{DDA}, All outputs LOW/LOW		3	5	mA
T_A	Ambient Temperature	Industrial grade	−40		85	°C

Note:

1. Input clock is not running.

Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R_{pu}	Internal pull up resistance			120		KΩ
R_{dn}	Internal pull down resistance			120		KΩ
L_{PIN}	Pin inductance				7	nH

SMBus Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{DDSMB}	Nominal bus voltage		2.7		3.6	V
V_{IHSMB}	SMBus Input High Voltage	SMBus, V_{DDSMB} = 3.3V	2.1		3.6	V
		SMBus, V_{DDSMB} < 3.3V	0.65 V_{DDSMB}			
V_{ILSMB}	SMBus Input Low Voltage	SMBus, V_{DDSMB} = 3.3V			0.6	V
		SMBus, V_{DDSMB} < 3.3V			0.6	
$I_{SMBSINK}$	SMBus sink current	SMBus, at V_{OLSMB}	4			mA
V_{OLSMB}	SMBus Output Low Voltage	SMBus, at $I_{SMBSINK}$			0.4	V
f_{MAXSMB}	SMBus operating frequency	Maximum frequency			400	kHz
t_{RMSB}	SMBus rise time	(Max V_{IL} - 0.15) to (Min V_{IH} + 0.15)			1000	ns
t_{FMSB}	SMBus fall time	(Min V_{IH} + 0.15) to (Max V_{IL} - 0.15)			300	ns

LVCMOS DC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Single-ended inputs, except tri-level pins	2		V_{DD} +0.3	V
V_{IL}	Input Low Voltage	Single-ended inputs, except tri-level pins	-0.3		0.8	V
V_{IH}	Input High Voltage	Single-ended tri-level inputs	2.4		V_{DD} +0.3	V
V_{IM}	Input Mid Voltage	Single-ended tri-level inputs	1.3	0.5V_{DD}	1.8	V
V_{IL}	Input Low Voltage	Single-ended tri-level inputs	-0.3		0.9	V
I_{IH}	Input High Current	Single-ended inputs, V_{IN} = V_{DD}			5	μA
I_{IL}	Input Low Current	Single-ended inputs, V_{IN} = 0V	-5			μA
I_{IH}	Input High Current	Single-ended inputs with pull up resistor, V_{IN} = V_{DD}			50	μA
I_{IL}	Input Low Current	Single-ended inputs with pull up resistor, V_{IN} = 0V	-50			μA
C_{IN}	Input Capacitance		1.5		5	pF
t_{RF}	Rise/ Fall time of Input				5	ns

LVCMOS AC Electrical Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{OELAT}	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion		5	10	clocks
t_{PDLAT}	PD# de-assertion	Differential outputs enable after PD# de-assertion			300	us
t_{STAB}	Output stabilization	From power up and after input clock stabilization or after PD# de-assertion to 1st clock		1.0	1.8	ms

HCSL Input Characteristics[1]

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	V_{DD}= 3.3V	1	100	400	MHz
V_{IHDIF}	Diff. Input High Voltage [3]	IN+, IN-, single-end measurement	330		1150	mV
V_{ILDIF}	Diff. Input Low Voltage [3]	IN+, IN-, single-end measurement	-300	0	300	mV
V_{SWING}	Diff. Input Swing Voltage	Peak to peak value (V_{IHDIF} - V_{ILDIF})	200			mV
V_{COM}	Common mode voltage		100		900	mV
t_{RF}	Diff. Input Slew Rate [2]		0.7			V/ns
I_{IN}	Diff. Input Leakage Current	$V_{IN+} = V_{DD}$, $V_{IN-} = 0.8V$	-40		100	uA
t_{DC}	Diff. Input Duty Cycle	Measured differentially	45		55	%
tj_{c-c}	Diff. Input Cycle to cycle jitter	Measured differentially			125	ps

Note:
1. Guaranteed by design and characterization, not 100% tested in production
2. Slew rate measured through +/-75mV window centered around differential zero
3. The device can be driven by a single-ended clock by driving the true clock and biasing the complement clock input to the Vbias, where Vbias is (V_{IH}-V_{IL})/2

HCSL Output Characteristics

Temperature = T_A; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V_{MAX}	Maximum output voltage	Measurement on single ended signal using absolute value	660	780	900	mV
V_{MIN}	Minimum output voltage		-150	20	150	mV
Vcross absolute	Absolute Crossing point Voltage		250		550	mV
Vcross relative	Relative Crossing point Voltage				140	mV
f_{OUT}	Output Frequency			100	400	MHz
t_{RF}	Slew rate (1,2,3)	Scope averaging on, 10 inches trace	1.5	3.0	4	V/ns
Dt_{RF}	Slew rate matching (1,2,4)	Scope averaging on, 10 inches trace			20	%
t_{SKEW}	Output Skew (1,2)	Averaging on, V_T = 50%			50	ps
t_{DC}	Diff. Output Duty Cycle	Measured differentially	45		55	%
DC Distortion	Duty Cycle Distortion (5)	Measured differentially at 100MHz	-0.5		0.5	%
T_{pd}	Propagation Delay			2.0	3	ns

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured through +/-75mV window centered around differential zero
5. Duty cycle distortion is the difference in duty cycle between the out and input clock

Side Band Interface

Temperature = T_A; Supply voltages per normal operation conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
t_{PERIOD}	Side Band clock period		40			ns
t_{SETUP}	SHFT Setup time	SHFT setup time to CLK rising edge	10			ns
t_{DSETUP}	Data setup time	DATA setup time to CLK rising edge	5			ns
t_{DHOLD}	Data hold time (1)	DATA hold time after CLK rising edge	2			ns
t_{DELAY}	Delay time (1)	Delay from CLK rising edge to LD# falling edge	10			ns
t_{PD}	Propagation delay (2)	Delay LD# falling edge to next output configuration taking effect	4		10	clocks
t_{RF}	CLK slew rate (3)	CLK input between 20% to 80%	0.7		4	V/ns

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Refer to device differential input clock
3. Control input must be monotonic from 20% to 80% of input swing

PCIe Common Clock (CC) Architecture Jitter (3)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Additive Integrated phase jitter (RMS) (1)	PCIe 1.0		0	0.03	86	ps (pkpk)
		PCIe 2.0 Low Band, 10kHz < f < 1.5MHz (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0	0.03	3	ps
		PCIe 2.0 High Band, 1.5MHz < f < Nyquist (50MHz); (PLL BW 5-16MHz or 8-5MHz, CDR = 10MHz)		0	0.03	3.1	ps
		PCIe 3.0 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0	0.03	1	ps
		PCIe 4.0 (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0	0.03	0.5	ps
		PCIe 5.0 (PLL BW of 500k to 1.8MHz. CDR =20MHz) (4)		0.07	0.12	0.15	ps
		100MHz (12kHz to 20MHz), input jitter ~156fs (2)		67	105	NA(5)	fs
		156.25MHz (12kHz to 20MHz), input jitter ~110fs (2)		50	90	NA(5)	fs
		100MHz, apply DB2000Q filter, see figure 5			25	80	fs

PCIe Independent Reference Clock Architecture Jitter (3)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Spec Limit	Units
t_{jPHASE}	Additive Integrated phase jitter (RMS)	PCIe 3.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0	0.03	0.7	ps
		PCIe 4.0 SRIS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0	0.03	0.7	ps
		PCIe 4.0 SRNS (PLL BW 2-4MHz or 2-5MHz, CDR= 10MHz)		0	0.03	0.7	ps

Note:

1. Guaranteed by design and characterization, not 100% tested in production
2. Additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)^{*2} - (input jitter)^{*2}]
3. See http://www.pcisig.com for complete specs
4. PCIe 5.0 v0.9 specification
5. Not available

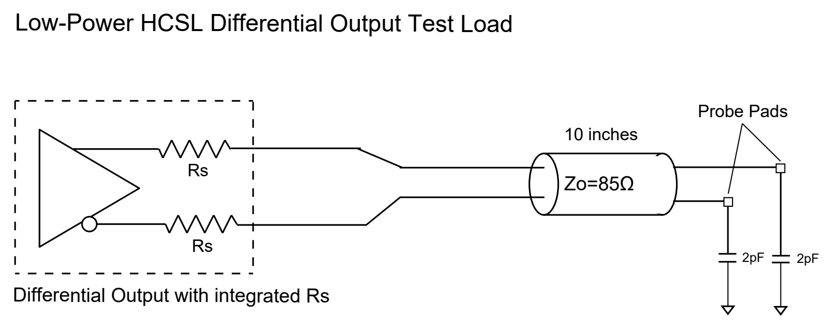


Figure 3. Low Power HCSL Test Circuit

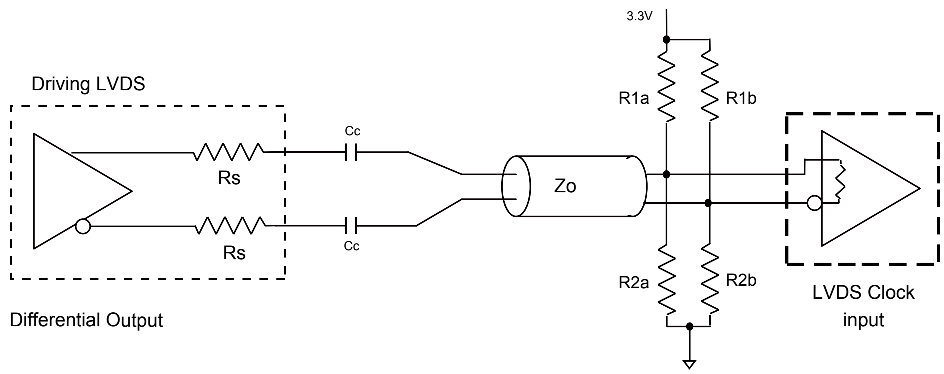


Figure 4. Differential Output Driving LVDS

Differential Output Terminations Driving LVDS (Z_0 =85Ω)

Component	Receiver with termination	Receiver without termination	Unit
R_{1a}, R_{1b}	10,000	130	Ω
R_{2a}, R_{2b}	5,600	64	Ω
C_C	0.1	0.1	µF
V_{CM}	1.2	1.2	V

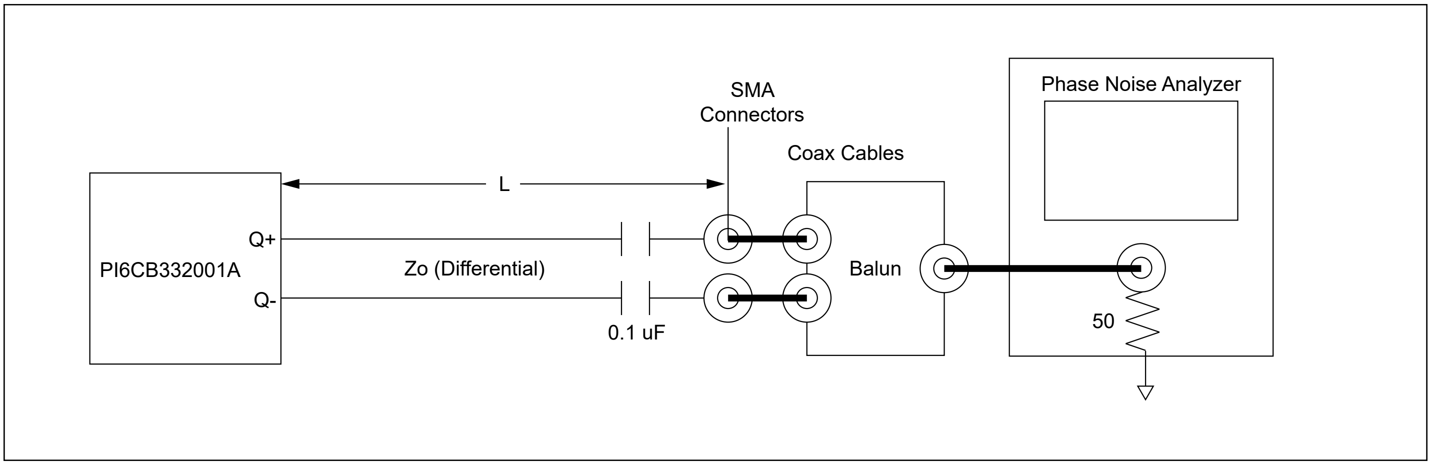


Figure 5. Test Setup for PI6CB332001A Additive Phase Jitter Measurement

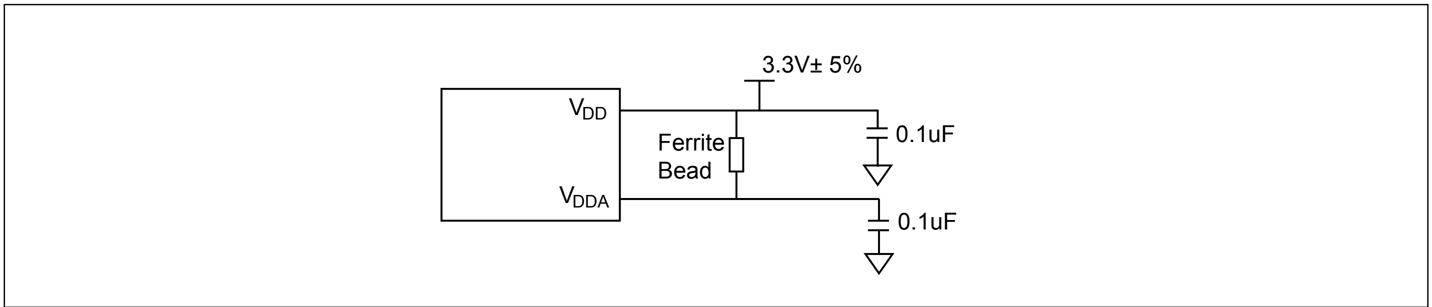


Figure 6. Power Supply Filter

SMBus Serial Data Interface

PI6CB332001A is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	See SMBus Address Selection table			1/0

Note: SMBus address is latched on SADR pin

How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	....	Data Byte (N+X-1)	Ack	Stop bit

How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
....	Data Byte (N+X-1)	NAck	Stop bit

Byte 0: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Q19_OE	Q19 output enable	RW	1	Low/Low	Enable
5	Q18_OE	Q18 output enable	RW	1	Low/Low	Enable
4	Q17_OE	Q17 output enable	RW	1	Low/Low	Enable
3	Q16_OE	Q16 output enable	RW	1	Low/Low	Enable
2	Reserved			0		
1	Reserved			0		
0	Reserved			0		

Byte 1: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q7_OE	Q7 output enable	RW	1	Low/Low	OE7# control
6	Q6_OE	Q6 output enable	RW	1	Low/Low	OE6# control
5	Q5_OE	Q5 output enable	RW	1	Low/Low	OE5# control
4	Q4_OE	Q4 output enable	RW	1	Low/Low	Enable
3	Q3_OE	Q3 output enable	RW	1	Low/Low	Enable
2	Q2_OE	Q2 output enable	RW	1	Low/Low	Enable
1	Q1_OE	Q1 output enable	RW	1	Low/Low	Enable
0	Q0_OE	Q0 output enable	RW	1	Low/Low	Enable

Byte 2: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Q15_OE	Q15 output enable	RW	1	Low/Low	Enable
6	Q14_OE	Q14 output enable	RW	1	Low/Low	Enable
5	Q13_OE	Q13 output enable	RW	1	Low/Low	Enable
4	Q12_OE	Q12 output enable	RW	1	Low/Low	OE12# control
3	Q11_OE	Q11 output enable	RW	1	Low/Low	OE11# control
2	Q10_OE	Q10 output enable	RW	1	Low/Low	OE10# control
1	Q9_OE	Q9 output enable	RW	1	Low/Low	OE9# control
0	Q8_OE	Q8 output enable	RW	1	Low/Low	OE8# control

Byte 3: OE# Pin Realtime Readback Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	OE12#	Realtime Readback of OE12#	R	Realtime	OE12# = Low	OE12# = High
6	OE11#	Realtime Readback of OE11#	R	Realtime	OE11# = Low	OE11# = High
5	OE10#	Realtime Readback of OE10#	R	Realtime	OE10# = Low	OE10# = High
4	OE9#	Realtime Readback of OE9#	R	Realtime	OE9# = Low	OE9# = High
3	OE8#	Realtime Readback of OE8#	R	Realtime	OE8# = Low	OE8# = High
2	OE7#	Realtime Readback of OE7#	R	Realtime	OE7# = Low	OE7# = High
1	OE6#	Realtime Readback of OE6#	R	Realtime	OE6# = Low	OE6# = High
0	OE5#	Realtime Readback of OE5#	R	Realtime	OE5# = Low	OE5# = High

Byte 4: SBEN

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:1	Reserved			0		
0	RB_SBEN	Readback of SBEN	R	Realtime	SBEN=Low	SBEN=High

Byte 5: Revision and Vendor ID Register

<table>
<tr><th>Bit</th><th>Control Function</th><th>Description</th><th>Type</th><th>Power Up Condition</th><th>0</th><th>1</th></tr>
<tr><td>7</td><td>RID3</td><td rowspan="4">Revision ID</td><td>R</td><td>0</td><td rowspan="4" colspan="2">rev = 0000</td></tr>
<tr><td>6</td><td>RID2</td><td>R</td><td>0</td></tr>
<tr><td>5</td><td>RID1</td><td>R</td><td>0</td></tr>
<tr><td>4</td><td>RID0</td><td>R</td><td>0</td></tr>
<tr><td>3</td><td>PVID3</td><td rowspan="4">Vendor ID</td><td>R</td><td>0</td><td rowspan="4" colspan="2">Pericom = 0011</td></tr>
<tr><td>2</td><td>PVID2</td><td>R</td><td>0</td></tr>
<tr><td>1</td><td>PVID1</td><td>R</td><td>1</td></tr>
<tr><td>0</td><td>PVID0</td><td>R</td><td>1</td></tr>
</table>

Byte 6: Device Type/Device ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DID7	Device ID	R	0		
6	DID6		R	1		
5	DID5		R	0		
4	DID4		R	0		
3	DID3		R	1		
2	DID2		R	0		
1	DID1		R	0		
0	DID0		R	0		

Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		

Byte 8: Side-band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask7	Mask off Side-band Disable	RW	0	Side-band shift register may disable the output	Force output to be enabled regardless of side-band shift register value
6	Mask6	Mask off Side-band Disable	RW	0		
5	Mask5	Mask off Side-band Disable	RW	0		
4	Mask4	Mask off Side-band Disable	RW	0		
3	Mask3	Mask off Side-band Disable	RW	0		
2	Mask2	Mask off Side-band Disable	RW	0		
1	Mask1	Mask off Side-band Disable	RW	0		
0	Mask0	Mask off Side-band Disable	RW	0		

Byte 9: Side-band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Mask15	Mask off Side-band Disable	RW	0	Side-band shift register may disable the output	Force output to be enabled regardless of side-band shift register value
6	Mask14	Mask off Side-band Disable	RW	0		
5	Mask13	Mask off Side-band Disable	RW	0		
4	Mask12	Mask off Side-band Disable	RW	0		
3	Mask11	Mask off Side-band Disable	RW	0		
2	Mask10	Mask off Side-band Disable	RW	0		
1	Mask9	Mask off Side-band Disable	RW	0		
0	Mask8	Mask off Side-band Disable	RW	0		

Byte 10: Side-band Mask Register only when SBEN=1

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	Reserved			0		
3	Mask19	Mask off Side-band Disable	RW	0	Side-band shift register may disable the output	Force output to be enabled regardless of side-band shift register value
2	Mask18	Mask off Side-band Disable	RW	0		
1	Mask17	Mask off Side-band Disable	RW	0		
0	Mask16	Mask off Side-band Disable	RW	0		

Byte 11: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q19	Impedance selection of Q19	RW	0	00 or 11 = Nominal	
6	Z1_Q19		RW	0	01=-5%, 10=+5%	
5	Reserved			0		
4	Z0_Q18	Impedance selection of Q18	RW	0	00 or 11 = Nominal	
3	Z1_Q18		RW	0	01=-5%, 10=+5%	
2	Reserved			0		
1	Z0_Q17	Impedance selection of Q17	RW	0	00 or 11 = Nominal	
0	Z1_Q17		RW	0	01=-5%, 10=+5%	

Byte 12: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q16	Impedance selection of Q16	RW	0	00 or 11 = Nominal	
5	Z1_Q16		RW	0	01=-5%, 10=+5%	
4	Reserved			0		
3	Z0_Q15	Impedance selection of Q15	RW	0	00 or 11 = Nominal	
2	Z1_Q15		RW	0	01=-5%, 10=+5%	
1	Reserved			0		
0	Reserved			0		

Byte 13: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q14	Impedance selection of Q14	RW	0	00 or 11 = Nominal	
6	Z1_Q14		RW	0	01=-5%, 10=+5%	
5	Reserved			0		
4	Z0_Q13	Impedance selection of Q13	RW	0	00 or 11 = Nominal	
3	Z1_Q13		RW	0	01=-5%, 10=+5%	
2	Reserved			0		
1	Z0_Q12	Impedance selection of Q12	RW	0	00 or 11 = Nominal	
0	Z1_Q12		RW	0	01=-5%, 10=+5%	

Byte 14: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q11	Impedance selection of Q11	RW	0	00 or 11 = Nominal	
5	Z1_Q11		RW	0	01=-5%, 10=+5%	
4	Reserved			0		
3	Z0_Q10	Impedance selection of Q10	RW	0	00 or 11 = Nominal	
2	Z1_Q10		RW	0	01=-5%, 10=+5%	
1	Reserved			0		
0	Reserved			0		

Byte 15: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q9	Impedance selection of Q9	RW	0	00 or 11 = Nominal	
6	Z1_Q9		RW	0	01=-5%, 10=+5%	
5	Reserved			0		
4	Z0_Q8	Impedance selection of Q8	RW	0	00 or 11 = Nominal	
3	Z1_Q8		RW	0	01=-5%, 10=+5%	
2	Reserved			0		
1	Z0_Q7	Impedance selection of Q7	RW	0	00 or 11 = Nominal	
0	Z1_Q7		RW	0	01=-5%, 10=+5%	

Byte 16: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q6	Impedance selection of Q6	RW	0	00 or 11 = Nominal	
5	Z1_Q6		RW	0	01=-5%, 10=+5%	
4	Reserved			0		
3	Z0_Q5	Impedance selection of Q5	RW	0	00 or 11 = Nominal	
2	Z1_Q5		RW	0	01=-5%, 10=+5%	
1	Reserved			0		
0	Reserved			0		

Byte 17: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Z0_Q4	Impedance selection of Q4	RW	0	00 or 11 = Nominal	
6	Z1_Q4		RW	0	01=-5%, 10=+5%	
5	Reserved			0		
4	Z0_Q3	Impedance selection of Q3	RW	0	00 or 11 = Nominal	
3	Z1_Q3		RW	0	01=-5%, 10=+5%	
2	Reserved			0		
1	Z0_Q2	Impedance selection of Q2	RW	0	00 or 11 = Nominal	
0	Z1_Q2		RW	0	01=-5%, 10=+5%	

Byte 18: Output Impedance Selection Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Z0_Q1	Impedance selection of Q1	RW	0	00 or 11 = Nominal	
5	Z1_Q1		RW	0	01=-5%, 10=+5%	
4	Reserved			0		
3	Z0_Q0	Impedance selection of Q0	RW	0	00 or 11 = Nominal	
2	Z1_Q0		RW	0	01=-5%, 10=+5%	
1	Reserved			0		
0	Reserved			0		

Byte 19: Reserved

Byte 20: Stop State Configuration Register

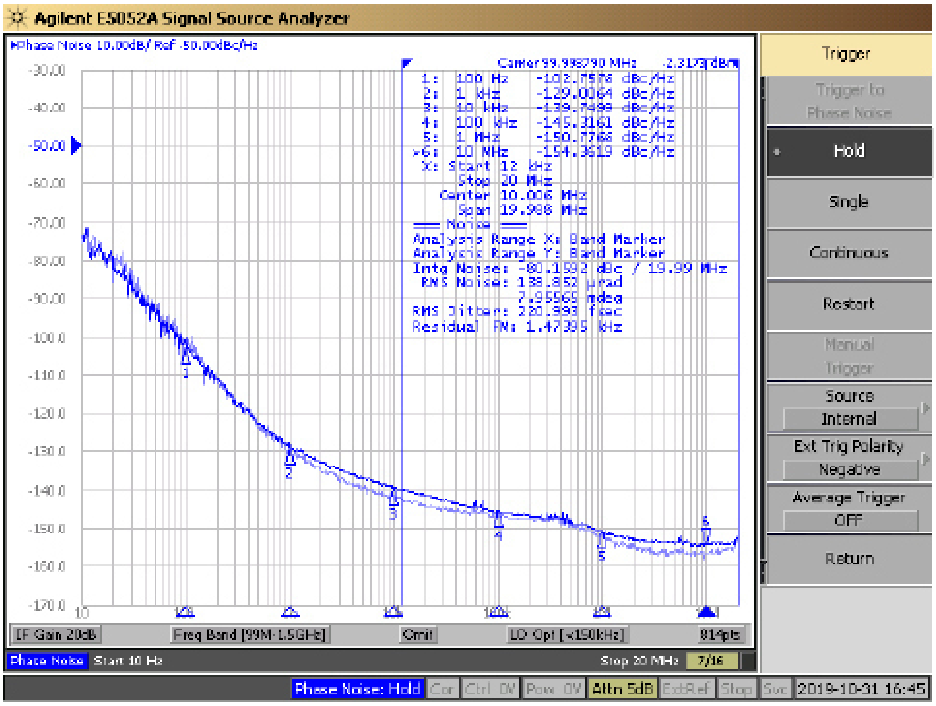
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	VSW[2]	Global differential output swing control	RW	1	Default=750mV	
6	VSW[1]		RW	0	0.3V-1.0V	
5	VSW[0]		RW	1	100mV/Step	
4	Reserved			0		
3	Reserved			0		
2	Reserved			1		
1	STOPST[1]	Differential Stop Mode State	RW	0	00=Low/Low; 10=High/Low	
0	STOPST[0]		RW	0	01=HiZ/HiZ; 11=Low/High	

Byte 21: Power Down Restore Configuration Register

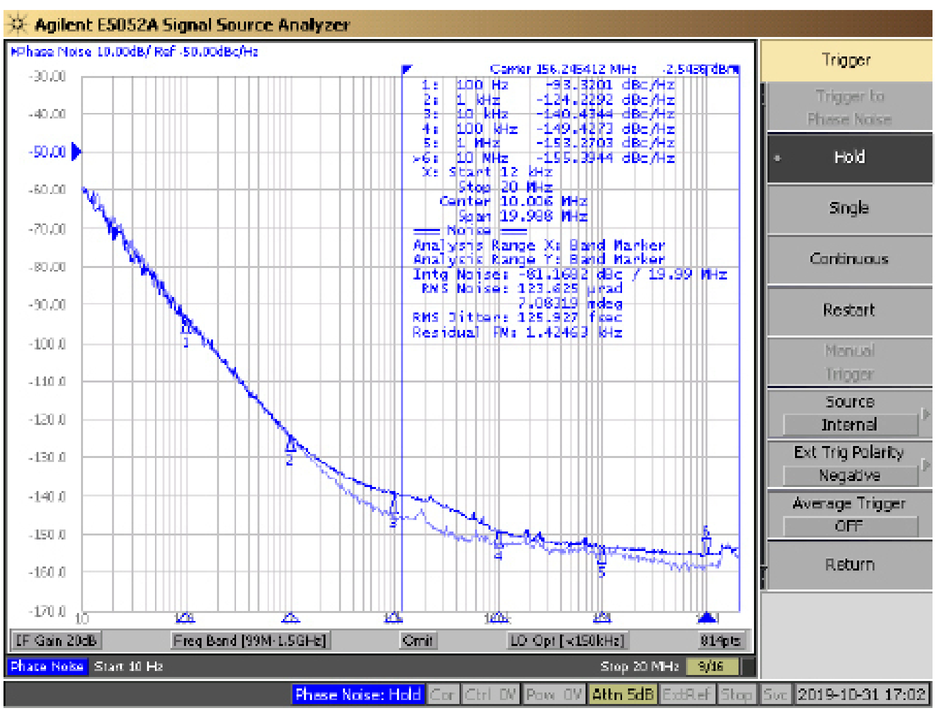
Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	Reserved			0		
3	PD_RESTORE#	Save configuration in power down mode	RW	1	Config cleared	Config saved
2	Reserved			0		
1	Reserved			0		
0	Reserved			0		

Phase Noise Plots

100MHz input phase noise vs output phase noise. Additive jitter[1] 67fs.



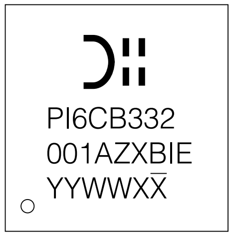
156.25MHz input phase noise vs output phase noise. Additive jitter[1] 51fs.



Note:

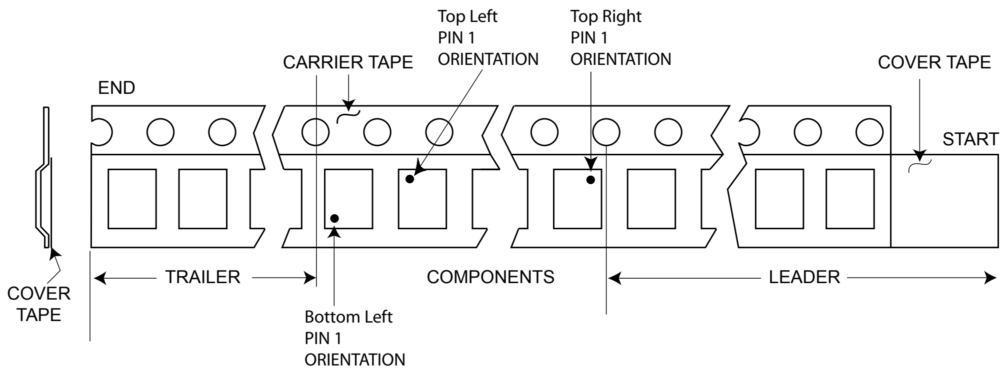
1. Additive jitter RMS value is calculated by the following equation = SQRT [(total jitter)*^{2} - (input jitter)*^{2}]

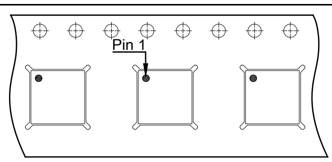
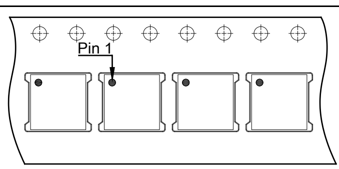
Part Marking



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

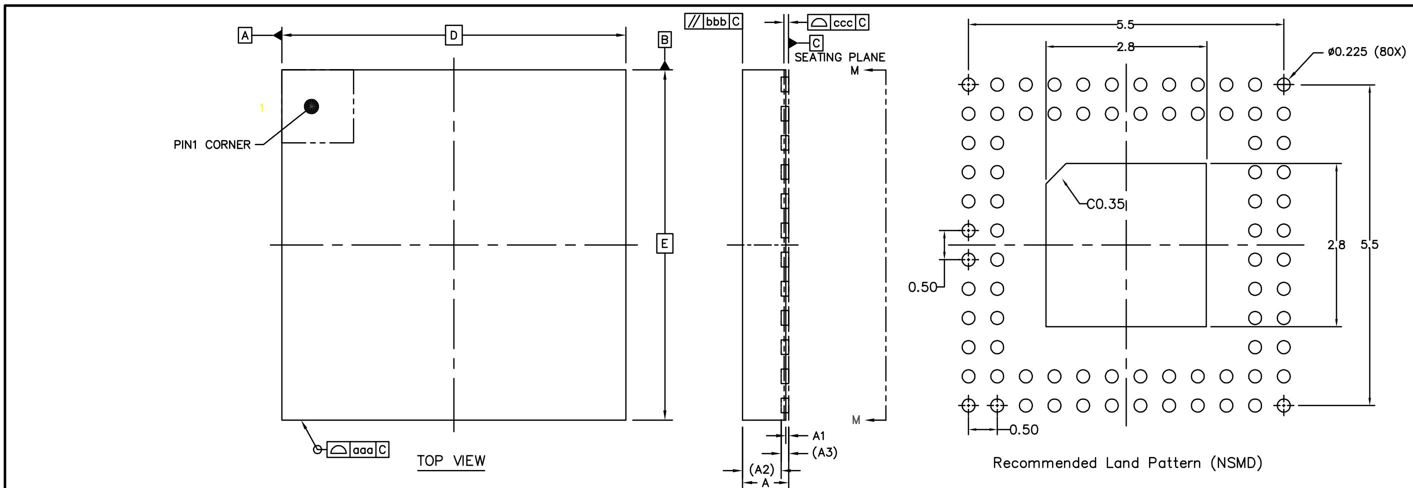
Package Information

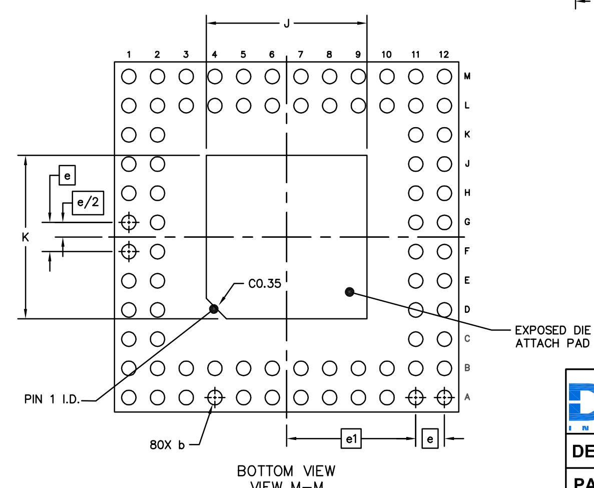


Suffix	Tape Orientation
-13R	
-13RA	

Packaging Mechanical

80-aQFN (ZXB)





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	0.85
STAND OFF		A1	0.02	0.05	0.08
MOLD THICKNESS		A2	0.675 REF		
L/F THICKNESS		A3	0.13 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
LEAD PITCH		e	0.5 BSC		
		e1	2.25 BSC		
EP SIZE	X	J	2.7	2.8	2.9
	Y	K	2.7	2.8	2.9
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.08		
COPLANARITY		ccc	0.08		

NOTES
1.0 DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS, RINGS AND DIE ATTACH PAD AS WELL AS THE TERMINALS.

19-0369

DATE: 07/03/19

DESCRIPTION: 80-contact, Advanced Quad Flat No-Lead (aQFN)

PACKAGE CODE: ZXB (ZXB80)

DOCUMENT CONTROL #: PD-2244 REVISION: --

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description	Pin 1 Location	Tape Pitch
PI6CB332001AZXBIEX	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN)	Top Right Corner	12mm
PI6CB332001AZXBIEX-13R	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN)	Top Left Corner	12mm
PI6CB332001AZXBIEX-13RA	ZXB	80-contact, Advanced Quad Flat No-Lead (aQFN)	Top Left Corner	8mm

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel
7. For packaging detail, go to our website at: https://www.diodes.com/assets/MediaList-Attachments/Diodes-Package-Information.pdf