Features

- Low cost frequency multiplier
- Zero ppm multiplication error
- Input crystal frequency of 5 - 30 MHz
- Input clock frequency of 4 - 50 MHz
- Output clock frequencies up to 180 MHz
- Low period jitter 50ps (100~180MHz)
- Duty cycle of 45/55%
- 9 selectable frequencies controlled by S0, S1 pins
- Operating voltages of 3.0 to 5.5V
- Tri-state output for board level testing

Ordering Information

Part No.	Package
PT7C4501W	SOIC-8
PT7C4501WE	Lead free SOIC-8
PT7C4501AW	SOIC-8
PT7C4501AWE	Lead free SOIC-8

Description

The PT7C4501/4501A is a high performance frequency multiplier, which integrates Analog Phase Lock Loop techniques.

The PT7C4501/4501A is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. It is designed to replace crystal oscillators in most electronic systems, clock multiplier and frequency translation.

Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 180 MHz.

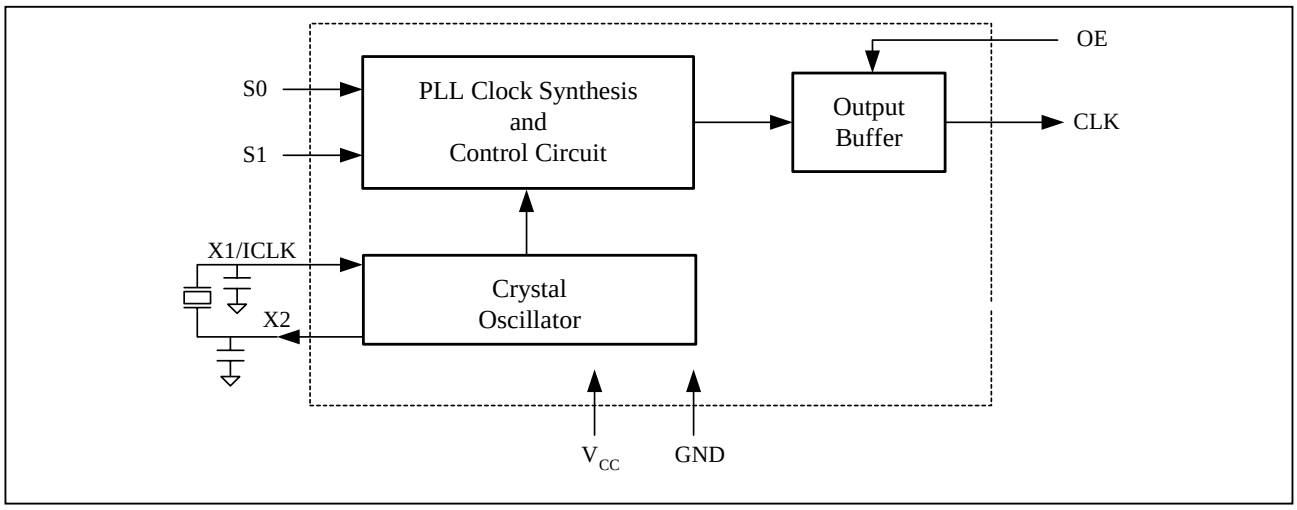
The complex Logic divider is the ability to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

The device also has an Output Enable pin that tri-states the clock output when the OE pin is taken low. This product is intended for clock generation and frequency translation with low output jitter (variation in the output period)

Applications

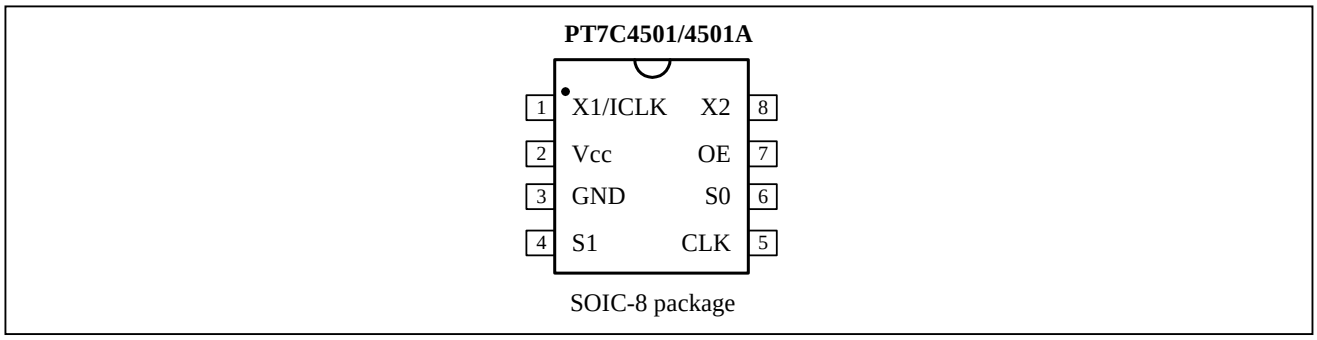
- Clock multiply and frequency translation

Block Diagram



Pin Information

Pin Configration



Pin Description

Pin No.	Pin Name	Type	Description
1	X1/ICLK	I	Crystal connection or clock input.
2	V_{CC}	P	Supply voltage.
3	GND	P	Ground.
4	S1	I	Multiplier select pin 1. Connect to GND or VDD or float (no connection).
5	CLK	O	Clock output.
6	S0	I	Multiplier select pin 0. Connect to GND or VDD or float (no connection).
7	OE	I	Output Enable. Tri-states CLK output when low. Internal pull-up.
8	X2	O	Crystal connection. Leave unconnected for clock input.

Note: XI/XO = crystal connections, TI = tri-level input, O = output, I = input, P = power supply connection

Clock Output Table

S1	S0	CLK	S1	S0	CLK
0	0	×4 [1)]	M	1	×(10/3)
0	M [2)]	×(16/3)	1	0	×6
0	1	×5	1	M	×3
M	0	×2.5	1	1	×8
M	M	×2			

Note 1: CLK output frequency = ICLK × 4.
Note 2: M = leave unconnected (self-biases to Vcc/2).

Common Output Frequencies Example (MHz)

Telecom Application

Output	16.384	32.768	30	38.88	51.2	37.5	32.768	52	60
Input	8.192	16.384	10	19.44	25.6	15	8.192	13	10
Selection (S1,S0)	M,M	M,M	1,M	M,M	M,M	M,0	0,0	0,0	1,0
Output	77.76	72	75	51.84	90	100	155.52	125	180
Input	19.44	12	25	6.48	15	20	19.44	25	30
Selection (S1,S0)	0,0	1,0	1,M	1,1	1,0	0,1	1,1	0,1	1,0
Output	20	24	30	32	33.33	37.5	40	48	60
Input	10	12	10	16	16.66	15	10	12	10
Selection (S1,S0)	M,M	M,M	1,M	M,M	M,M	M,0	0,0	0,0	1,0
Output	64	72	75	80	90	100	120	125	150
Input	16	12	25	10	15	20	15	25	25
Selection (S1,S0)	0,0	1,0	1,M	1,1	1,0	0,1	1,1	0,1	1,0

Note: All of the above outputs are achieved by using a common, inexpensive 10MHz to 30MHz crystal. Consult PTI on how to achieve other output frequencies.

Maximum Ratings

Storage Temperature ..... -65°C to 150°C
Ambient Operation Temperature..... -40°C to 85°C
Supply Voltage to Ground Potential (V_{CC}) ..... -0.3V to 7.0V
Inputs (Referenced to GND)..... -0.5 to Vcc+0.5V
Clock Output (Referenced to GND)..... -0.5 to Vcc+0.5V
Soldering Temperature (Max of 10 seconds)..... 260 °C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Sym	Description	Min	Type	Max	Unit
V_{CC}	Supply voltage	3	-	5.5	V
T_A	Range of operating temperature	-40	-	85	℃

DC Electrical Characteristics

(V_{CC} = 3.3V± 0.3V, T_A= -40~85ºC, unless otherwise noted)

Sym	Parameter	Test Condition	Pin	Min	Typ	Max	Unit
Vcc	Supply Voltage	-	Vcc	3	-	5.5	V
Icc	Supply Current	no load, 20MHz crystal	Vcc	-	12	20	mA
V_{IH}	Input Logic High	-	ICLK	(Vcc/2)+1	Vcc/2	-	V
			OE	2		-	V
V_{IL}	Input Logic Low	-	ICLK	-	Vcc/2	(Vcc/2)-1	V
			OE	-	-	0.8	V
V_{IH}	Input Logic High	-	S0, S1	Vcc-0.5	-	-	V
V_{IM}	Input Mid-level	-	S0, S1	-	Vcc/2	-	V
V_{IL}	Input Logic Low	-	S0, S1	-	-	0.5	V
V_{OH}	High-level output voltage	I_{OH} = -12mA	CLK	2.4	-	-	V
V_{OL}	Low-level output voltage	I_{OL} = 12mA	CLK	-	-	0.4	V
R	Internal pull up resistance	-	OE	-	270	-	kΩ
I_S	Short Circuit Current	-	CLK	-	±70	-	mA
I_{OZ}	Output Leakage Current	-	CLK	-	-	1	μA

AC Electrical Characteristics

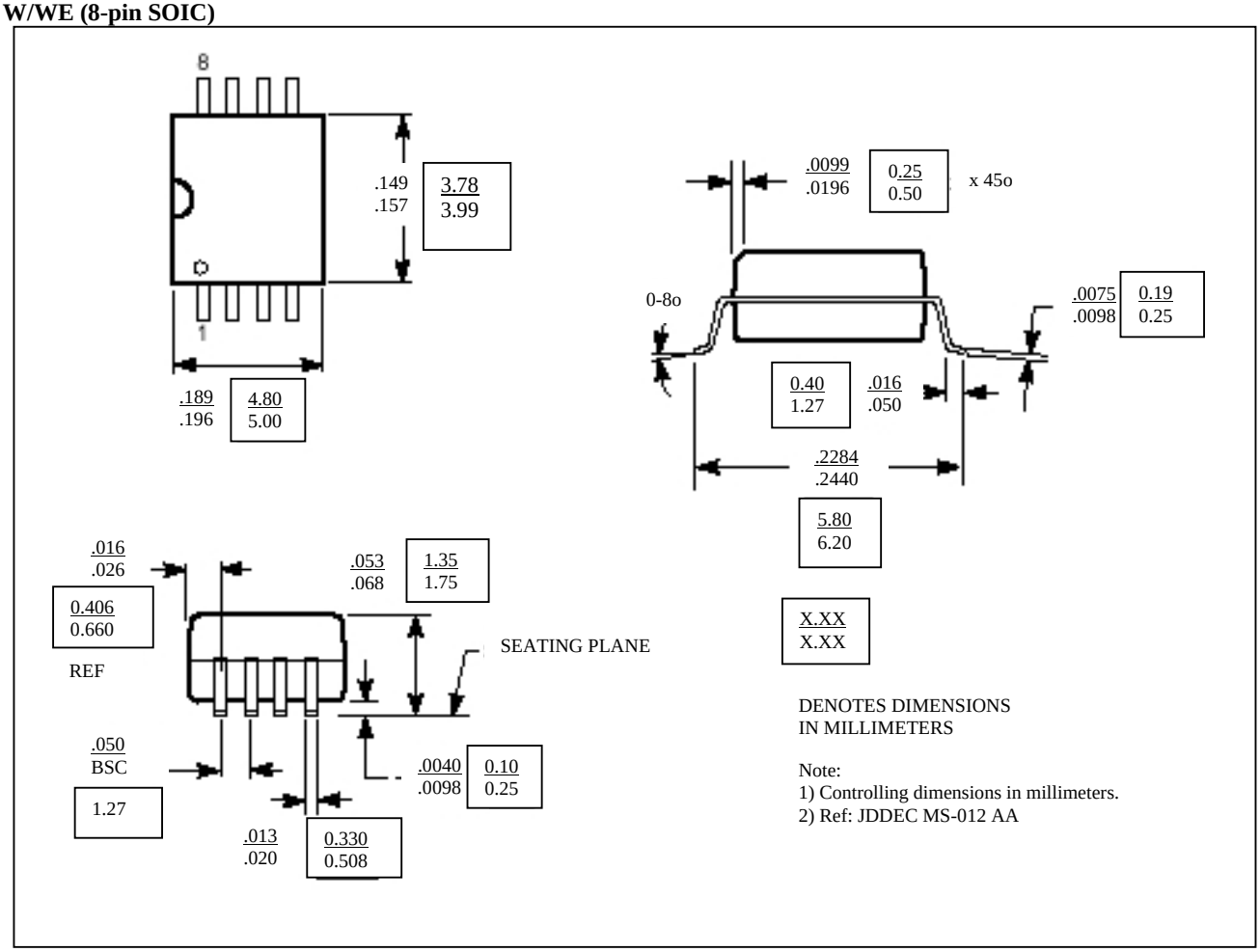
(V_{CC} = 3.3V± 0.3V, T_A= -40~85ºC, unless otherwise noted)

Sym	Parameter	Test Condition	Pin	Min	Typ	Max	Unit
f_{IN}	Input Frequency	crystal	ICLK	5	-	30	MHz
		Clock	ICLK	4	-	50	
f_{OUT}	Output frequency	V_{CC}: 3.0 to 5.5V	CLK(4501)	20	-	180	
		V_{CC}: 3.0 to 5.5V	CLK(4501A)	20	-	150	
t_r	Output clock rise time	0.8 to 2.0V, C_L=15pF	CLK	-	1	-	ns
t_f	Output clock fall time	2.0 to 0.8V, C_L=15pF	CLK	-	1	-	ns
Duty	Output clock duty cycle	At V_{CC}/2	CLK	45	50	55	%
	PLL bandwidth*	-	-	10	-	-	kHz
	Output enable time	OE high to output on	-	-	15	50	ns
	Output disable time	OE low to tri-state	-	-	15	50	ns
	Period Jitter	100MHz~180MHz	CLK(4501)	-	50	100	ps
		100MHz~150MHz	CLK(4501A)	-	50	100	
	Jitter over 200ns interval	100MH~180MHz,	CLK(4501)	-	-	200	ps
		100MH~150MHz	CLK(4501A)	-	-	200	

*__Note:__ Only reference for design.

Mechanical Information

W/WE (8-pin SOIC)



Notes

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