NCP81155

Product Preview

MOSFET Driver

The NCP81155 is a high−performance dual MOSFET gate driver in a small 3 mm x 3 mm package, optimized to drive the gates of both high−side and low−side power MOSFETs in a buck or buck−boost application. VCC UVLO ensures the MOSFETs are off when supply voltages are low. A bi−directional Enable pin provides a fault signal to the controller when a UVLO fault is detected.

Features

- Space−Efficient 3 mm x 3 mm DFN8 Thermally−Enhanced Package
- VCC Range of 4.5 V to 13.2 V
- Integrated Bootstrap Diode
- Compatible with 3.3 V and 5 V PWM Inputs
- Bi−Directional Enable Feature Pulls Enable Pin low during a UVLO Fault.
- Adaptive Anti−Cross Conduction Circuit Protects against Cross−Conduction during FET Turn−on and Turn−off
- Output Disable Control Turns Off Both MOSFETs
- VCC Undervoltage Lockout
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- E−Cigarettes
- Unmanned Aerial Vehicles (UAV)

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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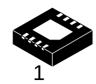
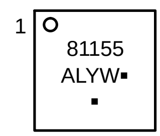


DFN8
MN SUFFIX
CASE 506BJ

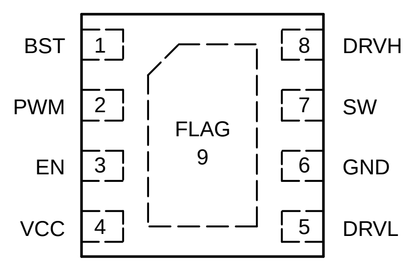
MARKING DIAGRAM



81155	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81155MNTXG	DFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

October, 2017 − Rev. P1
Publication Order Number:
NCP81155/D

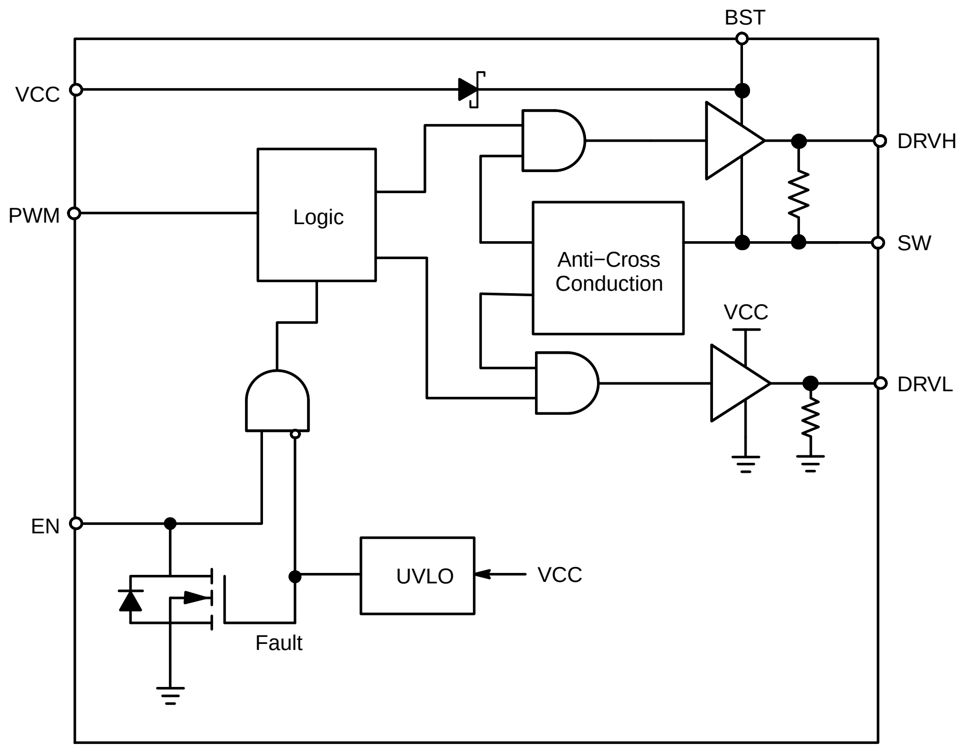


Figure 1. Simplified Block Diagram

Table 1. Pin Descriptions

Pin No.	Symbol	Description
1	BST	Floating bootstrap supply pin for high side gate driver. Connect the bootstrap capacitor between this pin and the SW pin.
2	PWM	Control input: PWM = High − DRVH is high, DRVL is low. PWM = Low − DRVH is low, DRVL is high.
3	EN	Enable input: EN = High − Driver is enabled. EN = Low − Driver is disabled.
4	VCC	Power supply input. Connect a bypass capacitor (0.1 μF) from this pin to ground.
5	DRVL	Low side gate drive output. Connect to the gate of low side MOSFET.
6	GND	Bias and reference ground. All signals are referenced to this node (QFN Flag).
7	SW	Switch node. Connect this pin to the source of the high side MOSFET and drain of the low side MOSFET.
8	DRVH	High side gate drive output. Connect to the gate of high side MOSFET.
9	FLAG	Thermal flag. There is no electrical connection to the IC. Connect to ground plane.

Table 2. ABSOLUTE MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}
VCC	Main Supply Voltage Input	15 V 16 V (< 50 ns)	−0.3 V
BST	Bootstrap Supply Voltage	35 V wrt/ GND 40 V ≤ 50 ns wrt/ GND 15 V wrt/ SW	−0.3 V wrt/SW
SW	Switching Node (Bootstrap Supply Return)	35 V 40 V ≤ 50 ns	−5 V −10 V (200 ns)
DRVH	High Side Driver Output	BST+0.3 V SW + 15 V (< 80 ns)	−0.3 V wrt/SW −2 V (<200 ns) wrt/SW
DRVL	Low Side Driver Output	VCC+0.3 V 15 V (< 80 ns)	−0.3 V DC −5 V (<200 ns)
PWM	DRVH and DRVL Control Input	6.5 V	−0.3 V
EN	Enable Pin	6.5 V	−0.3 V
GND	Ground	0 V	0 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION (All signals referenced to AGND unless noted otherwise)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Characteristic (Note 1)	74	°C/W
T_J	Operating Junction Temperature Range	−40 to 125	°C
T_A	Operating Ambient Temperature Range	−10 to +125	°C
T_{STG}	Maximum Storage Temperature Range	−55 to +150	°C
MSL	Moisture Sensitivity Level	1	

* The maximum package power dissipation must be observed.
1. I in^2 Cu, 1 oz thickness.

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
SUPPLY VOLTAGE					
VCC Operation Voltage		4.5		13.2	V
UNDERVOLTAGE LOCKOUT					
VCC Start Threshold		3.8	4.35	4.5	V
VCC UVLO Hysteresis		150	200	250	mV
SUPPLY CURRENT					
Normal Mode	Icc + Ibst, EN = 5 V, PWM = OSC, Fsw = 100 KHz, Cload = 3 nF for DRVH, 3 nF for DRVL		10		mA
Standby Current	Icc + Ibst, EN = GND		0.5	1.4	mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = LOW, No loading on DRVH & DRVL		2.0		mA
Standby Current	I_{CC} + I_{BST}, EN = HIGH, PWM = HIGH, No loading on DRVH & DRVL		2.0		mA
BOOTSTRAP DIODE					
Forward Voltage	V_{CC} = 12 V, forward bias current = 2 mA	0.1	0.4	0.6	V
PWM INPUT					
PWM Input High		2.0			V
PWM Input Low				0.8	V
HIGH SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current	VBST − VSW = 12 V		1.9	3.0	Ω
Output Impedance, Sinking Current	VBST − VSW = 12 V		1.0	1.7	Ω
DRVH Rise Time trDRVH	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		16	30	ns
DRVH Fall Time tfDRVH	V_{VCC} = 12 V, 3 nF load, VBST−VSW = 12 V		11	25	ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF	8	13	30	ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF			30	ns
DRVH Pull Down Resistance	DRVH to SW, BST−SW = 0 V		37.5		kΩ
HIGH SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current	VBST − VSW = 5 V		2.5		Ω
Output Impedance, Sinking Current	VBST − VSW = 5 V		1.6		Ω
DRVH Rise Time tr_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		30		ns
DRVH Fall Time tf_{DRVH}	V_{VCC} = 5 V, 3 nF load, VBST − VSW = 5 V		27		ns
DRVH Turn−Off Propagation Delay $tpdl_{DRVH}$	C_{LOAD} = 3 nF		20		ns
DRVH Turn−On Propagation Delay $tpdh_{DRVH}$	C_{LOAD} = 3 nF		27		ns
SW Pull Down Resistance	SW to PGND		37.5		kΩ
LOW SIDE DRIVER (VCC = 12 V)					
Output Impedance, Sourcing Current			2.0	3.0	Ω
Output Impedance, Sinking Current			0.7	1.5	Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		16	35	ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		11	20	ns

Table 4. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −10°C < T_A < +125°C; 4.5 V < V_{CC} < 13.2 V, 4.5 V < BST−SWN < 13.2 V, 4.5 V < BST < 30 V, 0 V < SWN < 21 V)

Parameter	Test Conditions	Min.	Typ.	Max.	Units
LOW SIDE DRIVER (VCC = 12 V)					
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF		15	35	ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF	8.0		30	ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		37.5		kΩ
LOW SIDE DRIVER (VCC = 5 V)					
Output Impedance, Sourcing Current			2.5		Ω
Output Impedance, Sinking Current			1.0		Ω
DRVL Rise Time tr_{DRVL}	C_{LOAD} = 3 nF		30		ns
DRVL Fall Time tf_{DRVL}	C_{LOAD} = 3 nF		22		ns
DRVL Turn−Off Propagation Delay $tpdl_{DRVL}$	C_{LOAD} = 3 nF		22		ns
DRVL Turn−On Propagation Delay $tpdh_{DRVL}$	C_{LOAD} = 3 nF		12		ns
DRVL Pull Down Resistance	DRVL to PGND, VCC = PGND		37.5		kΩ
EN INPUT					
Input Voltage High		2.0			V
Input Voltage Low				1.0	V
Hysteresis			500		mV
Normal Mode Bias Current		−1		1	μA
Enable Pin Sink Current		4		30	mA
Propagation Delay Time	PWM = 0 V, EN going from 0 V to EN_{HI} to DRVL rising to 10%		20	40	ns
SW Node					
SW Node Leakage Current				20	μA

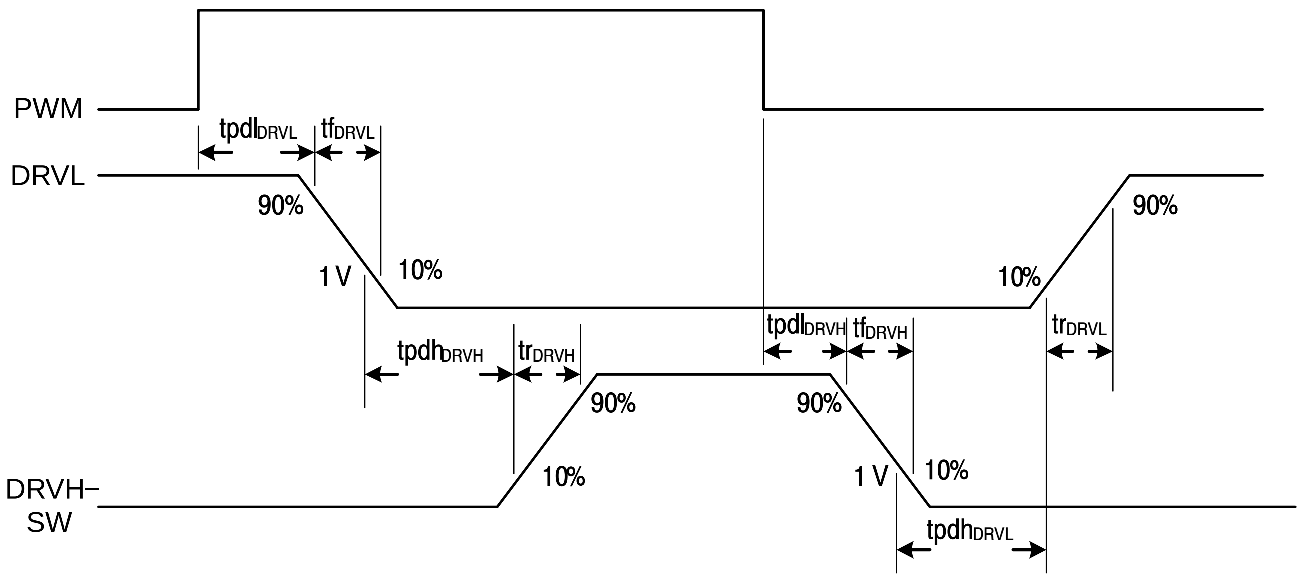


Figure 2. Gate Timing Diagram

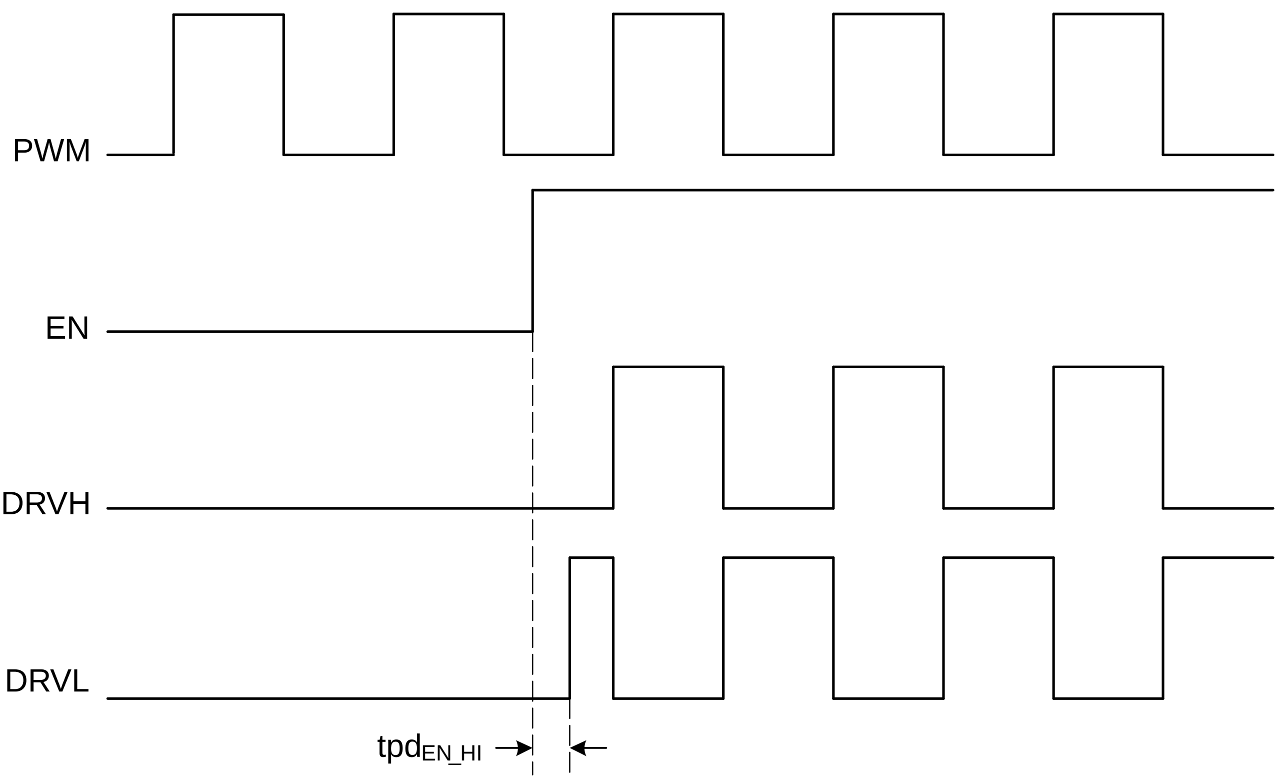


Figure 3. PWM/EN Logic Diagram

APPLICATIONS INFORMATION

The NCP81155 gate driver is a MOSFET driver designed for driving two N−channel MOSFETs in a synchronous buck or buck−boost topology.

Low−Side Driver

The low−side driver is designed to drive a ground referenced low $R_{DS(on)}$ N−channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCC and GND pins.

High−Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the SW pin.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor. When the NCP81155 is starting up, the SW pin is held at ground, allowing the bootstrap capacitor to charge up to VCC through the bootstrap diode. When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the SW pin rises. When the high−side MOSFET is fully turned on, SW will settle to VIN and BST will settle to VIN + VCC (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used for C_{BST}.

Power Supply Decoupling

The NCP81155 can source and sink relatively large currents to the gate pins of the MOSFETs. In order to maintain a constant and stable supply voltage, a low−ESR capacitor should be placed near the VCC and GND pins. A MLCC between 1 μF and 4.7 μF is typically used.

Undervoltage Lockout

DRVH and DRVL are low until VCC reaches the VCC UVLO threshold, typically 4.35 V. Once VCC reaches this threshold, the PWM signal will control DRVH and DRVL. There is a 200 mV hysteresis on VCC UVLO. There are pull−down resistors on DRVH and DRVL to prevent the gates of the MOSFETs from accumulating enough charge to turn on when the driver is powered off.

Bi−Directional EN Signal

The Enable pin (EN) is used to disable the DRVH and DRVL outputs to prevent power transfer. When EN is above the EN_{HI} threshold, DRVH and DRVL change their states according to the PWM input. A UVLO fault turns on the internal MOSFET that pulls the EN pin towards ground. By connecting EN to the DRON pin of a controller, the controller is alerted when the driver encounters a fault condition.

PWM Input

Switching PWM between logic−high and logic−low states will allow the driver to operate in continuous conduction mode as long as VCC is greater than the UVLO threshold and EN is high. The threshold limits are specified in the electrical characteristics table in this datasheet. Refer to Figure 2 for the gate timing diagrams.

When PWM is set above PWM_{HI}, DRVL will first turn off after a propagation delay of $tpdl_{DRVL}$. To ensure non−overlap between DRVL and DRVH, there is a delay of $tpdh_{DRVH}$ from the time DRVL falls to 1 V, before DRVH is allowed to turn on.

When PWM falls below PWM_{LO}, DRVH will first turn off after a propagation delay of $tpdl_{DRVH}$. To ensure non−overlap between DRVH and DRVL, there is a delay of $tpdh_{DRVL}$ from the time DRVH – SW falls to 1 V, before DRVL is allowed to turn on.

Thermal Considerations

As power in the NCP81155 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP81155 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP81155 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

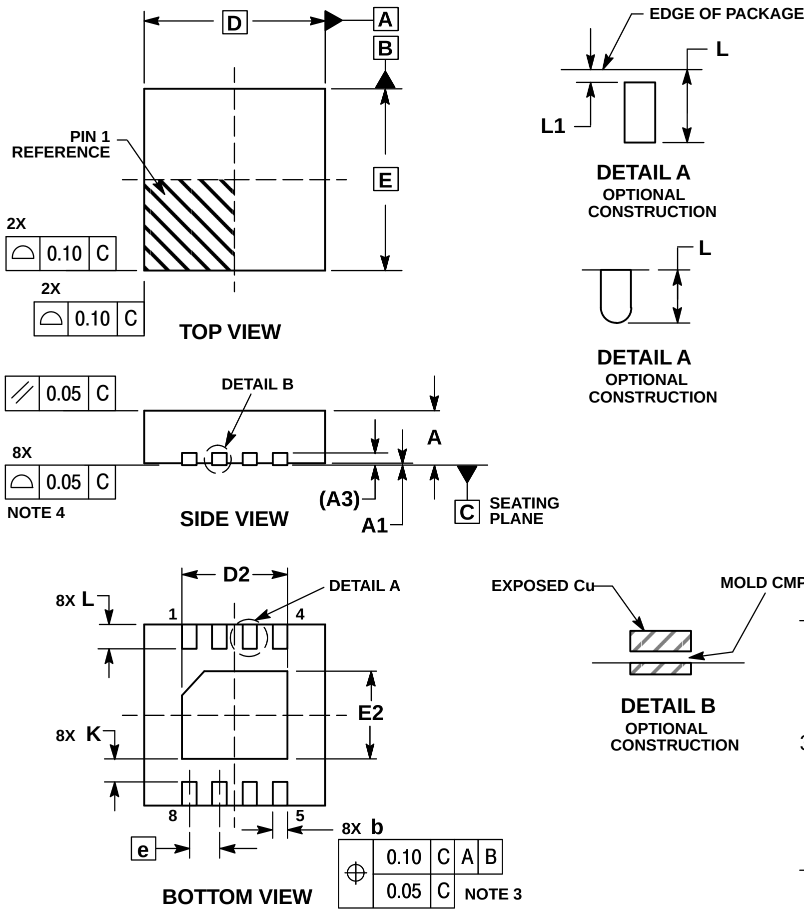
Since T_J is not recommended to exceed 150°C, the NCP81155, soldered on to a 645 mm^2 copper area, using 1 oz. copper and FR4, can dissipate up to 2.3 W when the ambient temperature (T_A) is 25°C. The power dissipated by the NCP81155 can be calculated from the following equation:

$$P_D \approx V_{CC} \times [(n_{HS} \times Qg_{HS} + n_{LS} \times Qg_{LS}) \times f + I_{standby}] \quad \text{(eq. 2)}$$

Where n_{HS} and n_{LS} are the number of high−side and low−side FETs, respectively, Qg_{HS} and Qg_{LS} are the gate charges of the high−side and low−side FETs, respectively and *f* is the switching frequency of the converter.

PACKAGE DIMENSIONS

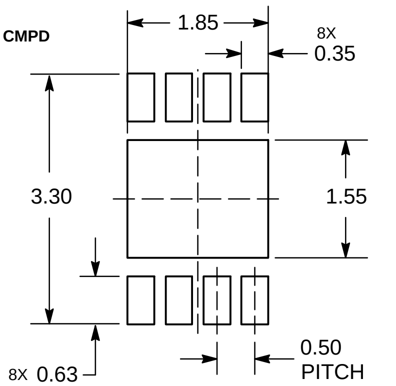
DFN8 3x3, 0.5P
CASE 506BJ
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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