

Field Programmable Crystal Oscillator

Series:CPPL

Features

- Programmed in the field with the PG-3200 oscillator programming instrument within seconds.
- Factory Programmable
- Can be programmed twice
- Standard Package Options
- Ultra low jitter @ 1 million samples

Applications

Driving A/Ds, D/As, FPGAs
 Digital Video
 Ethernet, GbE
 Medical
 Storage Area Networking
 COTS
 Broad Band Access
 SONET/ SDH/ DWDM
 Test & Measurement



MSL: 1

Part Numbering Example:

CPPL C 1 L Z A5 B6 xxx.xxxx TS

SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPL	C=CMOS	1 = Full Size	Blank=5.0V	Blank=Cut Tape	Blank=0°C ~ +70°C	B6=±100ppm	0.500~133.000MHz	TS=Tri-State
	T=TTL	4 = Half Size	L=3.3V	B=Bulk	A3=-55°C ~ +125°C	BP=±50ppm		PD=PowerDwn
		5 = 5X3.2 Ceramic	R=2.7V	T=Tube	A5=-20°C ~ +70°C	BR=±25ppm		
		7 = 5X7 Ceramic		Z=Tape and Reel	A7=-40°C ~ +85°C			

Specifications:

Description	Min	Typ	Max	Unit
Frequency Range: Programmable to any discrete frequency	0.500		133	MHz
Available Stability Options:	-100 -50 -25		+100 +50 +25	PPM
Programmable Supply Voltage:				V
	(1-133 MHz)	4.5	5.0	5.5
	(1-100 MHz)	3.0	3.3	3.6
	(1-66.0 MHz)	2.5	2.7	3.0
Operating Temperature Range Options:	-55 -20 -40		+125 +70 +85	°C
Storage Temperature:	-55		+125	°C
Aging: Ta=°25C, Vdd=5V/3.3V			±5	PPM/Year

Programmable Output Level:

CMOS/TTL

Operating Conditions:

Description	Min	Max	Unit
V_{DD} Supply Voltage	2.7	5.5	V
C_{TTL} Max capacitive load on outputs for TTL levels 4.5V-5.5V V _{DD} , ≤ 40 MHz 4.5V-5.5V V _{DD} , 40 - 133 MHz		50 25	pF pF
C_{CMOS} Max capacitive load on outputs for CMOS levels 4.5V-5.5V V _{DD} , ≤ 66 MHz 4.5V-5.5V V _{DD} , 66 - 133 MHz 3.0V-3.6V V _{DD} , ≤ 40 MHz 3.0V-3.6V V _{DD} , 40 - 100 MHz 2.5-3.0V V _{DD} , ≤ 66 MHz		50 25 30 15 25	pF pF pF pF pF



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Output Clock Switching Characteristics:

Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle: TTL @ 1.4V 4.5-5.5 V _{DD}	≤ 50 MHz, C _L = 50 pF	45	-	55	%
	50 - 66 MHz, C _L = 15 pF	45	-	55	%
	66 - 125 MHz, C _L = 25 pF	40	-	60	%
	125 - 133 MHz, C _L = 15 pF	40	-	60	%
Duty Cycle: CMOS @ V _{DD} /2 4.5-5.5 V _{DD} 3.0-3.6 V _{DD}	≤ 66 MHz, C _L ≤ 25 pF	45	-	55	%
	66 - 125 MHz, C _L ≤ 25 pF	40	-	60	%
	125 - 133 MHz, C _L ≤ 15 pF	60	-	60	%
	≤ 40 MHz, C _L ≤ 30 pF	45	-	55	%
	40 - 100 MHz, C _L ≤ 15 pF	40	-	60	%
Rise/Fall:	0.8V - 2.0V, 4.5 - 5.5 V _{DD} , C _L = 50 pF			1.8	ns
	0.8V - 2.0V, 4.5 - 5.5 V _{DD} , C _L = 25 pF			1.2	ns
	0.8V - 2.0V, 4.5 - 5.5 V _{DD} , C _L = 15 pF			0.9	ns
	0.2V - 0.8 * V _{DD} , 4.5 - 5.5 V _{DD} , C _L = 50 pF			3.4	ns
	0.2V - 0.8 * V _{DD} , 3.0 - 3.6 V _{DD} , C _L = 30 pF			4.0	ns
	0.2V - 0.8 * V _{DD} , 3.0 - 3.6 V _{DD} , C _L = 15 pF			2.4	ns
Start Up Time	From Power On	-	-	2	ms
Power Down Delay Time Synchronous Asynchronous	PWR_DOWN pin LOW to output Hi-Z, T = Frequency Oscillator Period		T/2	T+10	ns
			10	15	ns
Output Disable Time Synchronous Asynchronous	OE pin LOW to output Hi-Z, T = Frequency Oscillator Period		T/2	T+10	ns
			10	15	ns
Output Enable Time	T = Frequency Oscillator Period		T	1.5*T+25	ns
RMS Period Jitter	1-133.00 MHz		8	11	ps
Peak to Peak*	≤ 33.000 MHz		65	99	ps
	> 33.000 MHz		65	80	ps

* Jitter Tested at > 1,000,000 samples, exceeding JEDEC std JESD65

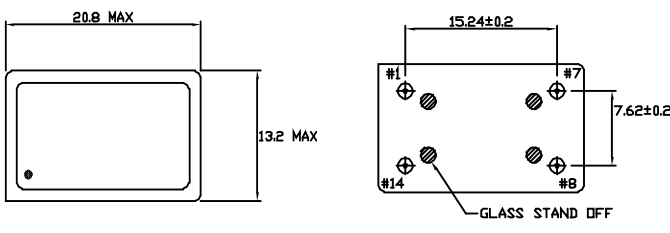
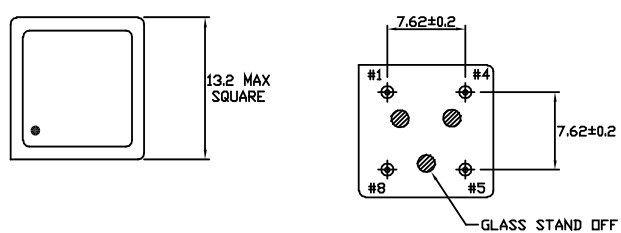
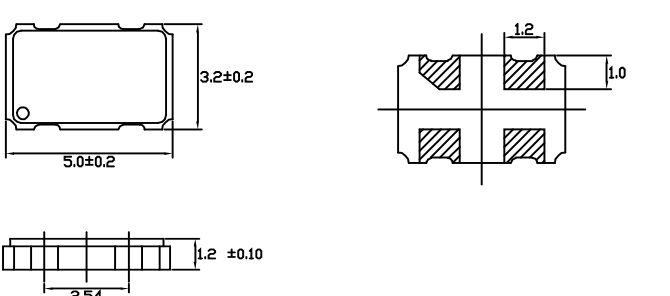
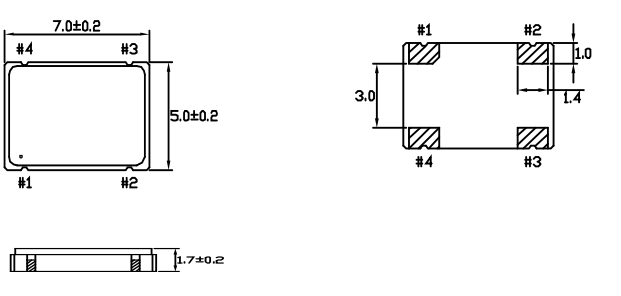
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Electrical Characteristics:

Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V _{IL} , Low-Level Input Voltage (To Tri-State or Power Down)	V _{DD} = 5.0 V	-	-	0.8	V
	V _{DD} = 3.3 V	-	-	0.2 * V _{DD}	V
	V _{DD} = 2.7 V	-	-	0.2 * V _{DD}	V
V _{IH} , High-Level Input Voltage (To Enable Output or Open)	V _{DD} = 5.0 V	2.0	-	-	V
	V _{DD} = 3.3 V	0.7 * V _{DD}	-	-	V
I _{IL} , Input Low Current	V _{IN} = 0 V	-	-	10	μA
I _{IH} , Input High Current	V _{IN} = V _{DD}	-	-	5	μA
Output Characteristics:					
V _{OL} , Low-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = 16mA	-	-	0.4	V
	V _{DD} = 3.3 V, I _{OL} = 8mA	-	-	0.4	V
V _{IHTTL} , High-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = -16mA	2.4	-	-	V
V _{IHCMOS} , High-Level Output Voltage	V _{DD} = 5.0 V, I _{OL} = -16mA	V _{DD} -0.4	-	-	V
	V _{DD} = 3.3 V, I _{OL} = -8mA	V _{DD} -0.4	-	-	V
Power Supply Current: (Unloaded)	V _{DD} = 5.0 V, F _O ≤ 133 MHz	-	-	45	mA
	V _{DD} = 3.3 V, F _O ≤ 100 MHz	-	-	25	mA
	V _{DD} = 2.7 V, F _O ≤ 66.0 MHz	-	-	20	mA
Standby Current:		-	10	50	μA
Tri-State Leakage Current	V _{DD} = 5.0 V	-	20	-	μA
Output Enable Mode:	Output is Tri-Stated				
Power Down Mode:	Output is Tri-Stated				

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*Note: **REQUIRED** Bypass V_{DD} to GND with a $0.01\mu\text{F}$ capacitor

Style 1 Full Size 14 pin DIP	Style 4 Half Size 8 pin DIP																				
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