

# Failsafe™ 2.5 V/3.3 V Zero Delay Buffer

## Features

- Internal digital controlled crystal oscillator (DCXO) for continuous glitch-free operation
- Zero input-output propagation delay
- Low jitter (35 ps max RMS) outputs
- Low output-to-output skew (200 ps max)
- 4.17 MHz to 166.7 MHz reference input
- Supports industry standard input crystals
- 166.7 MHz outputs
- 5 V tolerant Inputs
- Phase-locked loop (PLL) bypass mode
- Dual reference inputs
- 16-Pin thin shrunk small outline package (TSSOP)
- 2.5 V or 3.3 V output power supplies
- 3.3 V core power supply
- Industrial temperature range

## Functional Description

The CY23FS04 is a FailSafe™ zero delay buffer with two reference clock inputs and four phase-aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

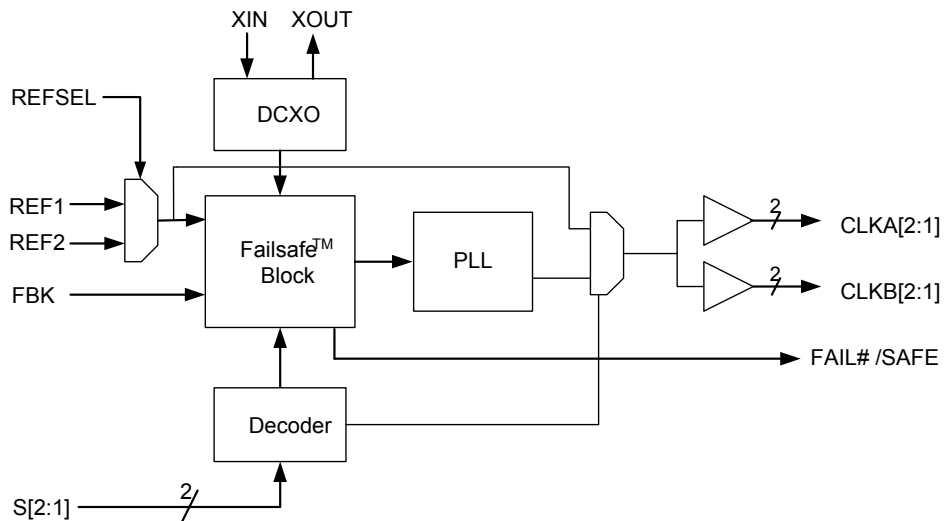
The continuous, glitch-free operation is achieved by using a DCXO. This serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS04 is that the DCXO is the primary clocking source, which is synchronized (phase-aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal that is connected to the DCXO must be an integer factor of the frequency of the reference clock. This factor is set by two select lines: S[2:1], see [Configuration Table](#) on page 3. The output power supply V<sub>DD</sub> can be connected to either 2.5 V or 3.3 V. VDDC is the power supply pin for internal circuits and must be connected to 3.3 V.

For a complete list of related documentation, click [here](#).

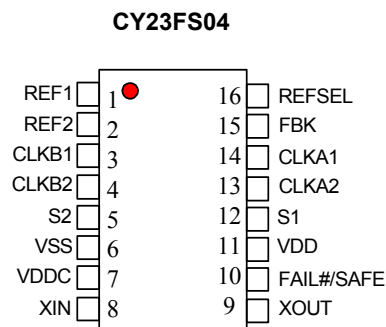
## Logic Block Diagram



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## Pin Configuration

**Figure 1. 16-pin TSSOP pinout**


## Pin Definitions

Pin No.	Pin Name	Description
2, 1	REF[2:1]	Reference clock inputs. 5 V tolerant. <sup>[4]</sup>
4, 3	CLKB[2:1]	Bank B clock outputs. <sup>[1,2]</sup>
13, 14	CLKA[2:1]	Bank A clock outputs. <sup>[1,2]</sup>
15	FBK	Feedback input to the PLL. <sup>[1,4]</sup>
5, 12	S[2:1]	Frequency select pins and PLL and DCXO bypass mode. <sup>[3]</sup>
8	XIN	Reference crystal input.
9	XOUT	Reference crystal output.
10	FAIL#/SAFE	Valid reference indicator. A high level indicates a valid reference input.
11	VDD	2.5 V or 3.3 V power supply.
7	VDDC	3.3 V power supply.
6	VSS	Ground.
16	REFSEL	Reference select. Selects the active reference clock from either REF1 or REF2. REFSEL = 1, REF1 is selected; REFSEL = 0, REF2 is selected.

## Configuration Table

S[2:1]	XTAL (MHz)		REF (MHz)		OUT (MHz)		REF:OUT Ratio	REF:XTAL Ratio	Out:XTAL Ratio
	Min	Max	Min	Max	Min	Max			
00			PLL and DCXO Bypass Mode						
01	8.33	30.00	4.17	15.00	4.17	15.00	x1	1/2	1/2
10	8.00	25.00	16.00	50.00	16.00	50.00	x1	2	2
11	8.33	27.78	50.00	166.70	50.00	166.70	x1	6	6

### Notes

- For normal operation, connect either one of the four clock outputs to the FBK input.
- Weak pull-downs on all outputs.
- Weak pull-ups on these inputs.
- Weak pull-down on these inputs

## FailSafe Function

The CY23FS04 is targeted at clock distribution applications that require continued operation should the main reference clock fail. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods to switch between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another, often requiring complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL, greatly simplifying system design.

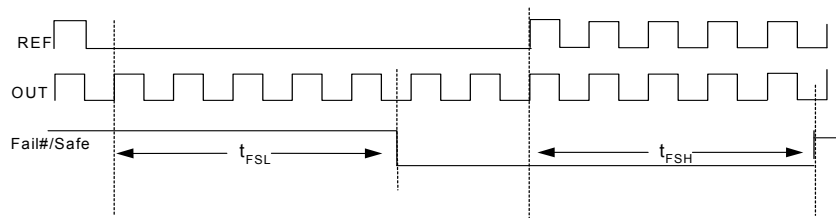
The CY23FS04 PLL is driven by the crystal oscillator, which is phase-aligned to an external reference clock so that the output of the device is effectively phase-aligned to the reference via the external feedback loop. This is accomplished by using a digitally

controlled capacitor array to pull the crystal frequency over an approximate range of  $\pm 300$  ppm from its nominal frequency.

In this mode, if the reference frequency fails (stop or disappear), the DCXO maintains its last setting and a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS04 provides two select bits, S1 and S2, to control the reference-to-crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared, indicating to the system that the selected reference is valid.

**Figure 2. Fail#/Safe Timing for Input Reference Failing Catastrophically**



**Figure 3. Fail#/Safe Timing Formula**

$$t_{FSL(max)} = 2 ( t_{REF} \times n ) + 25 ns$$

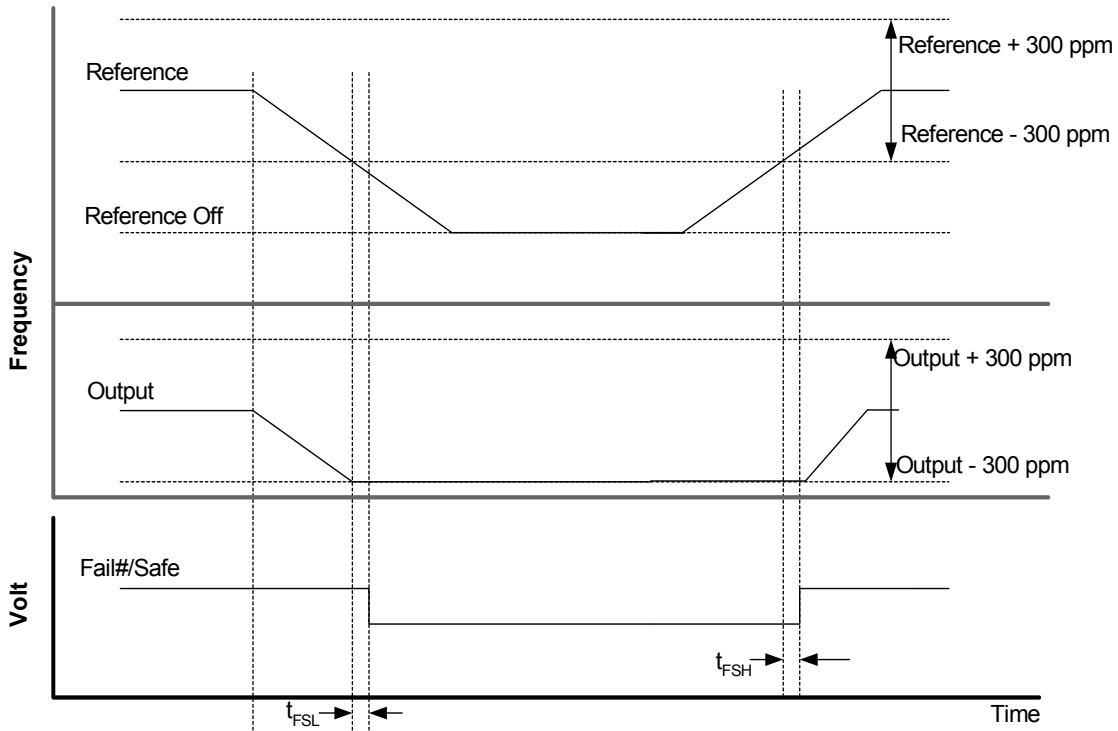
$$n = \frac{F_{REF}}{F_{XTAL}} = 4 \text{ (in above example)}$$

$$t_{FSH(min)} = 12 ( t_{REF} \times n ) + 25 ns$$

**Table 1. FailSafe Timing Table**

Parameter	Description	Conditions	Min	Max	Unit
t <sub>FSL</sub>	Fail#/safe assert delay	Measured at 80% to 20%, Load = 15 pF	–	See Figure 3 on page 4	ns
t <sub>FSH</sub>	Fail#/safe assert delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3 on page 4	–	ns

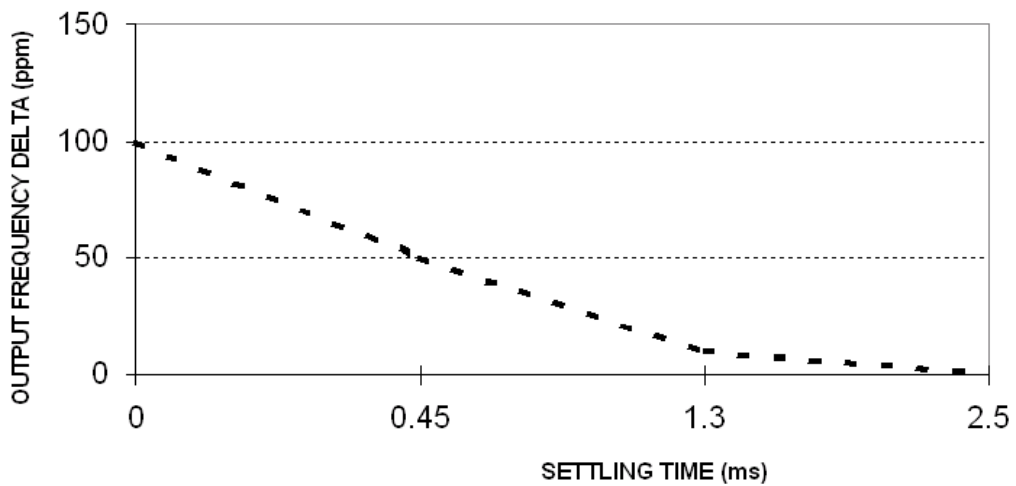
**Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range**



**Figure 5. FailSafe Reference Switching Behavior**

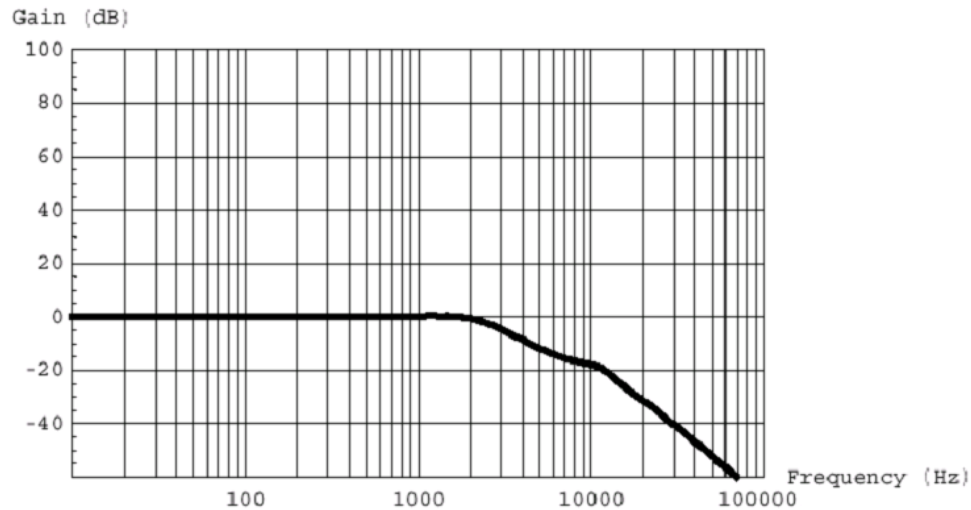
**Failsafe typical frequency settling time**

Initial valid Ref1=20MHz +100ppm,  
then switching to REF2=20MHz



Because of the DCXO architecture, the CY23FS04 has a much lower bandwidth than a typical PLL-based clock generator. This is shown in Figure 6. This low bandwidth makes the CY23FS04 also useful as a jitter attenuator. The loop bandwidth curve is also known as the jitter transfer curve.

Figure 6. FailSafe Effective Loop Bandwidth (min)



### XTAL Selection Criteria and Application Example

Choosing the appropriate XTAL ensures the FailSafe device is able to span an appropriate frequency of operation. Also, the XTAL parameters determine the holdover frequency stability. Critical parameters are given here. Cypress recommends that you choose:

- Low C0/C1 ratio (240 or less) so that the XTAL has enough range of pullability
- Low temperature frequency variation
- Low manufacturing frequency tolerance
- Low aging

C0 is the XTAL shunt capacitance (3 pF to 7 pF typ).

C1 is the XTAL motional capacitance (10 fF to 30 fF typ).

The capacitive load as “seen” by the XTAL is across its terminals. It is named C<sub>LOADMIN</sub> (for minimum value), and C<sub>LOADMAX</sub> (for maximum value). These are used to calculate the pull range.

Note that the C<sub>LOAD</sub> range “center” is approximately 20 pF, but you may not want a XTAL calibrated to that load. This is because the pullability is not linear, as represented in the equation. Plotting the pullability of the XTAL shows this expected behavior as shown in Figure 7 on page 7. In this example, specifying a XTAL calibrated to 16 pF load provides a balanced ppm pullability range around the nominal frequency.

#### Example

$$C_{LOADMIN} = (12 \text{ pF IC input cap} + 0 \text{ pF pulling cap} + 6 \text{ pF trace cap on board}) / 2 = 9 \text{ pF}$$

$$C_{LOADMAX} = (12 \text{ pF IC input cap} + 48 \text{ pF pulling cap} + 6 \text{ pF trace cap on board}) / 2 = 33 \text{ pF}$$

$$\text{Pull Range} = (f_{C_{LOADMIN}} - f_{C_{LOADMAX}}) / f_{C_{LOADMIN}} = (C1 / 2) * [(1 / (C0 + C_{LOADMIN})) - (1 / (C0 + C_{LOADMAX}))]$$

$$\text{Pull Range in ppm} = (C1 / 2) * [(1 / (C0 + C_{LOADMIN})) - (1 / (C0 + C_{LOADMAX}))] * 10^6$$

Figure 7. Frequency vs.  $C_{LOAD}$  Behavior for Example XTAL

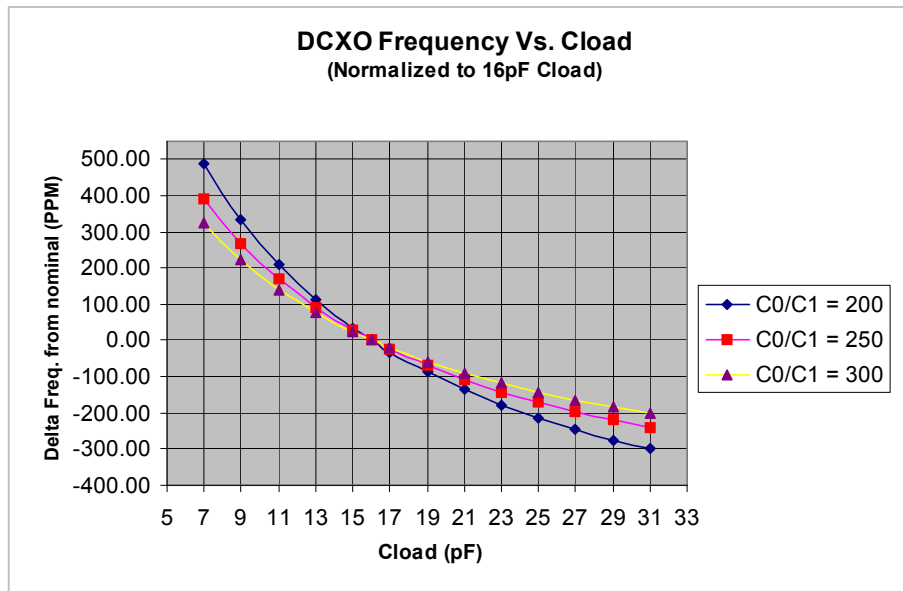


Table 2. Pullability Range from XTAL with Different  $C_0/C_1$  Ratio

$C_L$ (pF)	Calculated Pull Range in ppm, (Normalized)		
	$C_0/C_1 = 200$	$C_0/C_1 = 250$	$C_0/C_1 = 300$
7	489.13	391.30	326.09
9	332.88	266.30	221.92
11	211.35	169.08	140.90
13	114.13	91.30	76.09
15	34.58	27.67	23.06
16	0.00	0.00	0.00
17	-31.70	-25.36	-21.14
19	-87.79	-70.23	-58.53
21	-135.87	-108.70	-90.58
23	-177.54	-142.03	-118.36
25	-213.99	-171.20	-142.66
27	-246.16	-196.93	-164.11
29	-274.76	-219.81	-183.17
31	-300.34	-240.27	-200.23

Calculated value of the pullability range for the XTAL with  $C_0/C_1$  ratio of 200, 250, and 300 are shown in Table 2 on page 7. For this calculation,  $C_{LOADADMIN} = 7$  pF and  $C_{LOAD(max)} = 31$  pF is used. Using a XTAL that has a nominal frequency specified at load capacitance of 16 pF, almost symmetrical pullability range is obtained.

Next, it is important to calculate the pullability range including error tolerances. This is the capture range of the input reference frequency that the FailSafe device and XTAL combination can reliably span.

Calculating the capture range involves subtracting error tolerances as follows:

Parameter.....	f error (ppm)
Manufacturing frequency tolerance .....	15
Temperature stability .....	30
Aging .....	3
Board/trace variation .....	5
Total .....	53

Example: Capture range for XTAL with  $C_0/C_1$  Ratio of 200

Negative Capture range =  $-300$  ppm + 53 ppm =  $-247$  ppm

Positive Capture range =  $489$  ppm – 53 ppm =  $+436$  ppm

It is important to note that the XTAL with lower  $C_0/C_1$  ratio has wider pullability/capture range as compared to the higher  $C_0/C_1$  ratio. This helps to select the appropriate XTAL for use in the FailSafe application.

**Important Notes**

Following are some important notes that should be considered when designing with the failsafe device:

1. The trace capacitance of the XTAL inputs, XIN and XOUT must be kept as small as possible.
2. Specify the DCXO for  $C_0/C_1$  ratio to be less than 250 and the XTAL Load Capacitance to be approximately 16 pF. A typical DCXO specification from Ecliptek is attached here (please see page 6) for reference.
3. XTAL with low temperature frequency variation, low manufacturing frequency tolerance and low aging must be chosen.
4. Pull range must be checked for its upper and lower frequency symmetry from the nominal value as described in this application note.

## Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Supply voltage	–	–0.5	4.6	V
V <sub>IN</sub>	Input voltage	Relative to V <sub>SS</sub>	–0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	temperature, storage	Non functional	–65	150	°C
T <sub>J</sub>	temperature, junction	Functional	–	125	°C
ESD <sub>HBM</sub>	ESD protection (human body model)	MIL-STD-883, Method 3015	2000	–	V
UL–94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level	–	3		

**Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

## Recommended Pullable Crystal Specifications

Parameter <sup>[5]</sup>	Description	Comments	Min	Typ	Max	Unit
F <sub>NOM</sub>	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8.00	–	30.00	MHz
C <sub>LOADNOM</sub>	Nominal load capacitance		–	14	–	pF
R <sub>1</sub>	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R <sub>3</sub> /R <sub>1</sub>	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R <sub>1</sub> values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F <sub>3SEPLI</sub>	Third overtone separation from 3*F <sub>NOM</sub>	High side	300	–	–	ppm
F <sub>3SEPLO</sub>	Third overtone separation from 3*F <sub>NOM</sub>	Low side	–	–	–150	ppm
C <sub>0</sub>	Crystal shunt capacitance	–	–	–	7	pF
C <sub>0</sub> / C <sub>1</sub>	Ratio of shunt to motional capacitance	–	180	–	250	
C <sub>1</sub>	Crystal motional capacitance	–	14.4	18	21.6	fF

### Note

5. Ecliptek ECX-5788-13.500M, ECX-5807-19.440M, ECX-5872-19.53125M, ECX-6362-18.432M, ECX-5808-27.000M, ECX-5884-17.664M, ECX-5883-16.384M, ECX-5882-19.200M, ECX-5880-24.576M meet these specifications.



## Operating Conditions

For FailSafe Devices

Parameter	Description	Min	Max	Unit
V <sub>DDC</sub>	3.3 V supply voltage	3.135	3.465	V
V <sub>DD</sub>	2.5 V supply voltage range	2.375	2.625	V
	3.3 V supply voltage range	3.135	3.465	V
T <sub>A</sub>	Ambient operating temperature, Commercial	0	70	°C
	Ambient operating temperature, Industrial	-40	85	°C
C <sub>L</sub>	Output load capacitance (F <sub>out</sub> ≤ 100 MHz)	-	30	pF
	Output load capacitance (F <sub>out</sub> > 100 MHz)	-	15	pF
C <sub>IN</sub>	Input capacitance (except XIN)	-	7	pF
C <sub>XIN</sub>	Crystal input capacitance (all internal caps off)	10	13	pF
T <sub>PU</sub>	Power-up time for all V <sub>DD</sub> s to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

## Electrical Characteristics

For FailSafe Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage	CMOS Levels, 30% of V <sub>DD</sub>	-	-	0.3 × V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage	CMOS Levels, 70% of V <sub>DD</sub>	0.7 × V <sub>DD</sub>	-	-	V
I <sub>IL</sub>	Input low current	V <sub>IN</sub> = V <sub>SS</sub> (100k pull up only)	-	-	50	μA
I <sub>IH</sub>	Input high current	V <sub>IN</sub> = V <sub>DD</sub> (100k pull down only)	-	-	50	μA
I <sub>OL</sub>	Output low current	V <sub>OL</sub> = 0.5 V, V <sub>DD</sub> = 2.5 V	-	18	-	mA
		V <sub>OL</sub> = 0.5 V, V <sub>DD</sub> = 3.3 V	-	20	-	mA
I <sub>OH</sub>	Output high current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V, V <sub>DD</sub> = 2.5 V	-	18	-	mA
		V <sub>OH</sub> = V <sub>DD</sub> - 0.5 V, V <sub>DD</sub> = 3.3 V	-	20	-	mA
I <sub>DDQ</sub>	Quiescent current	All inputs grounded, PLL and DCXO in bypass mode, Reference Input = 0	-	-	250	μA

## Thermal Resistance

Parameter <sup>[6]</sup>	Description	Test Conditions	16-pin TSSOP	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	89	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		12	°C/W

**Note**

6. These parameters are guaranteed by design and are not tested.

## Switching Characteristics

For FailSafe Devices

Parameter <sup>[8]</sup>	Description	Test Conditions	Min	Max	Unit
$f_{REF}$	Reference frequency	Commercial/Industrial Grades	4.17	166.7	MHz
$f_{OUT}$	Output frequency	15 pF Load, Commercial/Industrial Grades	4.17	166.7	MHz
$f_{XIN}$	DCXO frequency		8.0	30	MHz
$t_{DC}$	Duty cycle	Measured at $V_{DD}/2$	47	53	%
$t_{SR(I)}$	Input slew rate	Measured on REF1 Input, 30% to 70% of $V_{DD}$	0.5	4.0	V/ns
$t_{SR(O)}$	Output slew rate	Measured from 20% to 80% of $V_{DD} = 3.3$ V, 15 pF Load	0.8	4.0	V/ns
		Measured from 20% to 80% of $V_{DD} = 2.5$ V, 15 pF Load	0.4	3.0	V/ns
$t_{SK(O)}$	Output-to-output skew	All outputs equally loaded, measured at $V_{DD}/2$	–	200	ps
$t_{SK(PP)}$	Part-to-part skew	Measured at $V_{DD}/2$	–	500	ps
$t_{(\phi)}$ <sup>[7]</sup>	Static phase offset	Measured at $V_{DD}/2$	–	250	ps
$t_{D(\phi)}$ <sup>[7]</sup>	Dynamic phase offset	Measured at $V_{DD}/2$	–	500	ps
$t_{J(CC)}$	Cycle-to-cycle jitter	Load = 15 pF, $f_{OUT} \geq 6.25$ MHz	–	200	ps
			–	35	ps <sub>RMS</sub>

### Notes

- The  $t_{(\phi)}$  reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as  $t_{SR(I)}$  is maintained. Static phase offset excludes jitter; dynamic phase offset includes jitter.
- Parameters guaranteed by design and characterization, not 100% tested in production

## Switching Waveforms

Figure 8. Duty Cycle

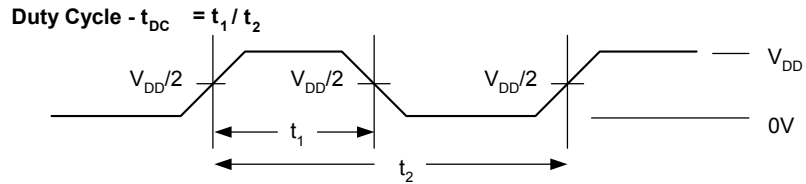


Figure 9. Input Slew Rate

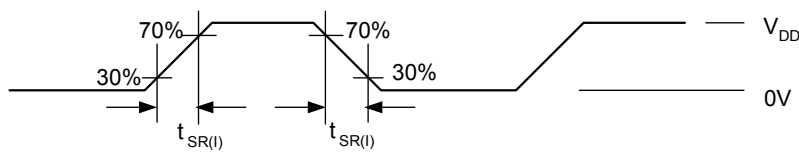


Figure 10. Output Slew Rate

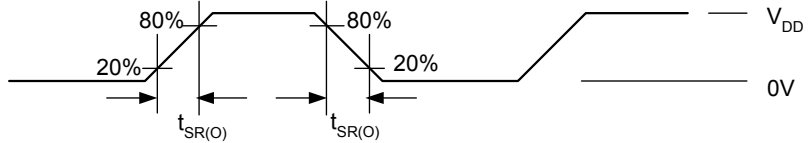


Figure 11. Output to Output Skew and IntraBank Skew

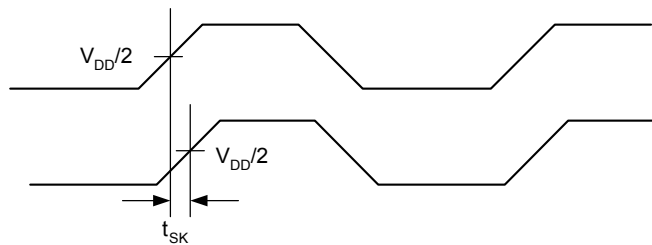
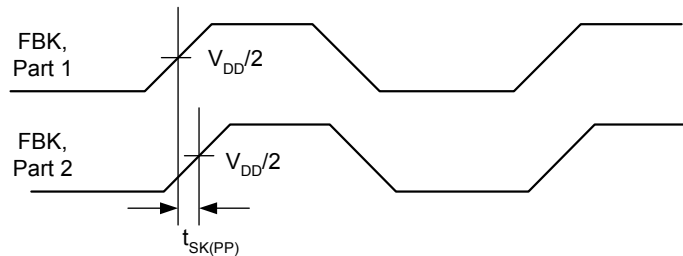
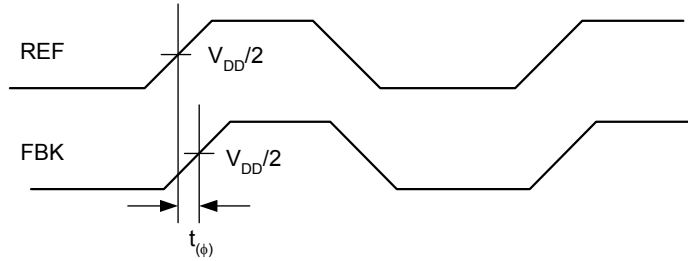


Figure 12. Part to Part Skew



Switching Waveforms (continued)

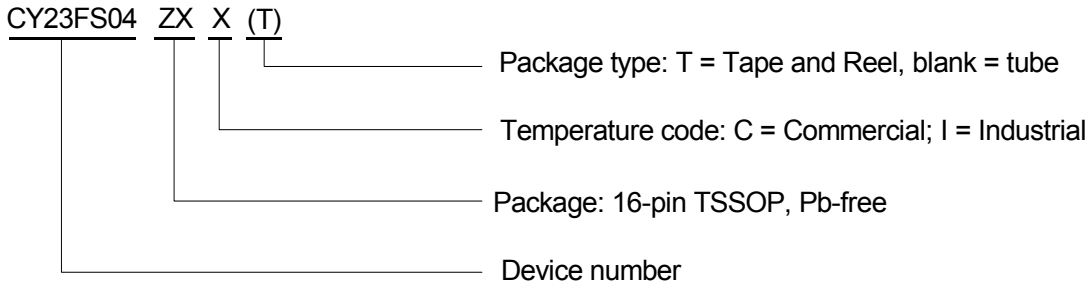
Figure 13. Phase Offset



Ordering Information

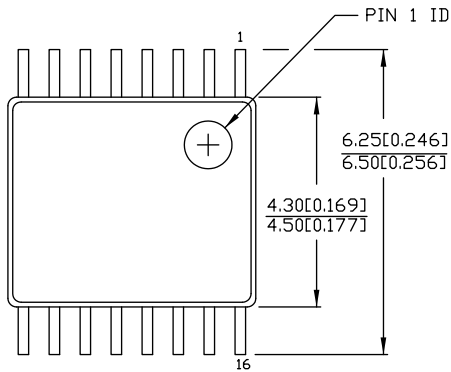
Part Number	Package Type	Product Flow
<b>Pb-free</b>		
CY23FS04ZXI	16-pin TSSOP	Industrial, -40 °C to 85 °C
CY23FS04ZXIT	16-pin TSSOP – Tape and Reel	Industrial, -40 °C to 85 °C
CY23FS04ZXC	16-pin TSSOP	Commercial, 0 °C to 70 °C
CY23FS04ZXCT	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Diagram

Figure 14. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091

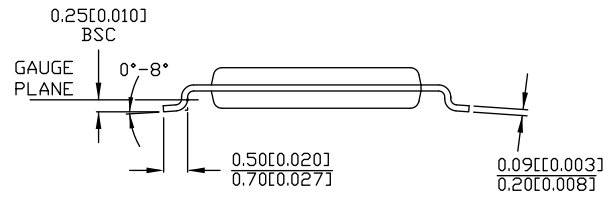
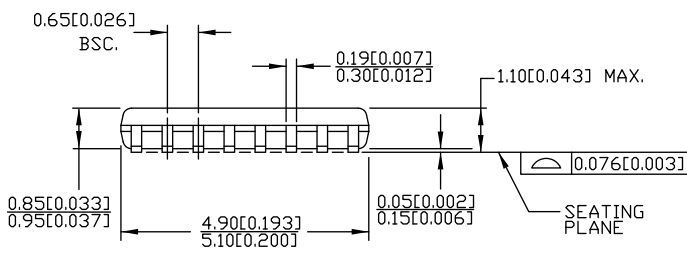


DIMENSIONS IN MM[INCHES] MIN.  
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



51-85091 \*E

## Acronyms

Acronym	Description
DCXO	digitally controlled crystal oscillator
ESD	electrostatic discharge
PLL	phase locked loop
RMS	root mean square
SSOP	shrunk small outline package
TSSPO	thin shrunk small outline package
XTAL	crystal

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
mA	milliampere
ms	milli second
MHz	megahertz
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

**Document History Page**

Document Title: CY23FS04, Failsafe™ 2.5 V/3.3 V Zero Delay Buffer Document Number: 38-07304				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	123698	04/24/03	RGL	New data sheet.
*A	223811	See ECN	RGL/ZJX	Changed the XTAL Specifications table.
*B	276712	See ECN	RGL	Removed (T <sub>LOCK</sub> ) Lock Time Specification
*C	378918	See ECN	RGL	Added Lead-free devices
*D	2865337	01/25/2010	CXQ	Updated format. Changed max output frequency from 170 MHz to 166.7 MHz. Added "Contents" section on page 2. Removed previous Figures 5 and 6. Added/separated Figures 7 through 12. Changed references of "CI" to "C <sub>LOAD</sub> ". Removed extra T <sub>A</sub> reference in Absolute Maximum Conditions. Changed table captions for Tables 4, 5, and 6 to section headings. Removed note 5 regarding programming cap array. Replaced crystal ECX-5806-18.432M with ECX-6362-18.432M in Note 5. Removed obsolete/pruned Pb-devices from Ordering Information. Removed unreferenced Note 9. Updated package drawing specification to rev *B.
*E	2925613	04/30/10	KVM	Post to external web.
*F	3054919	10/11/2010	KVM	Revised Dynamic Phase Offset value. Added phase offset definition. Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> . Added <a href="#">Acronyms</a> , and <a href="#">Units of Measure</a> .
*G	3342812	08/12/2011	PURU	Updated <a href="#">Ordering Code Definitions</a> .
*H	3695677	08/03/2012	PURU	Updated <a href="#">XTAL Selection Criteria and Application Example</a> : Updated <a href="#">Figure 7</a> . Updated <a href="#">Table 2</a> . Added Important Notes. Updated <a href="#">Ordering Code Definitions</a> under <a href="#">Ordering Information</a> Replaced SSOP with TSSOP. Updated <a href="#">Package Diagram</a> : spec 51-85091 – Changed revision from *C to *D.
*I	4580603	11/26/2014	AJU	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated <a href="#">Package Diagram</a> : spec 51-85091 – Changed revision from *D to *E.
*J	4930960	09/23/2015	TAVA	Updated to new template. Completing Sunset Review.
*K	5275836	05/27/2016	PSR	Updated <a href="#">Absolute Maximum Conditions</a> : Removed $\theta_{JC}$ , $\theta_{JA}$ parameters and their details. Added <a href="#">Thermal Resistance</a> . Updated to new template.
*L	5451081	09/27/2016	TAVA	Updated to new template. Completing Sunset Review.
*M	5994174	12/14/2017	AESATMP9	Updated logo and copyright.

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