

0 Hz/DC to 18 GHz, SP4T, MEMS Switch

FEATURES

- ▶ Fully operational from DC to 18 GHz (typical)
- ▶ RF performance characteristics
 - ▶ Insertion loss: -1.7 dB (typical) at 16 GHz
 - ▶ Isolation: -18.5 dB (typical) at 6 GHz
 - ▶ IIP3: 73 dBm (typical)
 - ▶ RF power: 33 dBm (maximum)
- ▶ On resistance: 1.9 Ω (typical)
- ▶ DC current handling: 200 mA
- ▶ Actuation lifetime: 200 million cycles (minimum)
- ▶ On switching time: 200 μ s (typical)
- ▶ Integrated 3.3 V driver for simple control with parallel and SPI interface
- ▶ Independently controllable switches
- ▶ Space saving integrated passive components
 - ▶ Eliminates floating nodes on the switch
- ▶ 5 mm \times 4 mm \times 1.0 mm, 24-lead land grid array package
- ▶ Temperature range: -40°C to +85°C
- ▶ Switch position is unknown with no supply voltage

APPLICATIONS

- ▶ Automatic test equipment (ATE) load and probe boards
- ▶ DC with high speed digital testing
- ▶ Relay replacements
- ▶ RF test instrumentation
- ▶ ATE: RF, digital, and mixed signals
- ▶ RF wireless communications
- ▶ High performance RF switching

GENERAL DESCRIPTION

The ADGM1144 is a wideband, single-pole, four-throw (SP4T) switch, fabricated using Analog Devices, Inc., microelectromechanical system (MEMS) switch technology. This technology enables a small form factor, wide RF bandwidth, highly linear, low insertion loss switch that is operational down to 0 Hz/DC, making it an ideal solution for a wide range of RF and precision equipment switching needs.

An integrated driver chip generates a high voltage to an electrostatically actuate switch that can be controlled by a parallel interface and a serial peripheral interface (SPI). All four switches are independently controllable.

The device is packaged in a 24-lead, 5 mm \times 4 mm \times 1.0 mm land grid array package (LGA).

The ADGM1144 has integrated 10 M Ω resistors required for floating node avoidance. The presence of these integrated 10 M Ω resistors saves board space and eliminates floating nodes on the switch. To ensure optimum operation of the ADGM1144, refer to the [Critical Operational Requirements](#) section.

Throughout this data sheet, multifunction pins, such as IN1/SDI, are referred to either by the entire pin name or by a single function of the pin, for example IN1, when only that function is relevant.

COMPANION PRODUCTS

- ▶ Quad PMU : [AD5522](#)
- ▶ MEMS Switch: [ADGM1304](#), [ADGM1004](#), [ADGM1001](#), [ADGM1002](#), [ADGM1003](#)
- ▶ Low Noise, LDO : [ADP7142](#), [LT1962](#), [LT3045-1](#)

FUNCTIONAL BLOCK DIAGRAM

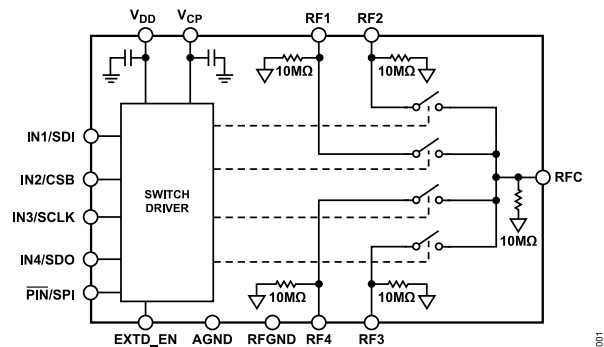


Figure 1.

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REVISION HISTORY**09/2022—Revision 0: Initial Version**

SPECIFICATIONS

$V_{DD} = 3.0\text{ V to }3.6\text{ V}$, AGND, RFGND = 0 V, all specifications at 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test Conditions/Comments ²
ON-RESISTANCE PROPERTIES						
Initial On-Resistance Properties						
On Resistance	R_{ON}		1.9	3	Ω	Drain-source current (I_{DS}) = 50 mA, 0 V input bias, at 1 ms after first actuation, maximum specification from -40°C to 85°C
On-Resistance Match Between Channels	$\Delta R_{ON\ CH_CH}$			0.8	Ω	Maximum value tested from -40°C to 85°C at Time 0 (T0)
On-Resistance Drift						
Over Time	$\Delta R_{ON\ TIME}$			-0.32	Ω	R_{ON} changed from 1 ms to 100 ms after first actuation, maximum value tested from -40°C to 85°C
Over Actuations	ΔR_{ON}		0.2	0.3	Ω	Absolute change after 10^6 actuations, switch is actuated at 25°C and R_{ON} is measured at 25°C
					Ω	Absolute change after 100×10^6 actuations lifetime, switch is actuated at 25°C and R_{ON} is measured at 25°C
					Ω	Absolute change after 100×10^6 actuations, switch is actuated at 85°C, R_{ON} is measured at 25°C, and actuation, frequency = 289 Hz
RELIABILITY PROPERTIES						
Continuously On Lifetime			10		Years	Time before failure ³ at 85°C
Actuation Lifetime						
Cold Switched		100×10^6	500×10^6		Actuations	Load between toggling is 220 mA, tested at 85°C
RF Hot Switched						
7 dBm			500×10^9		Actuations	RF power = continuous wave, terminated into 50 Ω , 50% of test population failure point (T50)
10 dBm			150×10^6		Actuations	
13 dBm			30×10^6		Actuations	
20 dBm			20×10^3		Actuations	
DC Hot Switched						
0.5 V or 9 mA			500×10^6		Actuations	Terminated into 50 Ω , RFx load capacitance = 10 μF , 50% of test population failure point (T50)
1 V or 18 mA			500×10^6		Actuations	
2.5 V or 46 mA			35×10^6		Actuations	
3.5 V or 65 mA			6.5×10^3		Actuations	
5 V or 93 mA			2×10^3		Actuations	
DYNAMIC CHARACTERISTICS						
Operational Frequency Range						
Insertion Loss	IL	DC	18		GHz	RFx to RFC (-3 dB)
			-0.34		dB	DC to 2.5 GHz, RFC to RFx
			-0.5		dB	2.5 GHz to 6 GHz, RFC to RFx
			-0.74		dB	6 GHz to 10 GHz, RFC to RFx
			-1.7		dB	10 GHz to 16 GHz, RFC to RFx
Isolation						
RFx to RFC (All Off)	ISO		-26		dB	DC to 2.5 GHz, RFC to RFx (all channels off)
			-18.5		dB	2.5 GHz to 6 GHz, RFC to RFx (all channels off)
			-14		dB	6 GHz to 10 GHz, RFC to RFx (all channels off)
			-13		dB	10 GHz to 16 GHz, RFC to RFx (all channels off)
			-31		dB	DC to 2.5 GHz, RFC to RFx (one channel on)

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test Conditions/Comments ²
Crosstalk	CTK		-24		dB	2.5 GHz to 6 GHz, RFC to RFx (one channel on)
			-19		dB	6 GHz to 10 GHz, RFC to RFx (one channel on)
			-16		dB	10 GHz to 16 GHz, RFC to RFx (one channel on)
Return Loss	RL		-29.5		dB	DC to 2.5 GHz, RFC to RFx
			-23		dB	2.5 GHz to 6 GHz, RFC to RFx
			-18		dB	6 GHz to 10 GHz, RFC to RFx
Third-Order Intermodulation Intercept	IIP3		-14.5			10 GHz to 16 GHz, RFC to RFx
			-26.5		dB	DC to 2.5 GHz, RFC to RFx
			-24.5		dB	2.5 GHz to 6 GHz, RFC to RFx
Second Harmonic	HD2		-24		dB	6 GHz to 10 GHz, RFC to RFx
			-14.5			10 GHz to 16 GHz, RFC to RFx
			73		dBm	Input: 2110 MHz and 2170 MHz, 3510 MHz and 3570 MHz, and P _{IN} = 30 dBm
Third Harmonic	HD3		-99		dBc	Input: 5 MHz, input power = 0 dBm
			-88		dBc	Input: 150 MHz, 800 MHz, and P _{IN} = 33 dBm
Total Harmonic Distortion	THD		-88		dBc	Input: 150 MHz, 800 MHz, and P _{IN} = 33 dBm
Total Harmonic Distortion Plus Noise	THD + N		-105		dBc	R _L = 300 Ω, f = 1 kHz, RFx = 2.5 V p-p
Maximum RF Power				33	dBm	R _L = 300 Ω, f = 1 kHz, RFx = 2.5 V p-p
DC Signal Range		-6		+6	V	50 Ω termination
Standoff Voltage		-6		+6	V	On switch DC input-bias voltage signal range, -40°C to +85°C
Maximum DC Current				200	mA	-40°C to +85°C
On Switching Time ⁴	t _{ON}			200	μs	50% INx to 90% (0.05 dB of final IL value) RFx, 50 Ω termination, -40°C to 85°C. See Figure 5 for details
Off Switching Time ⁵	t _{OFF}			200	μs	50% INx to 10% (0.05 dB of final IL value) RFx, 50 Ω termination, -40°C to +85°C. See Figure 5 for details
Power-Up Time			4	5	ms	VCP capacitor = 100 pF, -40°C to +85°C
Video Feedthrough			10		mV peak	1 MΩ termination at RFx and 50 Ω termination at RFC
Actuation Frequency				2	kHz	Both switches toggled simultaneously
Internal Oscillator Frequency		8.6	10	11	MHz	
Internal Oscillator Feedthrough ^{6, 7}			-123		dBm	
			-146		dBm/Hz	This value came from calculations
CAPACITANCE PROPERTIES						At 1 MHz, includes LGA package capacitance
On Switch Channel Capacitance	C _{ON}		2.3		pF	
Off Switch Channel Capacitance	C _{OFF}		1.4		pF	
LEAKAGE PROPERTIES ⁸						
On Leakage		0.7	1.11	1.39	μA	RFx (off channels) = +6 V, RFC/RFx (on channel) = -6 V, maximum value tested from -40°C to +85°C
Off Leakage		0.35	0.56	0.71	μA	RFx = +6 V, RFC = -6 V, maximum value tested from -40°C to +85°C
Internal Shunt Resistor		8.4	11	14.7	MΩ	Typical temperature coefficient = 27.5 kΩ/°C, maximum and minimum values tested at 25°C
DIGITAL INPUTS						Minimum and maximum over -40°C to +85°C

SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test Conditions/Comments ²
Input High Voltage	V_{INH}	2			V	Input voltage (V_{IN}) = V_{INL} or V_{INH}
Input Low Voltage	V_{INL}			0.8	V	
Input Current	I_{INL}/I_{INH}		0.025	1	μ A	
Capacitance			5		pF	
DIGITAL OUTPUTS						
Output Low Voltage	V_{OL}			0.4	V_{MAX}	Minimum and maximum over -40°C to $+85^{\circ}\text{C}$ $I_{SINK} = 1\text{ mA}$ $I_{SOURCE} = 1\text{ mA}$
Output High Voltage	V_{OH}	$V_{DD} - 0.4$ V			V_{MIN}	
Capacitance			5		pF	
POWER REQUIREMENTS						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Minimum and maximum over -40°C to $+85^{\circ}\text{C}$ Digital inputs = 0 V or V_{DD} , SDO floating in SPI mode This value is I_{DD} in low power mode
Supply Current	I_{DD}		2	2.5	mA	
Low Power Mode Current ⁹	$I_{DD_EXT_VCP}$			50	μ A	
External Drive Voltage ¹⁰	V_{CP_EXT}	79.2	80	80.8		
External Drive Current	$I_{CP_EXT_VCP}$			5	μ A	

¹ Typical specifications tested at 25°C with $V_{DD} = 3.3\text{ V}$.

² RFX is RF1, RF2, RF3, or RF4. INx is IN1, IN2, IN3, or IN4.

³ This value shows the time that it takes for 1% of a sample lot to fail.

⁴ Switch is settled after 200 μ s. Do not apply RF power between 0 μ s to 200 μ s.

⁵ RF power must be removed or less than 5 dBm, 50 μ s before turning the switch off.

⁶ Disable the internal oscillator to eliminate feedthrough.

⁷ Spectrum analyzer setup: resolution bandwidth (RBW) = 200 Hz, video bandwidth (VBW) = 2 Hz, span = 100 kHz, input attenuator = 0 dB, detector type = peak, maximum hold = off. Measurements taken with one on and off switch port terminated into 50 Ω . The fundamental feedthrough noise or harmonic thereof is tested (whichever is the highest).

⁸ The on-leakage and off-leakage specification depends on the DC voltage level applied to the switch node. For example, if 1 V is applied at RF1 to RFC, the on leakage specification is 0.2 μ A and the off leakage specification is 0.1 μ A. The leakage specification of the switch is mainly driven by the internal 10 M Ω resistors to ground connected on all the RF nodes to avoid floating nodes.

⁹ For more details, see the [Low Power Mode](#) section.

¹⁰ For more details, see the [Internal Oscillator Feedthrough Mitigation](#) section.

TIMING CHARACTERISTICS

$V_{DD} = 3.0\text{ V}$ to 3.6 V , AGND, RFGND = 0 V, and all specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}	Limit at T_{MAX}	Unit	Conditions/Comments
t_1	100		ns	SCLK period.
t_2	45		ns	SCLK high pulse width.
t_3	45		ns	SCLK low pulse width.
t_4	25		ns	$\overline{\text{CS}}$ falling edge to SCLK active edge.
t_5	20		ns	Data setup time.
t_6	20		ns	Data hold time.
t_7	25		ns	SCLK active edge to $\overline{\text{CS}}$ rising edge.
t_8		20	ns	$\overline{\text{CS}}$ falling edge to SDO data available.

SPECIFICATIONS

Table 2.

Parameter	Limit at T _{MIN}	Limit at T _{MAX}	Unit	Conditions/Comments
t ₉		40	ns	SCLK falling edge to SDO data available. Measured with a 20 pF load. t ₉ determines the maximum SCLK frequency when SDO is used.
t ₁₀		25	ns	$\overline{\text{CS}}$ rising edge to SDO returns to high impedance.
t ₁₁	100		ns	$\overline{\text{CS}}$ high time between SPI commands.
t ₁₂	25		ns	SCLK edge rejection to $\overline{\text{CS}}$ falling edge.
t ₁₃	25		ns	$\overline{\text{CS}}$ rising edge to SCLK edge rejection.

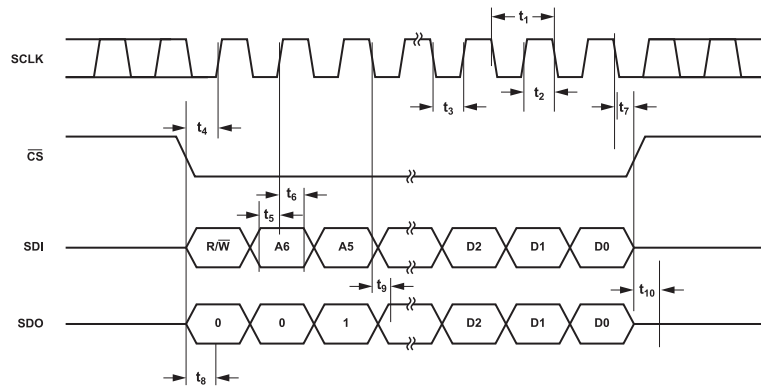


Figure 2. Addressable Mode Timing Diagram

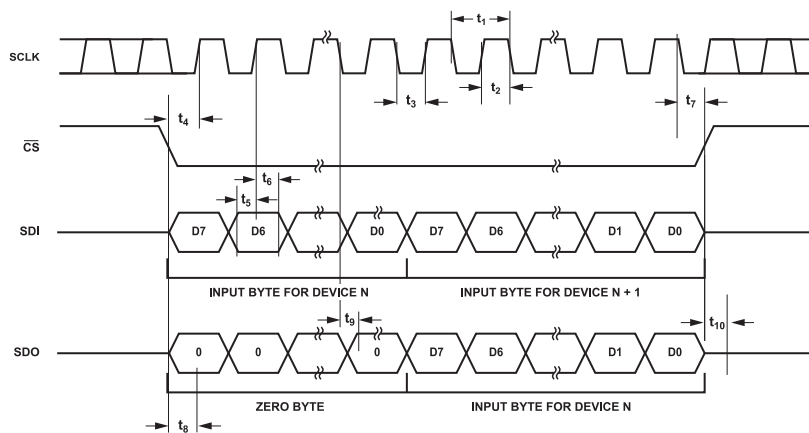


Figure 3. Daisy Chain Timing Diagram

SPECIFICATIONS

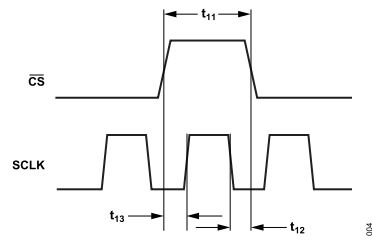


Figure 4. SCLK/ \overline{CS} Timing Relationship

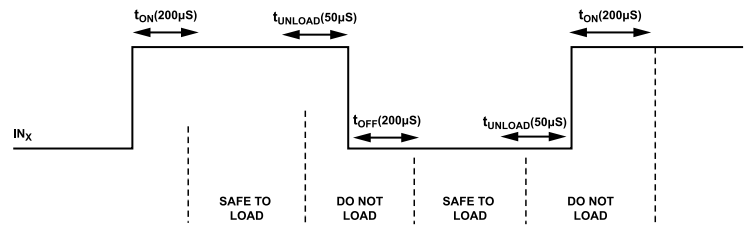


Figure 5. Switch Loading Profile

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to AGND	-0.3 V to +6 V
Digital Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V or 30 mA (whichever occurs first)
Switch DC Rating ²	
Voltage	± 7 V
Current	220 mA
$V_{CP_{EXT}}$	82 V
Stand Off Voltage ³	± 10 V
RF Power Rating ⁴	34 dBm
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Reflow Soldering (Pb-Free)	
Peak Temperature	260(+0/-5) $^\circ\text{C}$
Time at Peak Temperature	10 sec to 30 sec
Group D	
Mechanical Shock ⁵	1500 g with 0.5 ms pulse
Vibration	20 Hz to 2000 Hz acceleration at 50 g
Constant Acceleration	30,000 g

¹ Limit the current to the maximum ratings shown.

² This rating is with respect to the switch in the on position with no RF signal applied.

³ This rating is with respect to the switch in the off position with no RF signal applied.

⁴ This rating is with respect to the switch in the on position and terminated into 50 Ω .

⁵ If a device is dropped during handling, do not use the device.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JCT} is the junction to the top of the case thermal resistance. θ_{JCB} is the junction to the bottom of the case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JCT}	θ_{JCB}	Unit
CC-24-11	104.3	134	66.2	$^\circ\text{C}/\text{W}$

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001. Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADGM1144

Table 5. ADGM1144, 24-Lead LGA

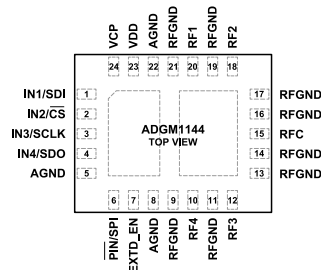
ESD Model	Withstand Threshold (V)	Class
HBM	150 V for the RF1, RF2, RF3, RF4 and RFC pins 2 kV for all other pins	0
FICDM	500 V	C2a

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. EXPOSED PAD1, EP1 IS INTERNALLY CONNECTED TO AGND. IT IS RECOMMENDED TO CONNECT TO BOTH AGND AND RFGND.
 2. EXPOSED PAD 2, EP2 IS INTERNALLY CONNECTED TO RFGND. IT IS RECOMMENDED TO CONNECT TO BOTH RFGND AND AGND.

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Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1/SDI	Parallel Logic Digital Control Input 1 (IN1). The voltage applied to this pin controls the gate of the RF1 to RFC MEMS switch. Serial Data Input (SDI). In SPI mode, this is the serial data input pin.
2	IN2/ \overline{CS}	Parallel Logic Digital Control Input 2 (IN2). The voltage applied to this pin controls the gate of the RF2 to RFC MEMS switch. Chip Select (\overline{CS}). In SPI mode, this is the chip select pin.
3	IN3/SCLK	Parallel Logic Digital Control Input 3 (IN3). The voltage applied to this pin controls the gate of the RF3 to RFC MEMS switch. Serial Clock Input (SCLK). In SPI mode, this is the serial clock input pin.
4	IN4/SDO	Parallel Logic Digital Control Input 4 (IN4). The voltage applied to this pin controls the gate of the RF4 to RFC MEMS switch. Serial Data Output (SDO). In SPI mode, this is the serial data output pin.
5, 8, 22	AGND	Analog Ground Connection. It is recommended to connect AGND and RFGND together.
6	\overline{PIN}/SPI	Parallel Mode Enable (\overline{PIN}). The parallel-interface (IN1, IN2, IN3, IN4) is enabled when this pin is low. SPI Mode Enable (SPI). The SPI interface is enabled when this pin is high.
7	EXTD_EN	External Voltage Drive Enable. In normal operation, set EXTD_EN low to enable the built-in 10 MHz oscillator, which enables the internal driver IC voltage boost circuitry. Setting EXTD_EN high disables the internal 10 MHz oscillator and driver boost circuitry. With the oscillator disabled, the switch can still be controlled by the logic interface pins (IN1 to IN4) or by the SPI interface, but the VCP pin must be driven with 80 V DC from an external voltage supply. With the oscillator disabled, the ADGM1144 only consumes 50 μ A maximum supply current. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough from the switch.
9, 11, 13, 14, 16, 17, 19, 21	RFGND	RF Ground Connection. It is recommended to connect AGND and RFGND together.
10	RF4	RF4 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
12	RF3	RF3 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
15	RFC	Common RF Port. This pin can be an input or an output.
18	RF2	RF2 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
20	RF1	RF1 Port. This pin can be an input or an output. If unused, the pin must be connected to RFGND or terminate the pin with a 50 Ω resistor to RFGND.
23	VDD	Positive Power Supply Input. For the recommend input voltage, see Table 1. No external AC decoupling capacitors are needed because they are integrated into the package.
24	VCP	Driver IC Input/Output. In normal operating mode, this pin outputs 80 V DC and must not be loaded externally because there is an internal decoupling capacitor connected to ground in the package. If Pin 7 is high, the internal voltage boost circuitry is disabled and an 80 V DC voltage must be input into VCP to drive the switches by the logic interface.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**Table 6. Pin Function Descriptions**

Pin No.	Mnemonic	Description
	EP1	Exposed Pad 1. EP1 is internally connected to AGND. It is recommended to connect EP1 to both AGND and RFGND.
	EP2	Exposed Pad 2. EP2 is internally connected to RFGND. It is recommended to connect EP2 to both RFGND and AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

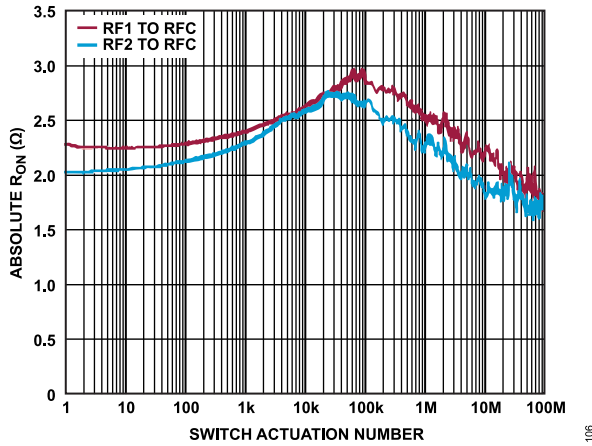


Figure 7. Absolute R_{ON} vs. Switch Actuation Number, $T_A = 25^\circ\text{C}$, Load Applied During Actuations = 50 mA

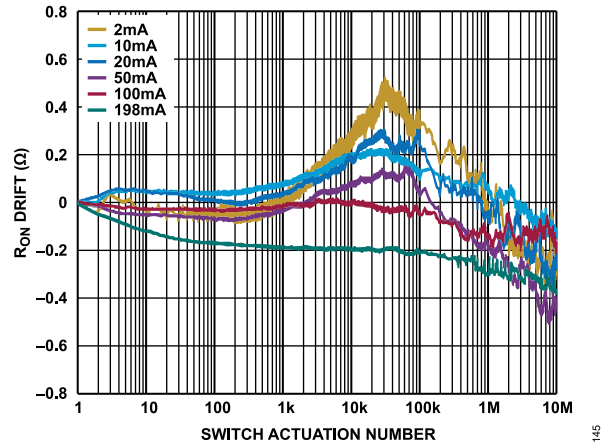


Figure 10. R_{ON} Drift vs. Switch Actuation Number Over Different Current Applied During Actuations, Normalized at Zero ($T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$)

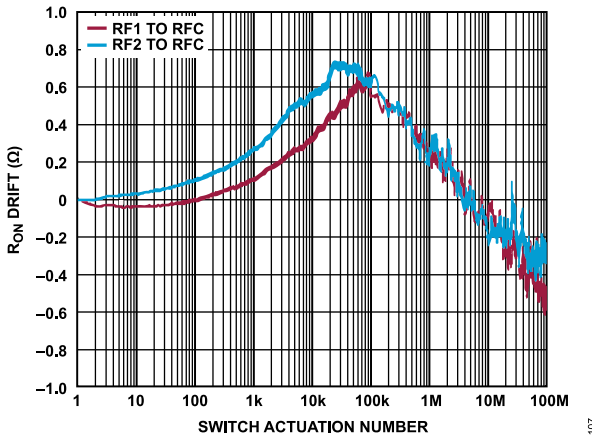


Figure 8. R_{ON} Drift vs. Switch Actuation Number, Normalized at Zero, $T_A = 25^\circ\text{C}$, and Load Applied During Actuations = 50 mA

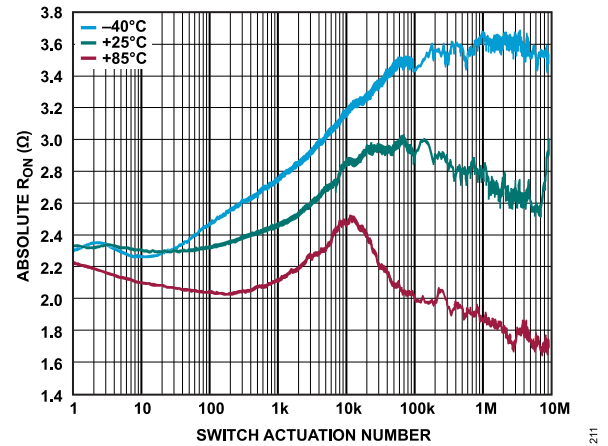


Figure 11. Absolute R_{ON} vs. Switch Actuation Number Over Different Temperature (Current Applied During Actuations = 50 mA, $V_{DD} = 3.3\text{ V}$)

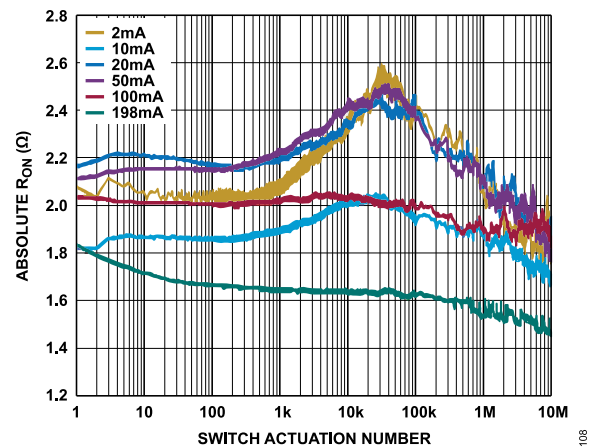


Figure 9. Absolute R_{ON} vs. Switch Actuation Number Over Different Current Applied During Actuations ($T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$)

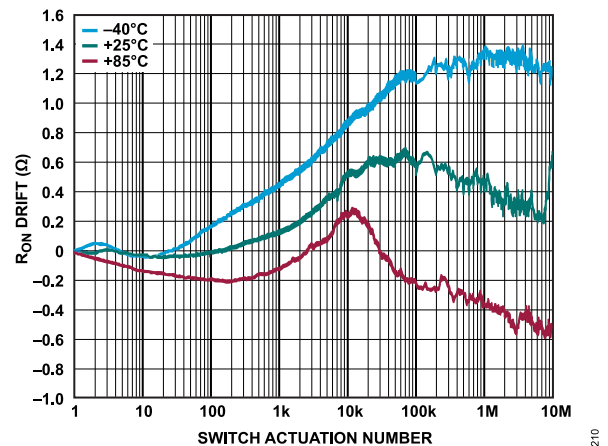


Figure 12. R_{ON} Drift vs. Switch Actuation Number Over Different Temperatures, Normalized at Zero (Current Applied During Actuations = 50 mA, $V_{DD} = 3.3\text{ V}$)

TYPICAL PERFORMANCE CHARACTERISTICS

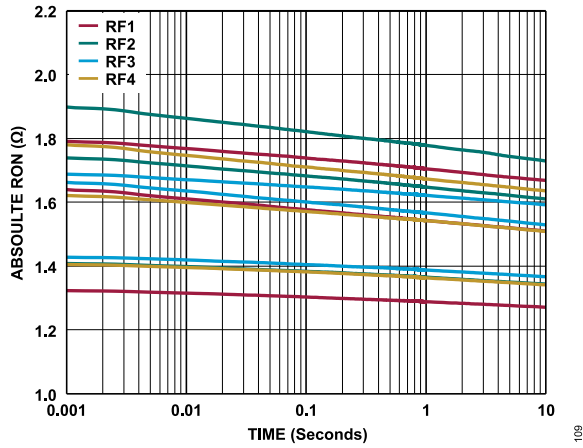


Figure 13. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Different Channels, Multiple Devices, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, Current = 50 mA

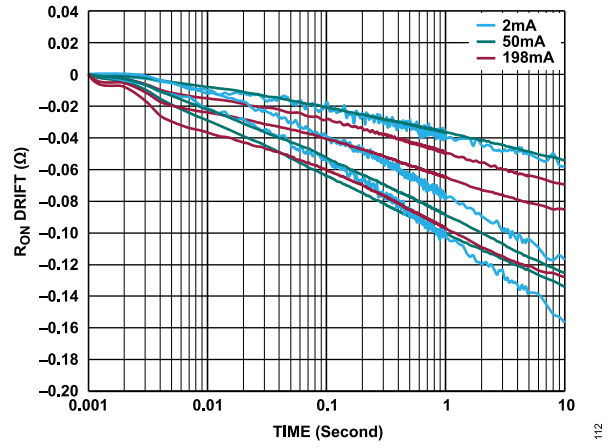


Figure 16. R_{ON} Drift vs. Time (1 ms to 10 sec) over Different Current Levels, Multiple Devices, Normalized at Zero, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, RF1 to RFC

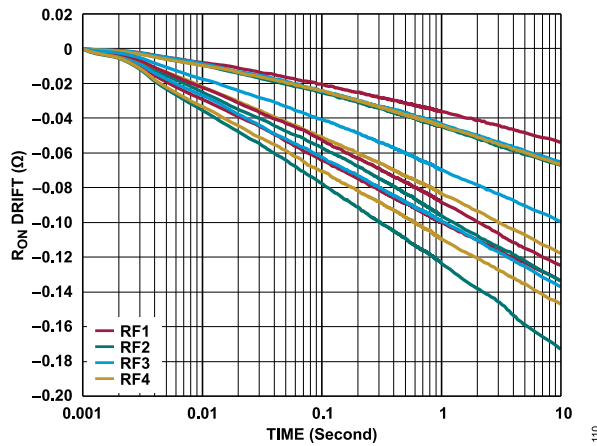


Figure 14. R_{ON} Drift vs. Time (1 ms to 10 sec) over Different Channels, Multiple Devices, Normalized at Zero, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, Current = 50 mA

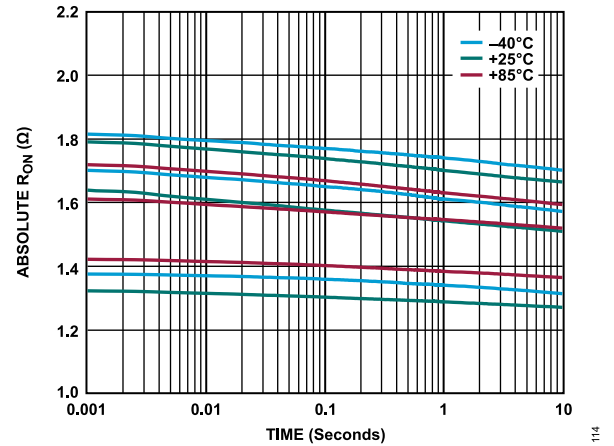


Figure 17. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Temperature, Multiple Devices, Current = 50 mA, $V_{DD} = 3.3\text{ V}$, RF1 to RFC

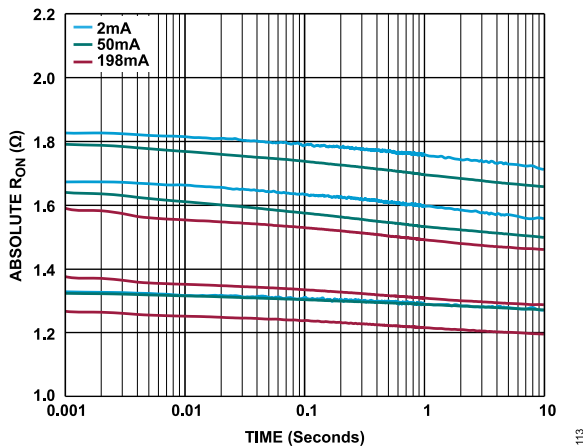


Figure 15. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Different Current Levels, Multiple Devices, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, RF1 to RFC

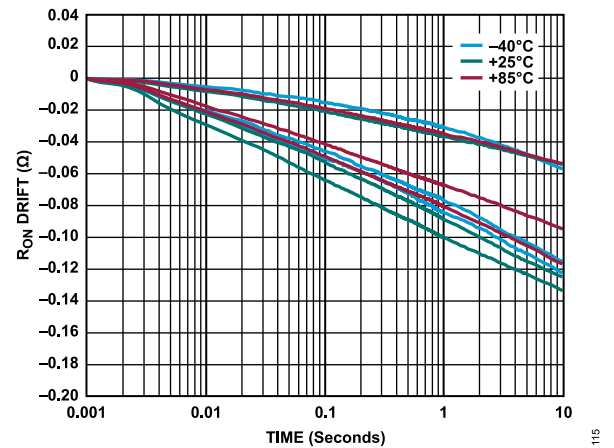


Figure 18. R_{ON} Drift vs. Time (1 ms to 10 sec) over Temperature, Multiple Devices, Normalized at Zero, Current = 50 mA, $V_{DD} = 3.3\text{ V}$, RF1 to RFC

TYPICAL PERFORMANCE CHARACTERISTICS

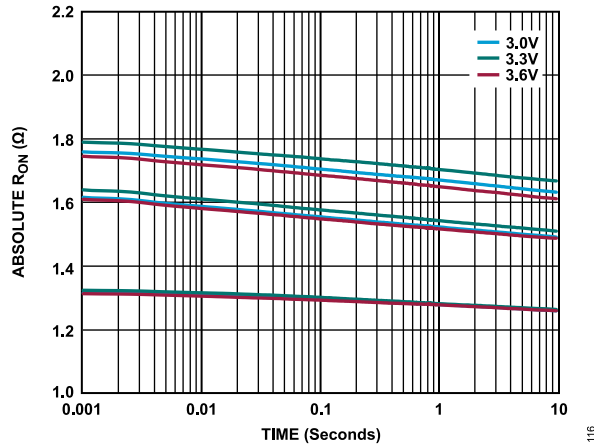


Figure 19. Absolute R_{ON} vs. Time (1 ms to 10 sec) over Supplies, Multiple Devices, Current = 50 mA, V_{DD} = 3.3 V, RF1 to RFC

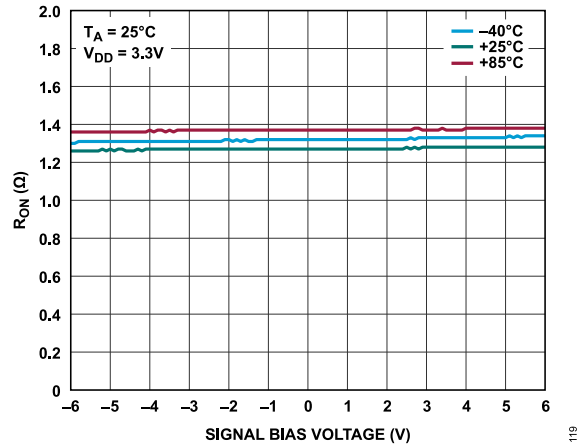


Figure 22. R_{ON} vs. Signal Bias Voltage over Temperature (RF1 to RFC On, 50 mA)

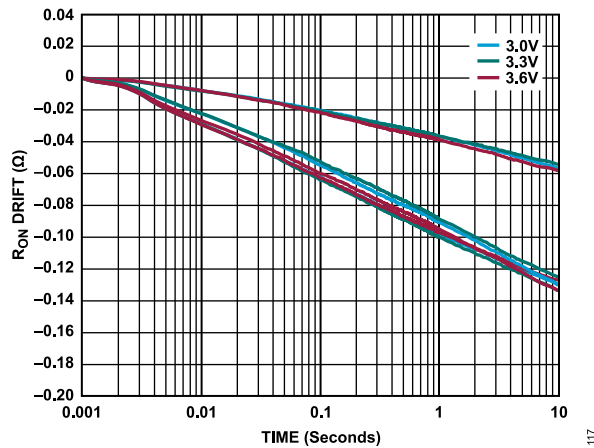


Figure 20. R_{ON} Drift vs. Time (1 ms to 10 sec) over Supplies, Multiple Devices, Normalized at Zero, Current = 50 mA, V_{DD} = 3.3 V, RF1 to RFC

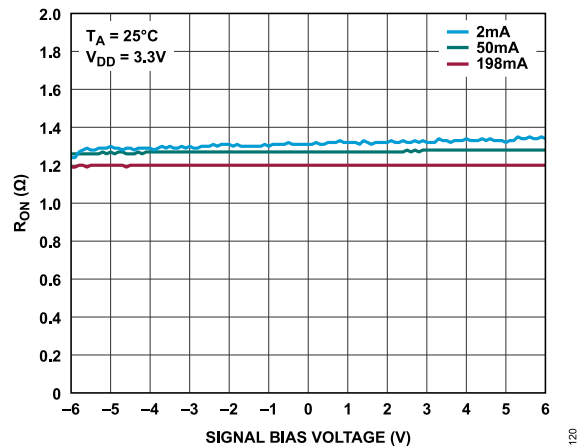


Figure 23. R_{ON} vs. Signal Bias Voltage over Different Current Levels, (RF1 to RFC On)

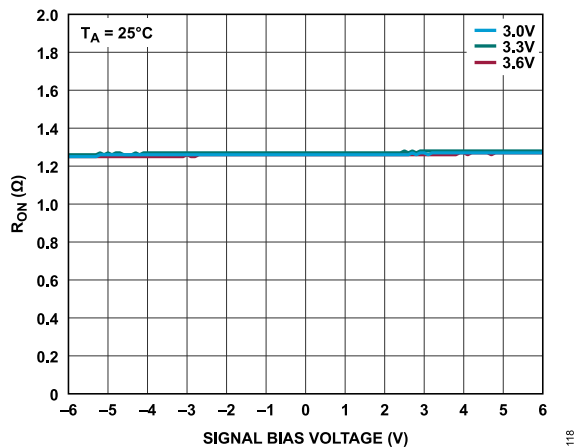


Figure 21. R_{ON} vs. Signal Bias Voltage over Supply Voltages (RF1 to RFC On, 50 mA)

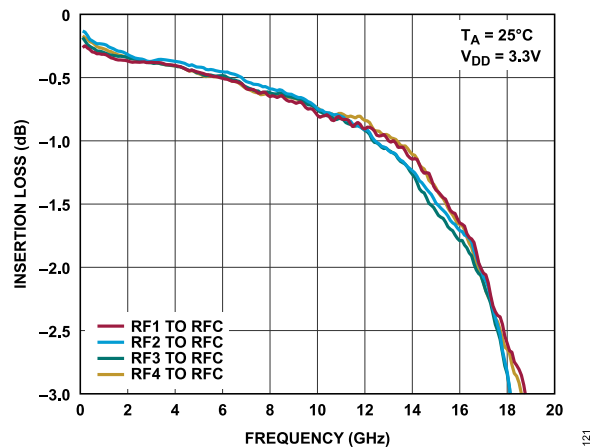


Figure 24. Insertion Loss vs. Frequency, Linear Scale

TYPICAL PERFORMANCE CHARACTERISTICS

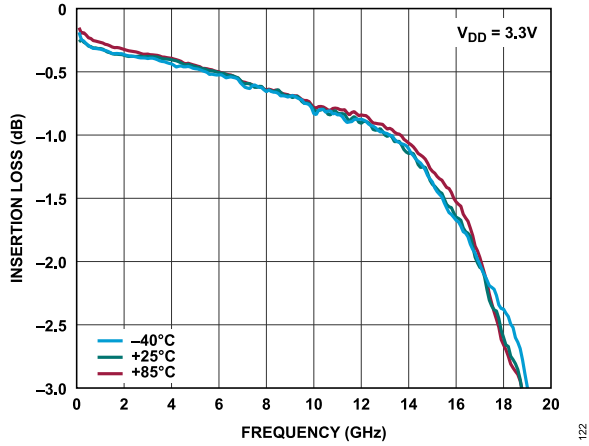


Figure 25. Insertion Loss vs. Frequency over Temperature (RF1 to RFC)

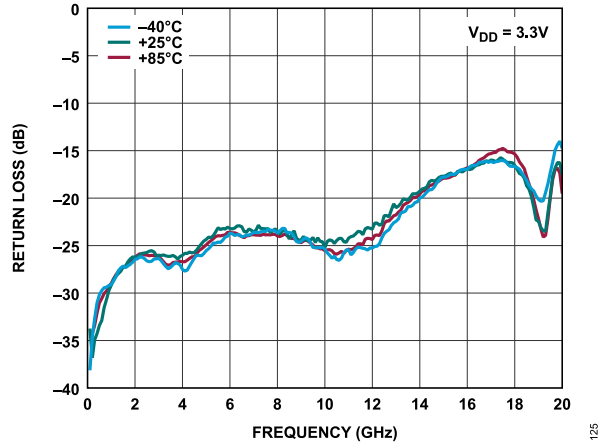


Figure 28. Return Loss vs. Frequency over Temperature (RF1 to RFC)

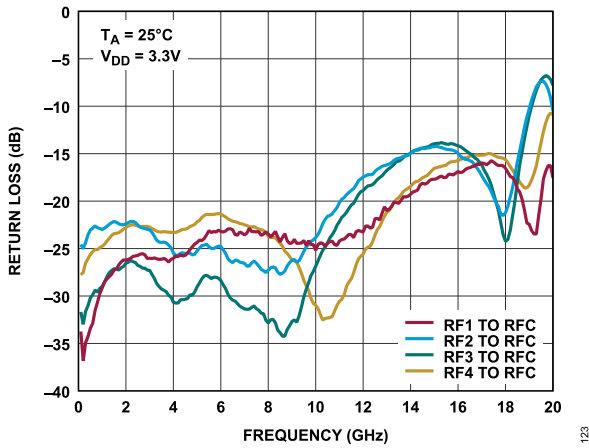


Figure 26. Return Loss vs. Frequency (RFx to RFC)

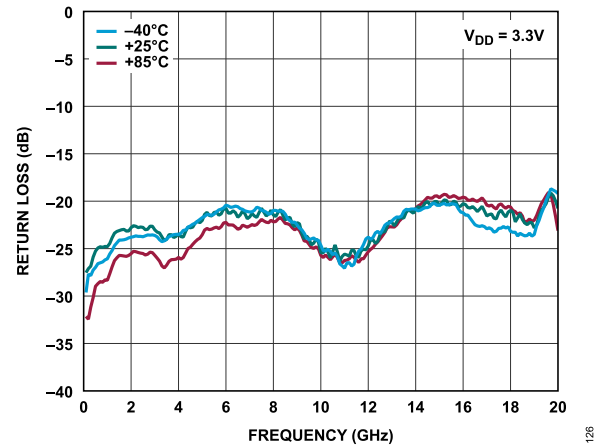


Figure 29. Return Loss vs. Frequency over Temperature (RFC to RF1)

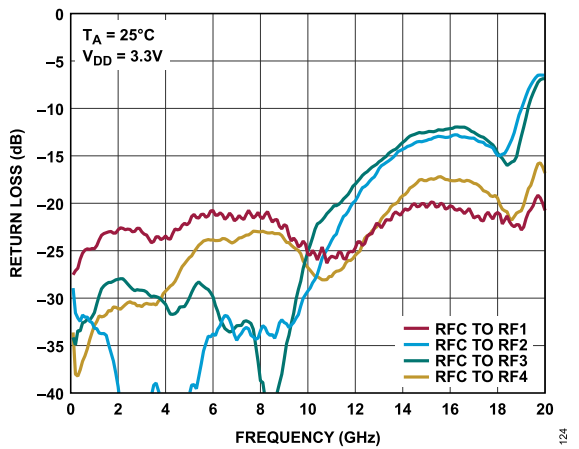


Figure 27. Return Loss vs. Frequency (RFC to RFx)

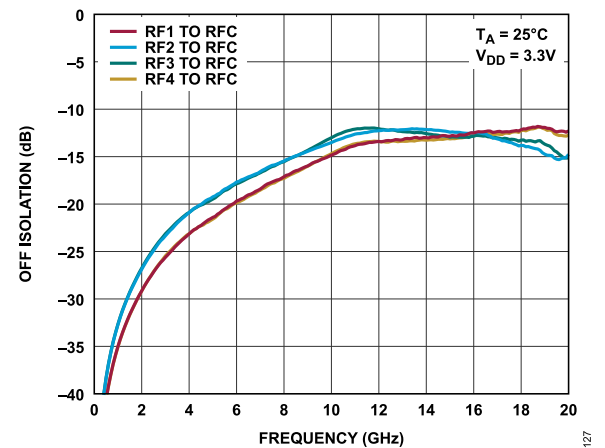


Figure 30. Off Isolation vs. Frequency, All Channels Off (RFx to RFC)

TYPICAL PERFORMANCE CHARACTERISTICS

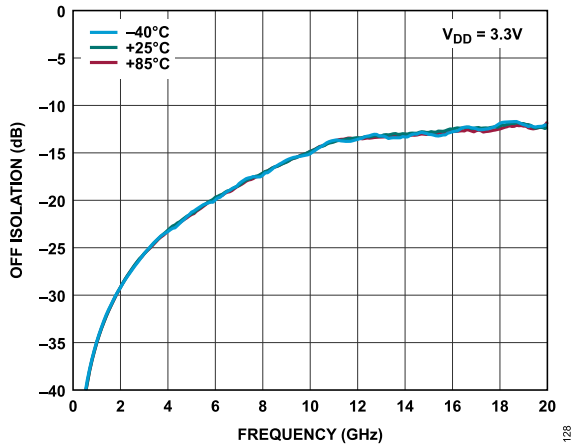


Figure 31. Off Isolation vs. Frequency over Temperature, All Channels Off (RF1 to RFC)

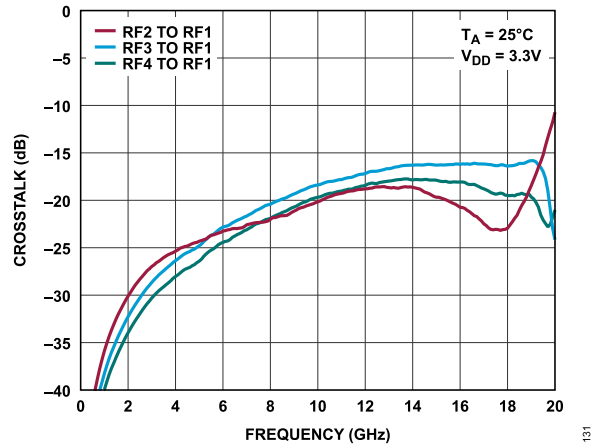


Figure 34. Crosstalk vs. Frequency (RFx to RF1)

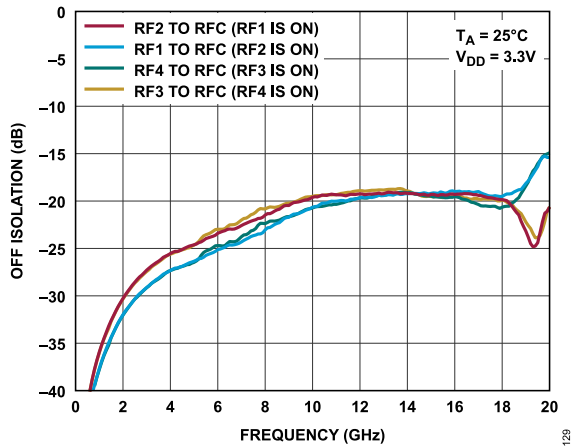


Figure 32. Off Isolation vs. Frequency, One Channel On

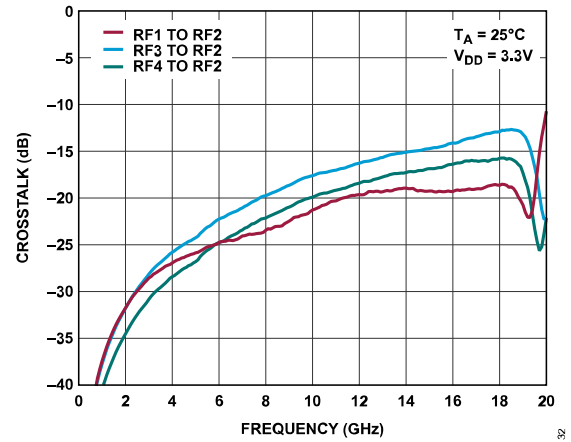


Figure 35. Crosstalk vs. Frequency (RFx to RF2)

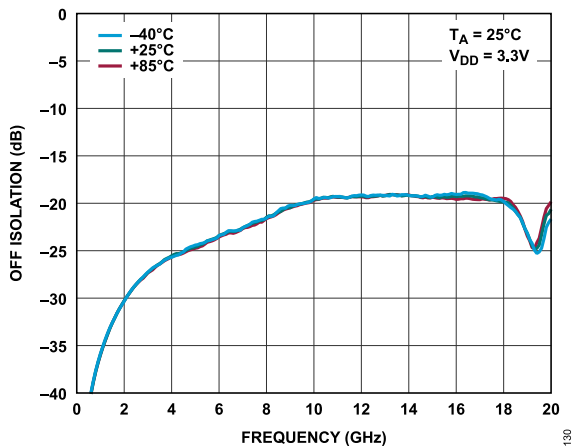


Figure 33. Off Isolation vs. Frequency over Temperature, RF1 to RFC On

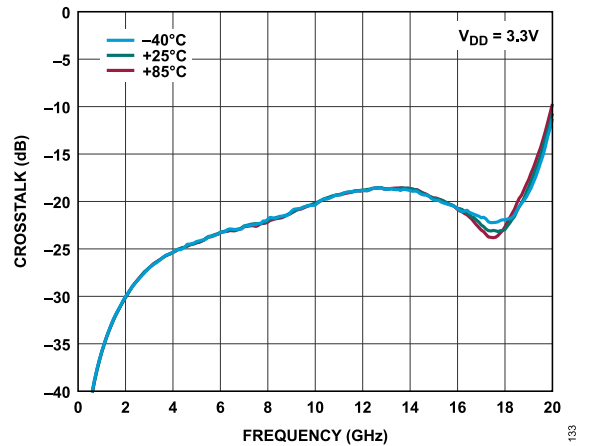


Figure 36. Crosstalk vs. Frequency over Temperature (RF2 to RF1)

TYPICAL PERFORMANCE CHARACTERISTICS

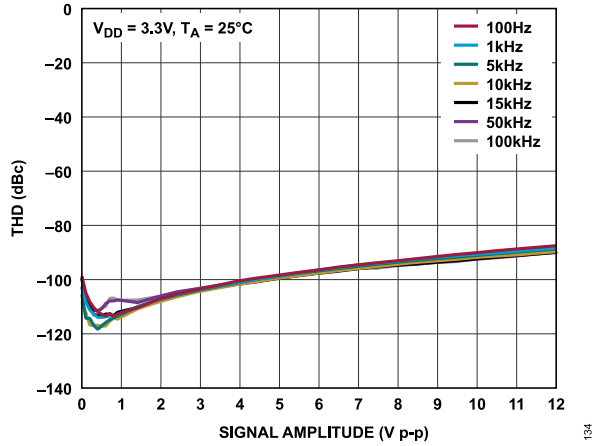


Figure 37. THD vs. Signal Amplitude ($R_L = 300 \Omega$, Signal Source Impedance = 20Ω)

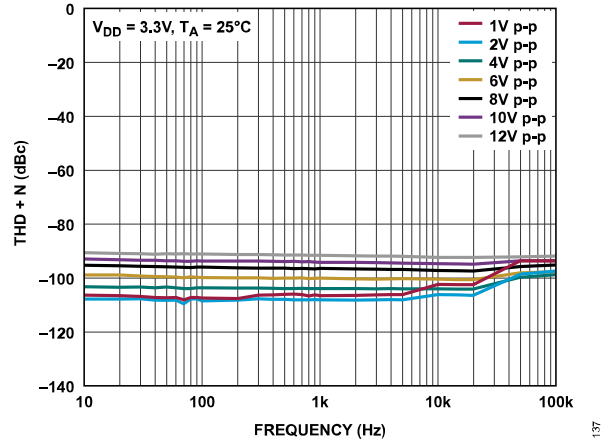


Figure 40. THD + N vs. Frequency ($R_L = 300 \Omega$, Signal Source Impedance = 20Ω)

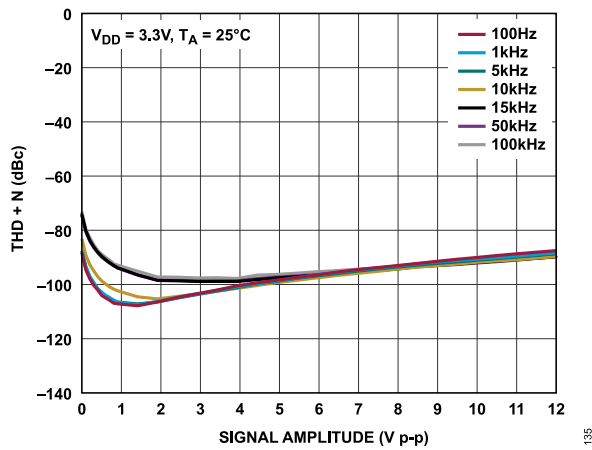


Figure 38. THD + N vs. Signal Amplitude ($R_L = 300 \Omega$, Signal Source Impedance = 20Ω)

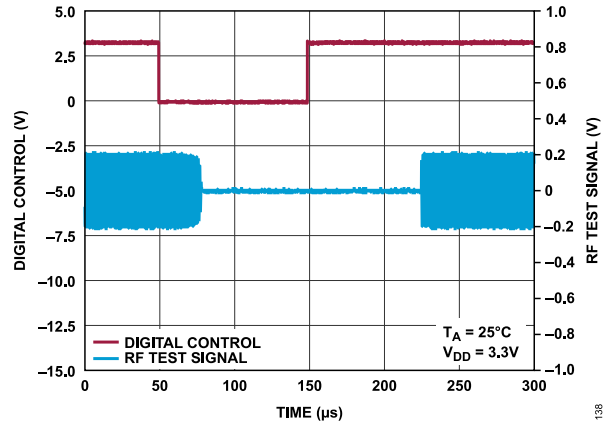


Figure 41. Digital Control and RF Test Signal vs. Time ($V_{DD} = 3.3 V$)

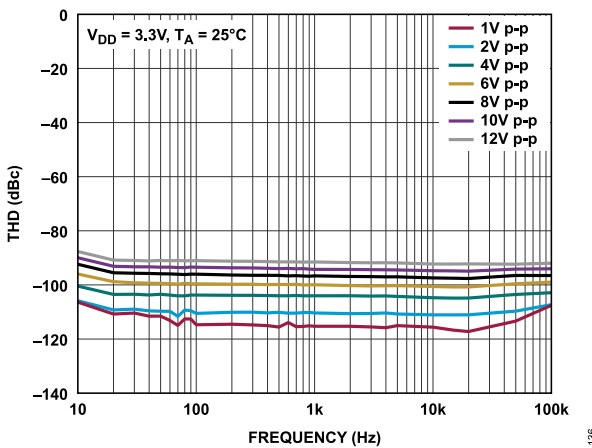


Figure 39. THD vs. Frequency ($R_L = 300 \Omega$, Signal Source Impedance = 20Ω)

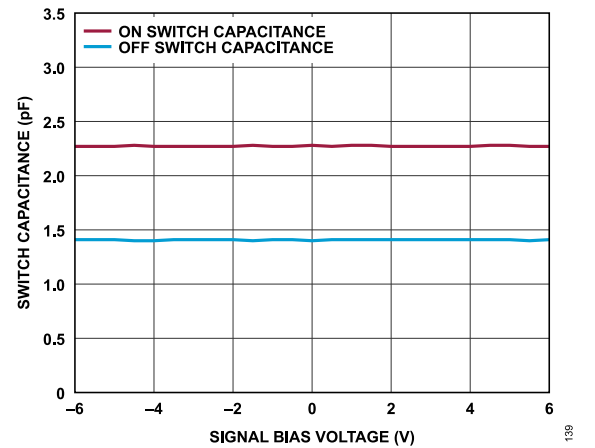


Figure 42. Switch Capacitance vs. Signal Bias Voltage ($V_{DD} = 3.3 V$, $T_A = 25^\circ C$)

TYPICAL PERFORMANCE CHARACTERISTICS

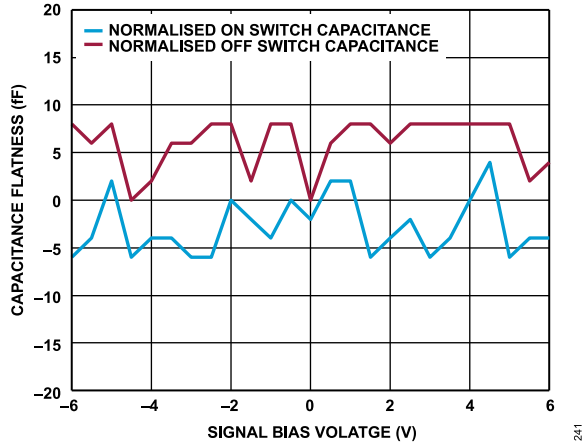


Figure 43. Capacitance Flatness vs. Signal Bias Voltage ($V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$)

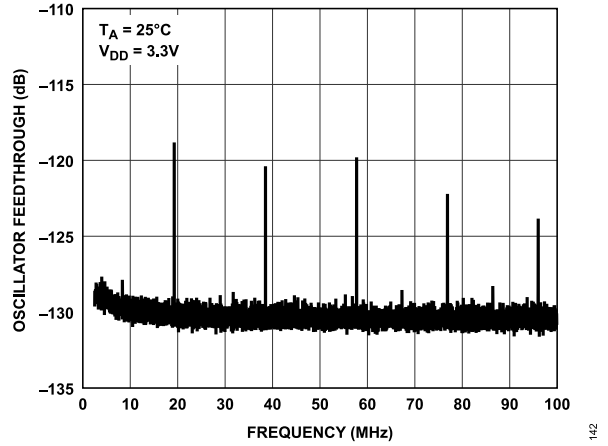


Figure 46. Oscillator Feedthrough vs. Frequency, Wide Bandwidth ($V_{DD} = 3.3\text{ V}$)

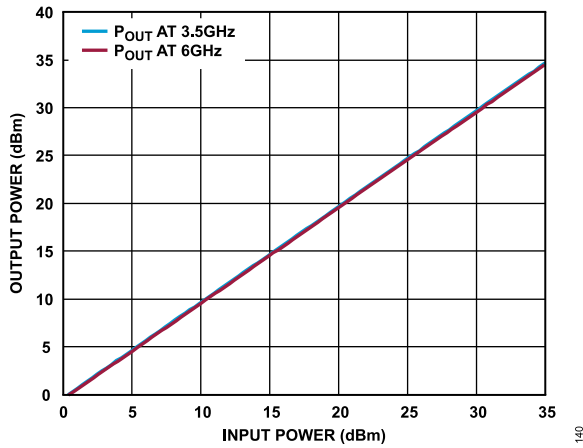


Figure 44. Output Power (P_{OUT}) vs. Input Power (P_{IN}) ($V_{DD} = 3.3\text{ V}$)

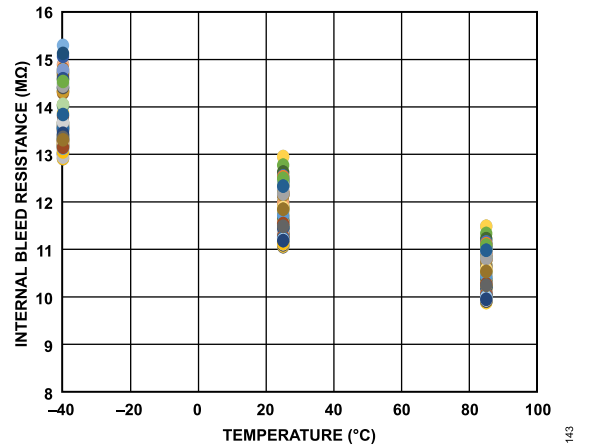


Figure 47. Internal Bleed Resistor Distribution over Temperature

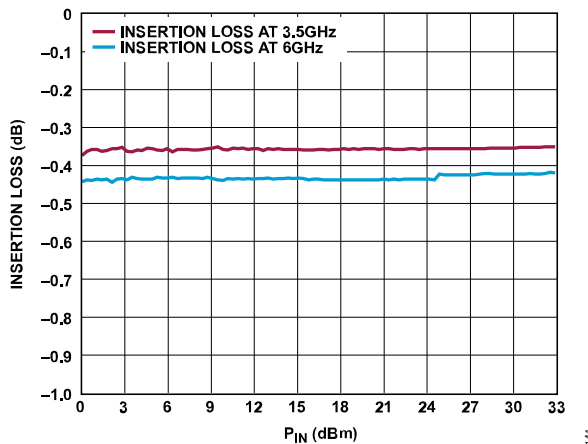


Figure 45. Insertion Loss vs. P_{IN}

THEORY OF OPERATION

SWITCH DESIGN

The ADGM1144 is a wideband SP4T switch fabricated using Analog Devices, Inc., MEMS switch technology. This technology enables high-power, low loss, low distortion GHz switches to be realized for demanding RF applications.

A key strength of the MEMS switch is that it simultaneously brings together best-in-class high-frequency RF performance and 0 Hz/DC precision performance. This combination coupled with superior reliability and a tiny surface mountable form factor make the MEMS switch the ideal switching solution for all RF and precision signal instrumentation needs.

The switches are electrostatically actuated MEMS structures. An on-board charge pump internally generates the bias voltage (80 V) used for actuation of the switch.

PARALLEL DIGITAL INTERFACE

The ADGM1144 can be controlled by a parallel-interface. Standard CMOS/low voltage transistor to transistor logic (LVTTTL) signals applied through this interface control the independent actuation and release of all of the switch channels of the ADGM1144.

Setting Pin 6 ($\overline{\text{PIN}}/\text{SPI}$) low enables the parallel control interface. Pin 1, Pin 2, Pin 3, and Pin 4 (IN1, IN2, IN3, and IN4) control the switching functions of the ADGM1144. When Logic 1 is applied to one of these pins, the corresponding switch turns on. Conversely, when Logic 0 is applied, the switch turns off. In SP4T mode, it is possible to connect more than one RFx input to RFC at a time. See [Table 7](#) for the truth table.

When no supply voltage is applied to Pin 23 (VDD), all switches are in an indeterminate state.

Table 7. Truth Table in Parallel Digital Interface Mode

IN1	IN2	IN3	IN4	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
0	0	0	0	Off	Off	Off	Off
0	0	0	1	Off	Off	Off	On
0	0	1	0	Off	Off	On	Off
0	0	1	1	Off	Off	On	On
0	1	0	0	Off	On	Off	Off
0	1	0	1	Off	On	Off	On
0	1	1	0	Off	On	On	Off
0	1	1	1	Off	On	On	On
1	0	0	0	On	Off	Off	Off
1	0	0	1	On	Off	Off	On
1	0	1	0	On	Off	On	Off
1	0	1	1	On	Off	On	On
1	1	0	0	On	On	Off	Off
1	1	0	1	On	On	Off	On
1	1	1	0	On	On	On	Off
1	1	1	1	On	On	On	On

THEORY OF OPERATION

SPI DIGITAL INTERFACE

The ADGM1144 can be controlled by an SPI digital interface when Pin 6 ($\overline{\text{PIN}}/\text{SPI}$) is high. SPI Mode 0 or Mode 3 can be used with the ADGM1144 and it operates with SCLK frequencies up to 10 MHz. The default mode when the SPI interface is active is the addressable mode, in which the registers of the ADGM1144 are accessed by a 16-bit SPI command that is bounded by the state of $\overline{\text{CS}}$. The ADGM1144 can also operate in daisy-chain mode.

The SPI interface pins of the ADGM1144 are $\overline{\text{CS}}$, SCLK, SDI, and SDO. Hold $\overline{\text{CS}}$ low when using the SPI interface. The data on the SDI is captured on the rising edge of SCLK and data is propagated out of SDO on the falling edge of SCLK. The SDO has a push-pull output driver architecture and does not require pull-up resistors. When not pulled low by the ADGM1144, SDO is in a high-impedance state. The two available SPI operation modes are addressable mode and daisy-chain mode.

Addressable Mode

Addressable mode is the default mode for the ADGM1144 upon power up. A single SPI frame can only be in addressable mode by a $\overline{\text{CS}}$ falling edge and the succeeding $\overline{\text{CS}}$ rising edge. It is comprised of 16 SCLK cycles. The timing diagram for Addressable Mode is seen in Figure 48 for SPI Mode 0.

The first SDI bit indicates if the SPI command is a read or write command. The next 7 bits determine the target register address. The remaining 8 bits provide the data to the addressed register. The last 8 bits are ignored during a read command because during these clock cycles SDO propagates out the data contained in the addressed register.

In Mode 0, during any SPI command, SDO sends out 8 alignment bits on the $\overline{\text{CS}}$ falling edge and the first seven SCLK falling edges (in Mode 3, the first SCLK falling edge is ignored, as shown in Figure 49) The alignment bits observed at SDO are 0x25.

The switch data register address is determined by the eighth SCLK rising edge. The switch data register propagates out on SDO from the eighth to the 15th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

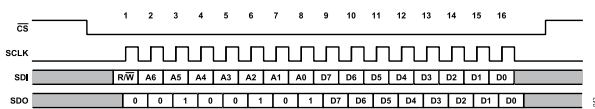


Figure 48. Addressable Mode Timing Diagram (Mode 0)

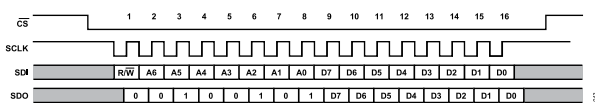


Figure 49. Addressable Mode Timing Diagram (Mode 3)

Daisy-Chain Mode

The connection of several ADGM1144 devices in a daisy-chain configuration is possible. All devices share the same $\overline{\text{CS}}$ and SCLK line, and the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an 8-cycle delayed version of SDI.

The ADGM1144 can only enter daisy-chain mode from the addressable mode by sending the 16-bit SPI command (0x2500) (see Figure 50). When the ADGM1144 receives this command, the SDO of the ADGM1144 devices sends out the same command. This is because the alignment bits at SDO are 0x25. These alignment bits allow multiple daisy connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 51. When $\overline{\text{CS}}$ goes high, Device 1 writes Command0[7:0] to its switch data register, Device 2 writes Command1[7:0] to its switches, and so on. The SPI block uses the last 8 bits it received through SDI to update the switches. After entering daisy-chain mode, the first 8 bits sent out by SDO are 0x00. When $\overline{\text{CS}}$ goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out on SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before $\overline{\text{CS}}$ goes high. When this is not the case, the SPI interface sends the last 8 bits received to the switch data register.

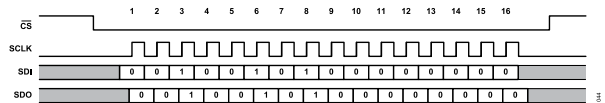
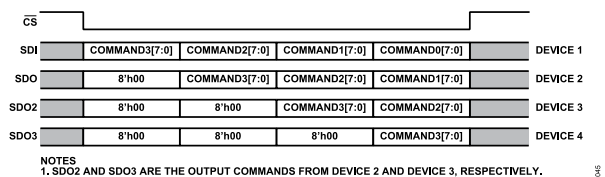


Figure 50. SPI Command to Enter Daisy-Chain Mode



NOTES
1. SDO2 AND SDO3 ARE THE OUTPUT COMMANDS FROM DEVICE 2 AND DEVICE 3, RESPECTIVELY.

Figure 51. Example of a SPI Frame when Three ADGM1144 Devices are Connected in Daisy-Chain Mode

Hardware Reset

The digital circuitry of the ADGM1144 goes through an initialization phase during VDD power up. To hardware reset the device, power cycle the VDD input. After power-up or a hardware reset, ensure there is a minimum of 10 μs from the time of power-up or reset before any SPI command is issued. Ensure that the V_{DD} does not drop out during the 10 μs initialization phase because it may result in incorrect operation of the ADGM1144.

THEORY OF OPERATION

Internal Error Status

Where an internal error is detected in the device, it is flagged in the internal error status bits, Bits[7:6], of the SWITCH_DATA register. An internal error results from an error in the configuration of the device at power-up.

INTERNAL OSCILLATOR FEEDTHROUGH

The ADGM1144 has an internal oscillator running at a nominal frequency of 10 MHz. This internal oscillator drives the charge-pump circuitry that provides the actuation voltage for each of the switch gate electrodes. Although this oscillator is very low power, the 10 MHz signal is coupled to the switch and can be considered a noise spur on the switch channels. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically -123 dBm when one switch is on. The V_{DD} level and temperature changes affect the frequency of the noise spur. For the maximum and minimum frequency range over the temperature range and voltage-supply range, see Table 1.

INTERNAL OSCILLATOR FEEDTHROUGH MITIGATION

In normal operation, the 80 V actuation voltage is supplied by the driver IC. Setting the EXT_D_EN pin (Pin 7) low enables the built-in 10 MHz oscillator. This setting enables the charge-pump circuitry to generate the 80 V required for MEMS switch actuation. The internal oscillator is a source of noise that couples through to the RF ports. The magnitude of this feedthrough noise spur is specified in Table 1 and is typically -123 dBm when one switch is on. The internal oscillator feedthrough can be eliminated by setting the EXT_D_EN pin high, which disables the internal oscillator and charge-pump circuitry. When the internal oscillator and charge-pump circuitry is disabled, the VCP pin (Pin 24) must be driven with 80 V DC (V_{CP_EXT}) from an external voltage supply, as outlined in Table 6, which is required for MEMS switch actuation. The switch can still be controlled by the digital logic interface pins.

LOW POWER MODE

Setting the EXT_D_EN pin high shuts down the internal oscillator. The ADGM1144 enters the low power quiescent state, drawing only 50 μ A maximum supply current.

TYPICAL OPERATING CIRCUIT

Figure 52 shows the typical operating circuit for the ADGM1144 as it is used in the EVAL-ADGM1144SDZ. The VDD pin is connected to 3.3 V. No decoupling capacitor is required on the VDD pin (Pin 23). The VDD pin has an internal decoupling capacitor connected to ground in the package. RFGND is separated from AGND internally in the device.

It is recommended to connect RFGND to AGND using one large pad on the PCB to short together EP1 and EP2. EP1 and EP2 are not connected internally. Figure 52 shows the ADGM1144 configured to use the internal oscillator as the reference clock to the

driver IC control circuit. Alternatively, set Pin 7 (EXT_D_EN) high and apply 80 V DC directly to Pin 24 to disable the internal oscillator and eliminate all oscillator feedthrough. The switches can then be controlled as normal by the logic control interface, IN1 to IN4 (Pin 1 to Pin 4).

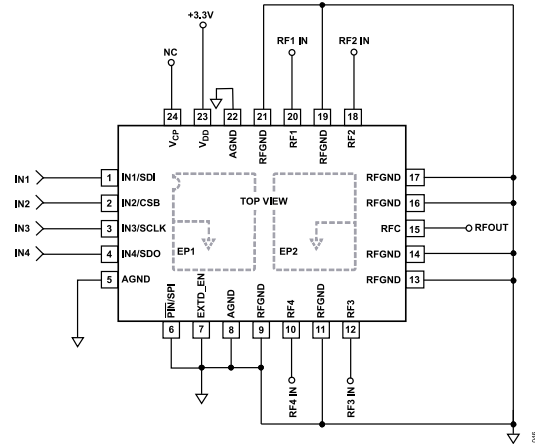


Figure 52. ADGM1144 Typical Operating Circuit in Parallel Digital Interface Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

The ADGM1144 can operate with unipolar supplies between 3.0 V and 3.6 V.

The device is fully specified at a 3.3 V analog supply voltage.

POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a unipolar power solution for the ADGM1144 is shown in Figure 53. The ADP7142 is a low dropout linear regulator that operates from 2.7 V to 40 V and is ideal for regulation of high performance analog and mixed-signal circuits operating from 39 V down to 1.2 V rails. The ADP7142 has 11 μ V rms output noise independent of the output voltage. The ADP7142 can be used to power the supply rail for the ADGM1144, a microcontroller, and/or other devices in the signal chain.

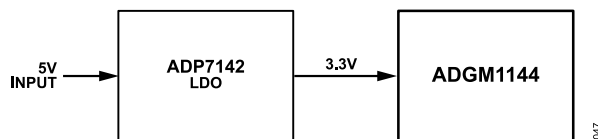


Figure 53. Unipolar Power Solution

If low noise performance at the power supply is required, the ADP7142 can be replaced by the LT1962 or the LT3045-1.

Table 8. Recommended Power Management Devices

Product	Description
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
LT1962	300 mA, low noise, micropower, LDO regulator
LT3045-1	20 V, 500 mA, ultra-low noise, ultra-high PSRR linear regulator with voltage for input to output control (VIOC)

HIGH-SPEED DIGITAL LOOPBACK

Testing high-speed input and output (HSIO) interfaces, such as peripheral component interconnect express 4.0 (PCIe 4.0) and PCIe 5.0, in a high volume manufacturing environment is a challenge. A common approach to validate an HSIO interface is the implementation of a high-speed loopback test method. This incorporates both high-speed and DC test paths in one configuration.

To perform high-speed loop back testing, generally a pseudorandom bit sequence (PRBS) is transmitted at high speed from the transmitter and received at the receiver end after being looped back on the load board or test board. At the receiver end, the sequence is analyzed to calculate the bit error rate (BER).

DC parametric tests are performed on the input and output pins, such as a continuity test and a leakage test, to ensure device functionality. To perform these tests, the input/output pins of the DUT must be connected directly to a DC instrument where the DC measurement of the input/output pin is executed.

The ADGM1144 offers both high speed digital and DC testing capability with superior density in a small 5.00 mm \times 4.00 mm \times 1.0 mm LGA package, as shown in Figure 54. The MEMS switch also enables communication from the tester to the device under test (DUT). The ADGM1144 provides excellent performance from DC to 16 GHz, which allows the switch to handle both high-speed signals up to 32 Gbps and precision DC signals.

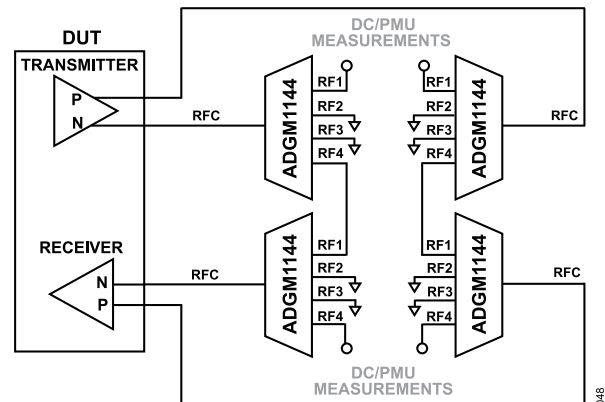


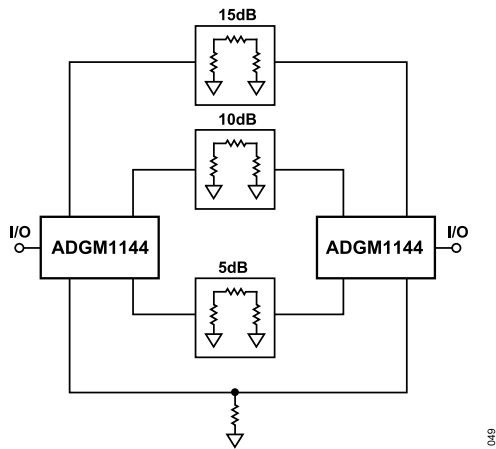
Figure 54. ADGM1144 Enabling Both High Speed Digital and DC Testing

SWITCHABLE RF ATTENUATOR

It is common to see RF attenuator networks used in RF instrumentation equipment, such as vector network analyzers, spectrum analyzers, and signal generators. Routing RF signals through an attenuator enables the equipment to accept higher power signals and increase the dynamic range of the instrument. In RF attenuation applications, such as vector network analyzers, spectrum analyzers, and signal generators, maintaining the bandwidth of the signal after it passes through the network is critical. Any degradation of the signal reduces the performance of the equipment. Therefore, the RF characteristics of the switches used for routing are integral to the quality of an attenuator network.

The ADGM1144 MEMS switch is suited for use as a switchable RF attenuator due to its low flat insertion loss, wide RF bandwidth, and high reliability. The ADGM1144, as an SP4T switch, also provides added flexibility. Figure 55 shows an example of an attenuation network configuration using two ADGM1144 switches and three different attenuators. The fourth channel of the switches is used as a nonattenuated route.

APPLICATIONS INFORMATION



049

Figure 55. Switching RF Attenuators Using ADGM1144 MEMS Switches

CRITICAL OPERATIONAL REQUIREMENTS

SYSTEM ERROR CONSIDERATIONS DUE TO ON-RESISTANCE DRIFT

The R_{ON} performance of the ADGM1144 is affected by device to device variation, channel to channel variation, cycle actuations, settling time post turn on, bias voltage, and temperature changes.

In a $50\ \Omega$ system, the on-resistance drift over switch actuations (ΔR_{ON}) can introduce system inaccuracy. Figure 56 shows the ADGM1144 connected with the load in a $50\ \Omega$ system, where R_S is the source impedance and V_S is the voltage source. To calculate the system error caused by the ADGM1144 on-resistance drift, use the following equation:

$$\text{System Error (\%)} = \Delta R/R_L$$

where:

ΔR is the ADGM1144 on-resistance drift.

R_L is the load impedance.

The ADGM1144 on-resistance drift also affects insertion loss, which must be considered when using the device. To calculate the on-resistance impact on insertion loss, use the following equation:

$$\text{Insertion Loss} = 10\log(1 + (\Delta R/R_L))$$

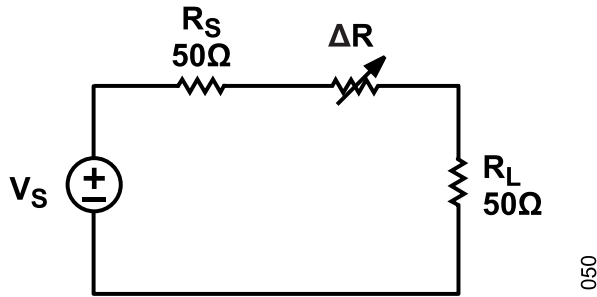


Figure 56. $50\ \Omega$ System Representation Where the ADGM1144 Is Connected with the Load

Table 9. System Error and Insertion Loss Error Due to ADGM1144 R_{ON} Drift

On-Resistance Drift	System Error (%)	Insertion Loss Error (dB)
0.7	1.4	0.06
2	4	0.17

The on-resistance drift over time specification is $-0.32\ \Omega$ (maximum) measured after 100 ms, as shown in Figure 13 to Figure 20. According to the plots, the on-resistance drift over time is $-0.06\ \Omega$ (typical) after 100 ms. The on resistance of the ADGM1144 typically drifts by $-0.04\ \Omega$ per decade. For example, after 100 ms, the on resistance drifts $-0.06\ \Omega$. After 1 sec, the on resistance drifts $-0.1\ \Omega$, and after 10 sec, it drifts $-0.14\ \Omega$. Therefore, after 1000 sec, the on resistance is expected to drift by $-0.22\ \Omega$.

ON-RESISTANCE SHIFT DUE TO TEMPERATURE SHOCK POST ACTUATIONS

When the switch is actuated multiple times at one temperature, and if there is a sudden shift in this temperature, a large shift is shown in the switch. Figure 57 shows the absolute R_{ON} performance of the population of devices over actuations at different actuation frequencies. During this measurement, the switch is actuated at 85°C and the switch R_{ON} is measured at 25°C . Actuating the switch at 85°C and measuring R_{ON} at 25°C is the most severe condition for the ADGM1144 R_{ON} drift over actuations.

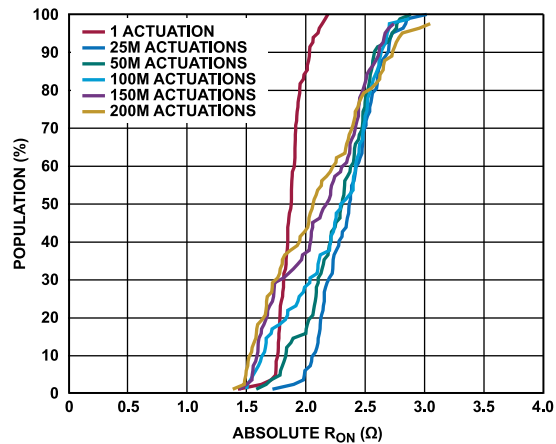
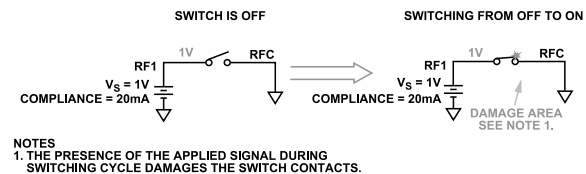


Figure 57. Population vs. Absolute R_{ON} , Switch Actuated at 85°C and R_{ON} Measured at 25°C , Actuation Frequency = 289 Hz, $V_{DD} = 3.3\ \text{V}$

HOT SWITCHING

Hot switching occurs by cycling the switch on or off with an excessive voltage or current applied to the switch. The presence of the applied signal during the switching cycle damages the switch contacts. Hot switching damage is dependent on the current or the voltage levels. Hot switching causes a significant reduction in the cycle lifetime of the switch, as shown in Figure 61 and Figure 63. Figure 58 shows the hot switching condition when the switch is turned on with 1 V present at the switch terminal during switching. With a voltage across an off switch, damage can occur as the contact or switch closes.



NOTES
1. THE PRESENCE OF THE APPLIED SIGNAL DURING SWITCHING CYCLE DAMAGES THE SWITCH CONTACTS.

Figure 58. Hot Switching Condition When Turning the Switch from Off to On State

Figure 59 shows the hot switching condition when the switch is turned off with 10 mA passing through the switch during switching. With current passing through an on switch, damage can occur as the contact or switch opens.

CRITICAL OPERATIONAL REQUIREMENTS

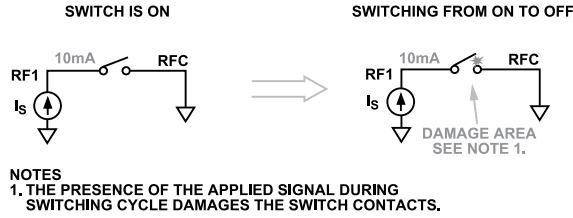


Figure 59. Hot Switching Condition When Turning the Switch from On to Off State

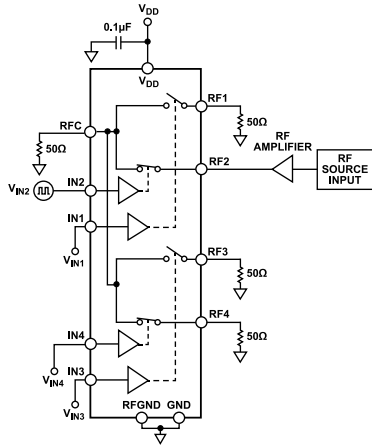


Figure 60. RF Hot Switching Setup

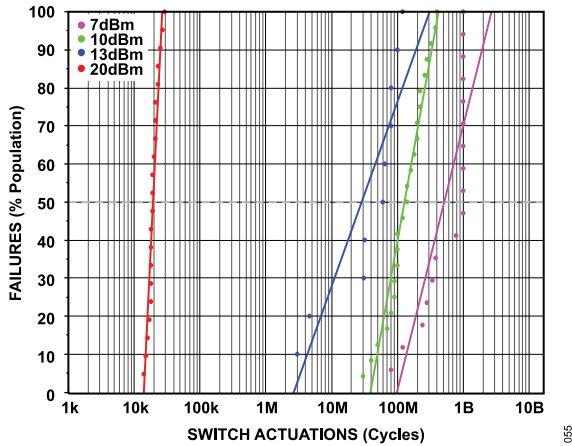


Figure 61. RF Hot Switching Probability Distribution on Log Normal (RF Power = Continuous Wave, Terminated into 50 Ω, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$)

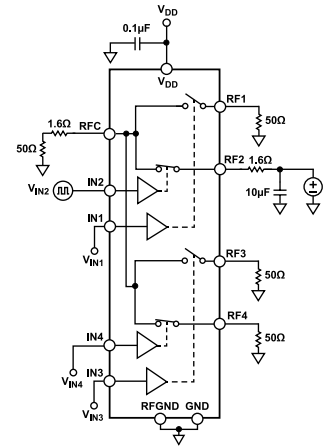


Figure 62. DC Hot Switching Setup

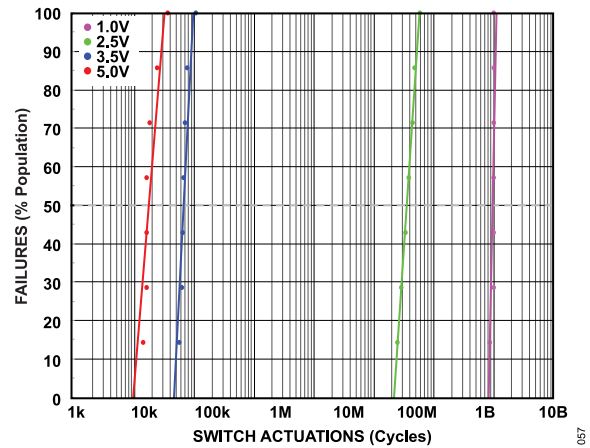


Figure 63. DC Hot Switching Probability Distribution on Log Normal (Terminated into 50 Ω, $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$)

HANDLING PRECAUTIONS

ESD Precautions

All RF pins (RF1, RF2, RF3, RF4 and RFC) of the ADGM1144 pass the following ESD limits:

- ▶ 150 V, Class 0 HBM, ANSI/ESDA/JEDEC JS-001-2010
- ▶ 500 V FICDM

All the RFx pins are rated to 500 V FICDM, making the device safe for automated handling and assembly process. Take standard ESD precautions during manufacturing.

The 150 V HBM rating for the RF1, RF2, RF3, RF4 and RFC pins of the ADGM1144 is susceptible to ESD surge due to human body contact. Add ESD protection if human body contact is expected.

CRITICAL OPERATIONAL REQUIREMENTS

Electrical Overstress (EOS) Precautions

The ADGM1144 is susceptible to EOS. Therefore, observe the following precautions:

- ▶ The ADGM1144 is an ESD sensitive device that observes all normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps or other ESD control devices, and storing unused devices in conductive foam.
- ▶ Avoid running measurement instruments, such as digital multi-meters (DMMs), in autorange modes. Some instruments can generate large transient compliance voltages when switching between ranges.
- ▶ Use the highest practical DMM range setting (the lowest resolution) for resistance measurements to minimize compliance voltages, particularly during switching.
- ▶ Coaxial cables can store charge and lead to EOS when directly connected to the switch. Discharge cables before connecting directly to the switch.
- ▶ Avoid connecting capacitive terminations directly to the switch, as shown in Figure 64. A shunt capacitor can store a charge that can potentially lead to hot switching events when the switch opens or closes, affecting the lifetime of the switch.

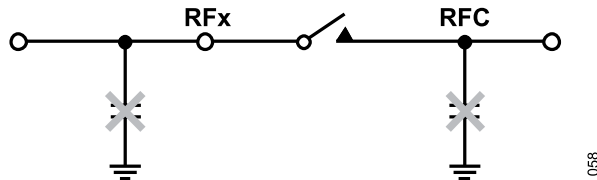


Figure 64. Avoid Large Capacitor Directly Connected to the Switch

Mechanical Shock Precautions

The ADGM1144 passes Group D mechanical shocks tests, as detailed in the Absolute Maximum Ratings section. Do not use the device if it is dropped. To reduce excessive mechanical shock and ESD events, avoid handling of loose devices, as outlined in Figure 65.

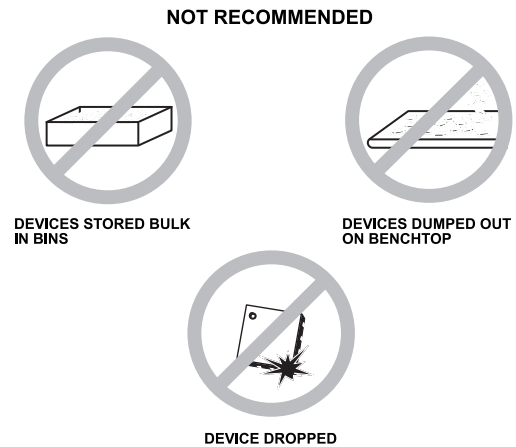


Figure 65. Situations to Avoid During Handling

SOLDER STENCIL RECOMMENDATION

To avoid solder voids under the ADGM1144, it is recommended to use a 0.0767 mm (3 mil) thick solder stencil with nano coating. The aperture size for the solder stencil must be 1:1, and divide the paste mask with multiple pads, as shown in Figure 66. Poor soldering can impact the RF performance of the ADGM1144.

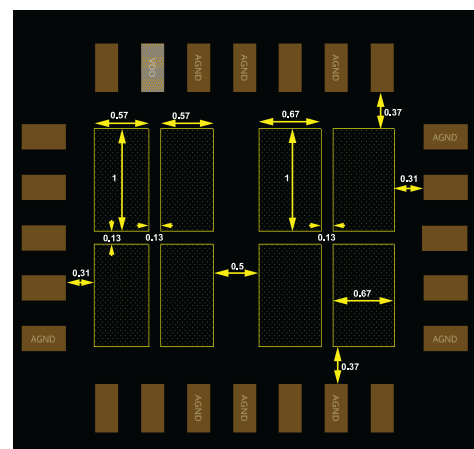


Figure 66. Solder Stencil Recommendation for ADGM1144 (Dimensions Shown in Millimeters)

REGISTER SUMMARY*Table 10. Register Summary*

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x20	SWITCH_DATA	INTERNAL_ERROR	RESERVED				SWITCH_DATA			0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x20, Reset: 0x00, Name: SWITCH_DATA

The switch data register controls the status of the two switches of the ADGM1144.

Table 11. Bit Descriptions for SWITCH_DATA

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	INTERNAL_ERROR		These bits determine if an internal error has occurred. 00 No error detected. 01 Error detected. 10 Error detected. 11 Error detected.	0x0	R
[5:4]	RESERVED		These bits are reserved. Set these bits to 0.	0x0	R
3	SW4_EN		Enable bit for Switch 4. 0 Switch 4 open. 1 Switch 4 closed.	0x0	R/W
2	SW3_EN		Enable bit for Switch 3. 0 Switch 3 open. 1 Switch 3 closed.	0x0	R/W
1	SW2_EN		Enable bit for Switch 2. 0 Switch 2 open. 1 Switch 2 closed.	0x0	R/W
0	SW1_EN		Enable bit for Switch 1. 0 Switch 1 open. 1 Switch 1 closed.	0x0	R/W

OUTLINE DIMENSIONS

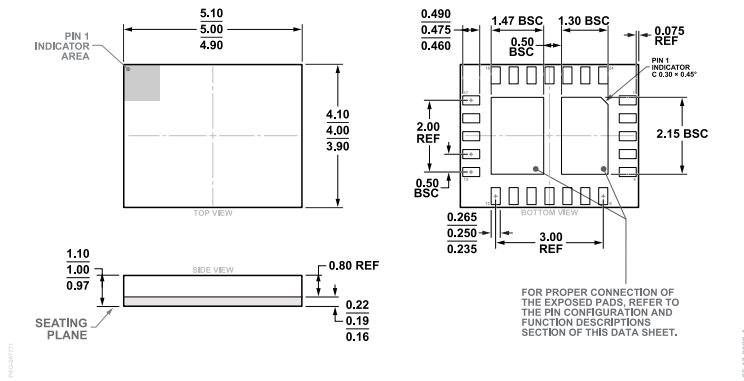


Figure 67. 24-Lead Land Grid Array [LGA] 5 mm × 4 mm Body and 1.0 mm Package Height (CC-24-11) Dimensions shown in millimeters

Updated: August 31, 2022

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity	Package Option
ADGM1144BCCZ-RL7	-40°C to +85°C	LGA/CASON/CH ARRAY SO NO LD	Reel, 1500	CC-24-11

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

Model ¹	Description
EVAL-ADGM1144SDZ	Evaluation Board

¹ Z = RoHS Compliant Part.