Non-Isolated Evaluation Board for the Si3402

1. Description

The Si3402 non-isolated evaluation board (Si3402-EVB Rev 1.41) is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application. The Si3402 is described more completely in the data sheet and application notes. This document describes the evaluation board. An evaluation board demonstrating the isolated application is described in the Si3402ISO-EVB user's guide.

2. Si3402 Board Interface

Ethernet data and power are applied to the board through the RJ-45 connector (J1). The board may be powered by the following:

- Connecting a dc source to 1, 2 and 3, 4 (either polarity)
- Connecting a dc source to 4, 5 and 7, 8 (either polarity)
- Using an 802.3af-compliant PSE such as Phihong PSA16U-480 (PoE)

The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary is brought out to the test points. The dc output is at connectors J4(+) and J3(–).

Boards are generally shipped configured to produce +5 V but can be configured for +3.3 V or other output voltages by changing resistors R5 and R6. Refer to "AN296: Using the Si3400/1/2 PoE PD Controllers in Isolated and Non-Isolated Designs" and its accompanying Excel® spreadsheet utility for more information. The only other test point provided is J6, which is the power loss (PLOSS) indicator.

3. Schematics

The Si3402-EVB board schematics and layers are shown in Figures 1 through 6. The Si3402-EVB is normally populated for 5 V output, Class 3 signature, and without the diode bridge bypass recommended for higher power levels. Use the ordering option Si3402-C4-EVB for 5 V output, Class 4 signature, and diode bridge bypass for higher power levels.
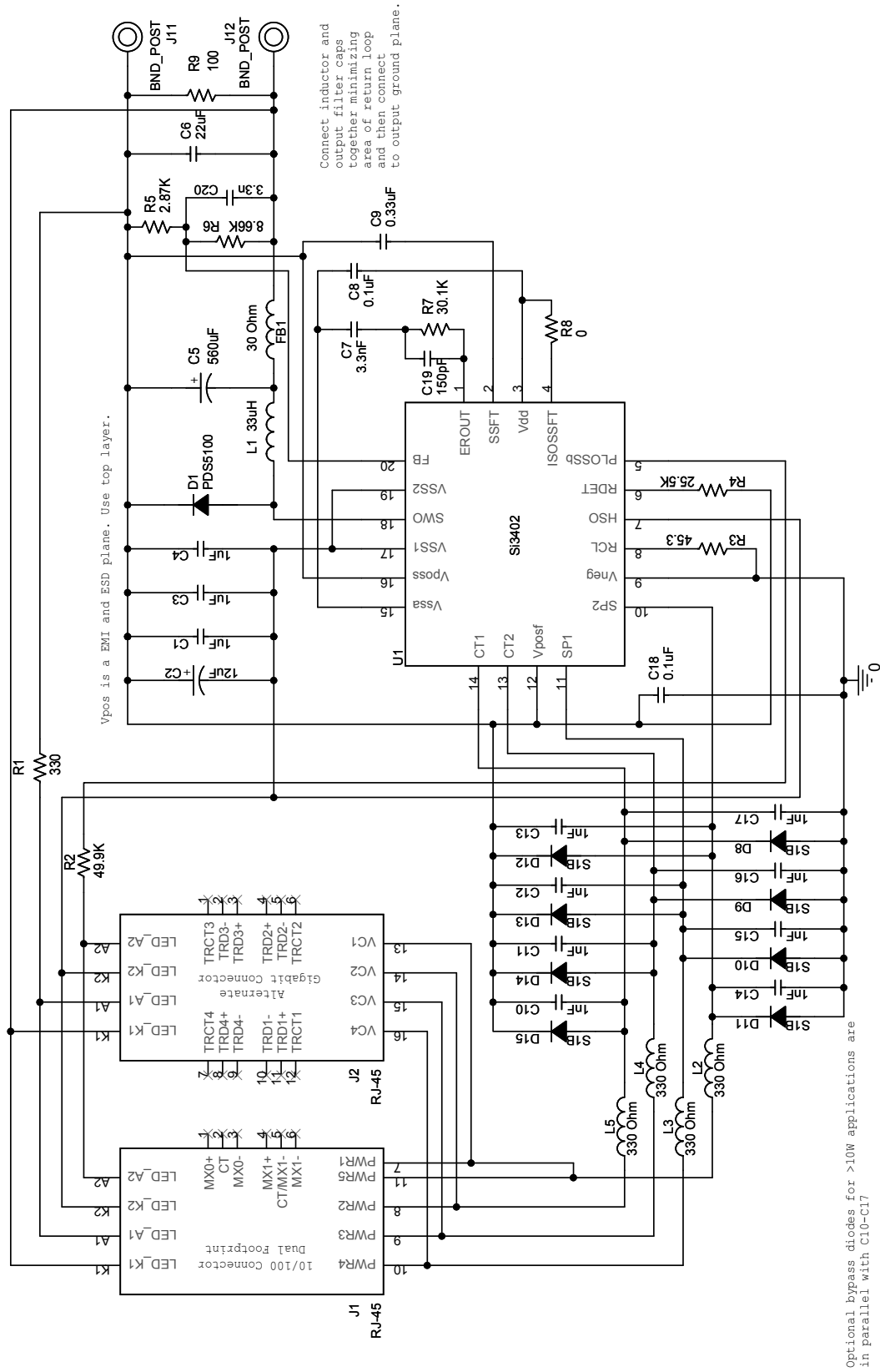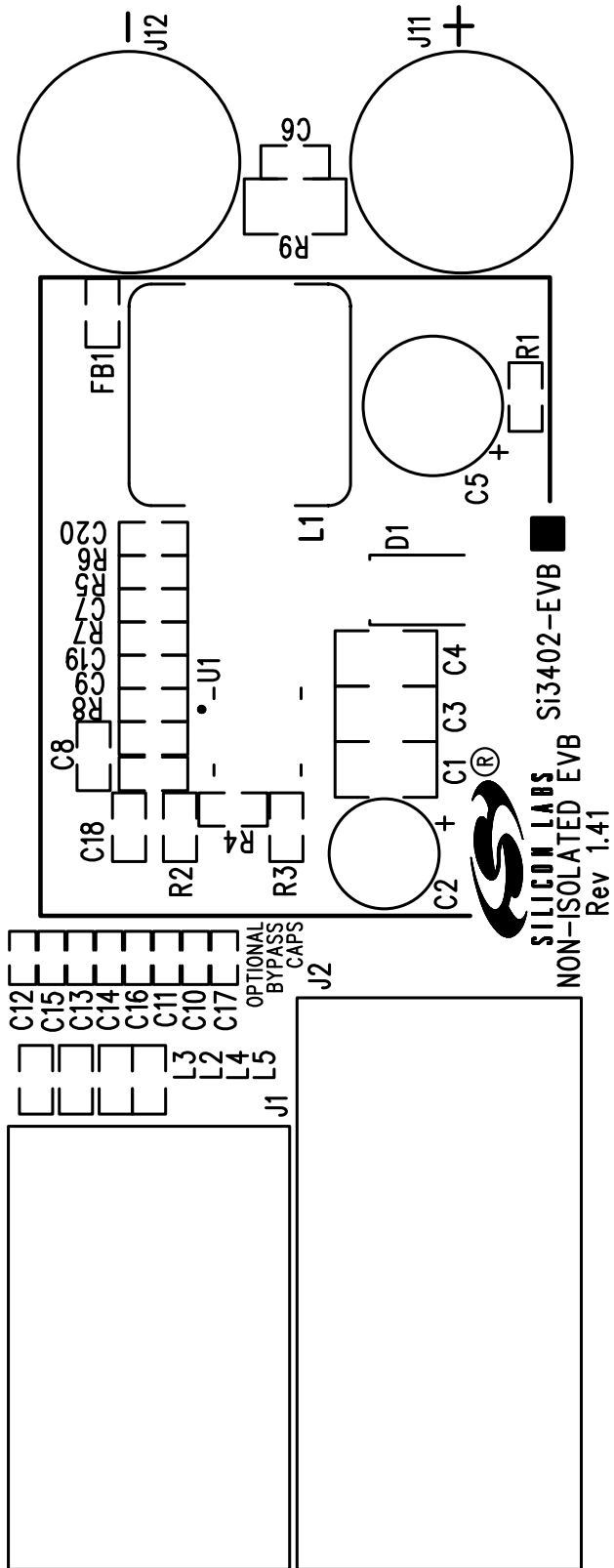
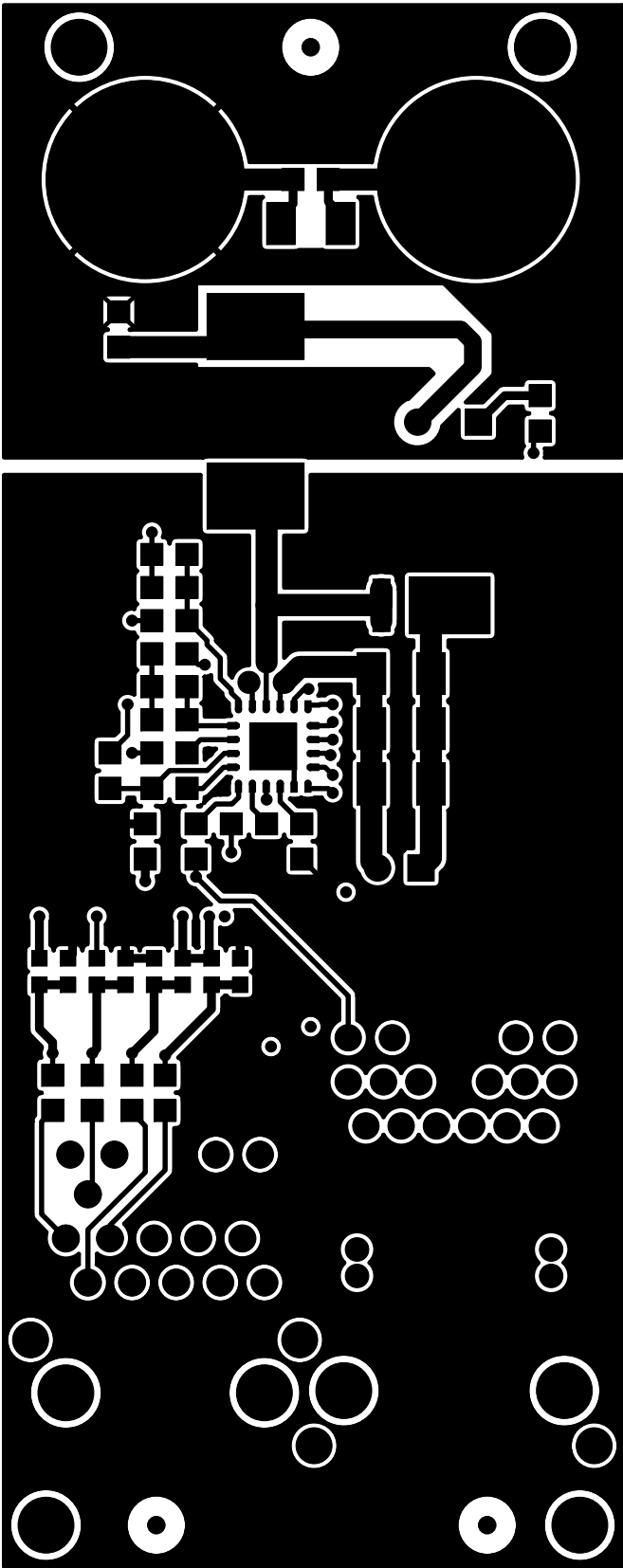Figure 1. Si3402 Schematic—5 V, Class 3 PD

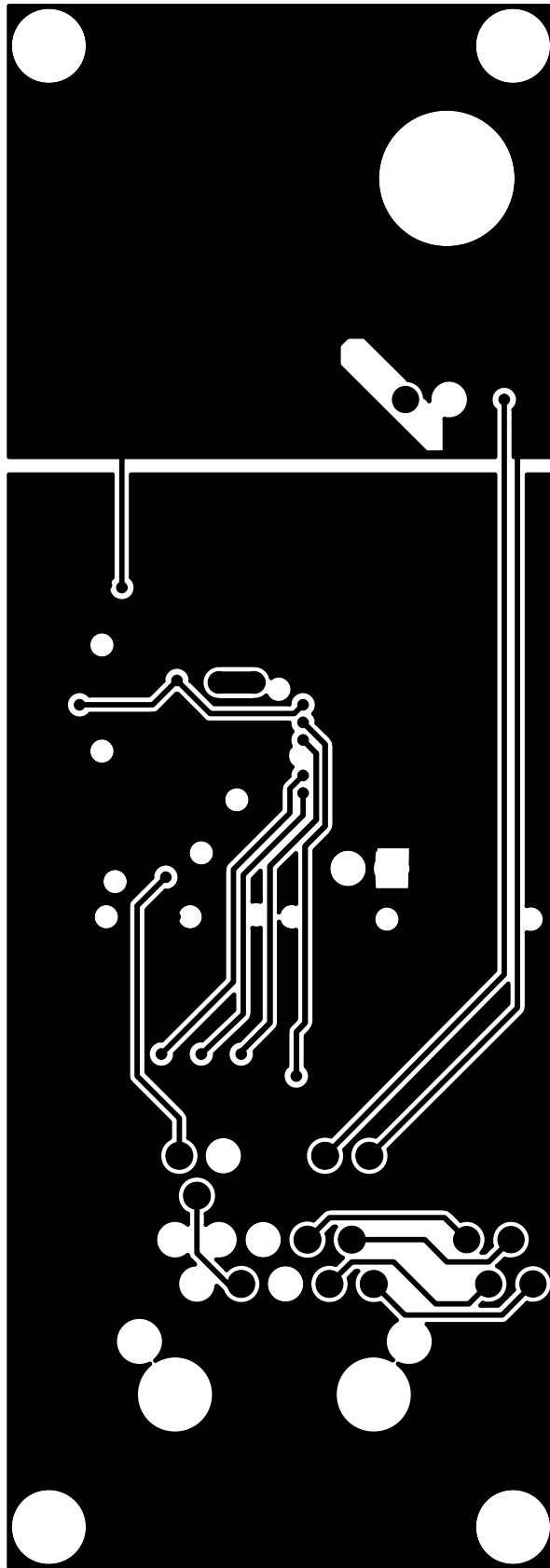**Figure 2. Top Silkscreen**

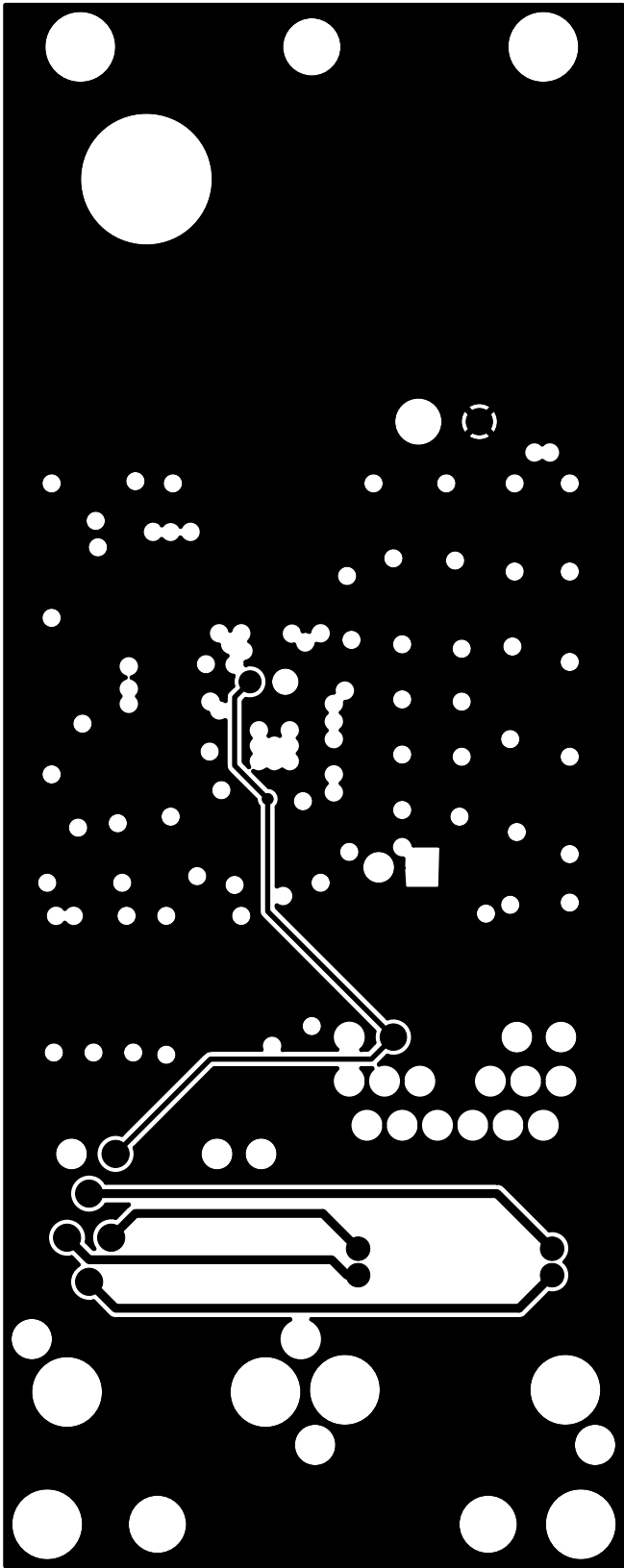**Figure 3. Top Layer**

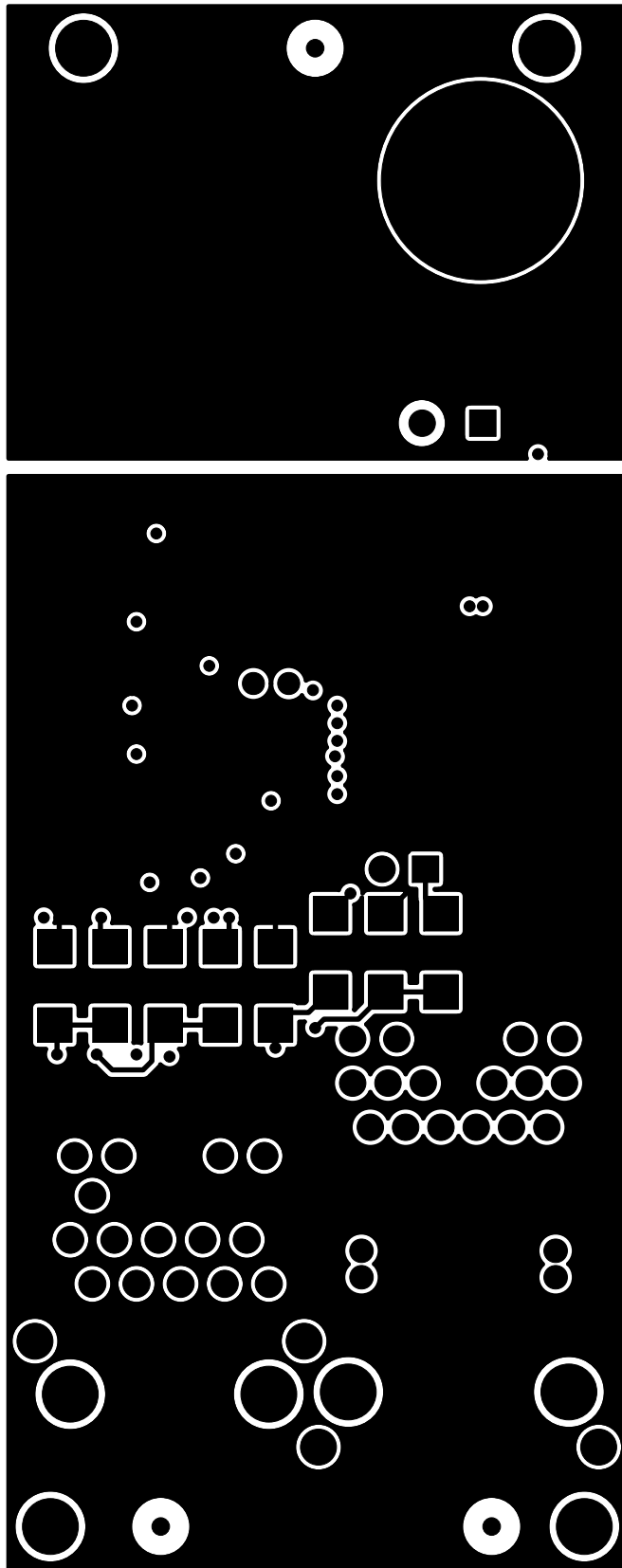**Figure 4. Internal 1**

Figure 5. Internal 2

Figure 6. Bottom Layer

Si3402-EVB

4. Bill of Materials

Table 1 is the BOM listing for the standard 5 V evaluation board with a popular option for Class 3 or Class 4.

Table 1. Si3402-EVB Bill of Materials

Item	NI	Qty	Reference	Value	Rating	Tol	Dielectric	PCB Footprint	Manufacturer Part Number	Manufacturer
1		3	C1,C3,C4	1 µF	100 V	10%	X7R	1210	GRM32ER72A105KA01 C1210X7R101105K	Murata Venkel
2		1	C2	12 µF	12 µ		Al Elec	thru hole	EEUFC2A120 100ME12AX	Panasonic Sanyo
3		1	C5	560 µF		±20%		C3.5X8MM-RAD	EEUFM0J561	Panasonic
4		1	C6	22 µF	6.3 V		X5R	0805	GRM21BR60J226M C0805X5R6R3226K	Murata Venkel
5		2	C7,C20	3.3 nF		±10%		C0603	C0603X7R160-332K	Venkel
6		1	C8	100 nF	16 V		X7R	0805	C0805X7R160104K	
		1	C9	0.33 µF	16 V		X7R		C0805X7R160-334KNE	Venkel
7[1]		8	C10,C11,C12, C13,C14,C15, C16,C17	1000 pF	100 V	10%		0603		Venkel
		1	C18	0.1 µF	100 V	10%	X7R	0805	C0805X7R101104K	Venkel
		1	C19	150 pF	16 V	10%	X7R	0805	C0805X7R160151K	Venkel
8		1	D1	PDS5100				PDI5	PDS5100	Diodes Inc.
9		1	J1	MagJack				RJ45	SI-52003-F RJSE1R8090B-R	BelFuse Delta
10		2	J11,J12	CON1					101	Abbatron HH Smith
11		1	L1	33 µH					MSS1278-333ML	Coilcraft
12		1	FB1	22 Ω	6000 mA			L0805	BLM21PG220SN1B	MuRata
13		4	L2,L3,L4,L5	330 Ω			Ferrite	0805	BLM21PG331SH1	Murata
14		1	R1	330 Ω				0805	CR0805-10W3300F	Venkel
15		1	R2	49.9 kΩ	100 V			0805	CR0805-8W4992F	Venkel
16		1	R3	30.9 Ω (Class 4)				0805	CR0805-10W-30R9F	Venkel
				45.3 Ω (Class 3)				0805	CR0805-10W-45R3F	Venkel
17		1	R4	25.5 kΩ				0805	CR0805-10W2552F	Venkel
18		1	R5	2.87 kΩ				0805	CR0805-10W2871F	Venkel
19		1	R6	8.66 kΩ				0805	CR0805-10W8661F	Venkel
20		1	R7	30.1 kΩ				0805	CR0805-10W3012F	Venkel
		1	R8	0 Ω				0805	CR0805-000	Venkel
21		1	RLOAD	100 Ω	1/2 W	±1%		R1210	CR1210-2W-1000F	Venkel
22		1	U1	Si3402				5x5 QFN	Si3402	Silicon Labs
24[2]		8	D8,D9,D10,D11, D12,D13,D14, D15	S1B	1 A 100 V			SMB	S1B	Diodes Inc.
23	NI	5	J5,J6,J7,J8,J9	HEADER 1					Standard	

Notes:
1. C10–C17 are populated by default. See the "Surge" section in AN296 for more information.
2. Bypass diodes D8–D15 are populated for the Class 4 option.

5. BOM Options

The Si3402 non-isolated EVB has been compensated for eight different output voltage and filter combinations:

■ 3.3 V output standard ESR 1000 μF 6.3 V filter

■ 5 V output standard ESR 1000 μF 6.3 V filter

■ 9 output standard ESR 470 μF 16 V filter

■ 12 V output standard ESR 470 μF 16 V filter

■ 3.3 V output low ESR 560 μF 6.3 V filter

■ 5 V output low ESR 560 μF 6.3 V filter

■ 9 V output low ESR 330 μF 16 V filter

■ 12 V output low ESR 330 μF 16 V filter

For the standard ESR capacitor, the ESR increase at very low temperatures may cause a loop stability issue. A typical evaluation board has been shown to exhibit instability under very heavy loads at –20 °C. Due to self-heating, this condition is not a great concern. However, using a low ESR filter capacitor solves this problem (but requires some re-compensation of the feedback loop). The low ESR capacitor also improves load transient response and output ripple.

The Si3402 (non–isolated) EVB was designed with a very simple pole-zero compensation consisting of R7 and C7. Capacitors C19 and C20 can be added in parallel with resistors R6 and R7 for optimized performance.

The standard evaluation board is shipped with C19 and is optimized for a standard ESR filter capacitor for 5 V output.

The following table gives the options that have been tested for other situations.

V$_{OUT}$	R6 (To Adjust Output Voltage)	Filter Cap C5 (Type FM are Low ESR)	Filter Cap Part Number (Panasonic)	R7	C7	C19	C20
3.3 V	4.87 kΩ	1000 μF, 6.3 V	ECA0JM102	21 kΩ	4.7 nF	150 pF	NP
3.3 V	4.87 kΩ	560 μF, 6.3 V	EEUFM0J561	30.1 kΩ	4.7 nF	150 pF	4.7 nF
5.0 V	8.66 kΩ	100 0 μF, 6.3 V	ECA0JM102	30.1 kΩ	3.3 nF	150 pF	NP
5.0 V	8.66 kΩ	560 μF, 6.3 V	EEUFM0J561	30.1 kΩ	3.3 nF	150 pF	3.3 nF
9.0 V	18.2 kΩ	470 μF, 16 V	ECA1CM471	21 kΩ	4.7 nF	150 pF	NP
9.0 V	18.2 kΩ	330 μF, 16 V	EEUFM1C331	30.1 kΩ	4.7 nF	150 pF	3.3 nF
12.0 V	24.9 kΩ	470 μF, 16 V	ECA1CM471	30.1 kΩ	3.3 nF	150 pF	NP
12.0 V	24.9 kΩ	330 μF, 16 V	EEUFM1C331	30.1 kΩ	3.3 nF	150 pF	3.3 nF

Si3402-EVB

APPENDIX—SI3402 DESIGN AND LAYOUT CHECKLIST

Introduction

Although the EVB design is pre-configured as a Class 3 PD or Class 4 with a 5 V output, the schematics and layouts can easily be adapted to meet a wide variety of common output voltages and power levels.

The complete EVB design databases for the standard 5 V/Class 3 configuration are located at www.silabs.com/PoE under the "Documentation" link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Following are recommended design checklists that can assist in trouble-free development of robust PD designs.

Refer also to the Si3402 data sheet and AN296 when using the following checklists.

1. **Design Planning Checklist:**
    a. Determine if your design requires an isolated or non-isolated topology. For more information, see Section 4 of AN296.
    b. To begin integrating the Si3402 into your schematics, download the schematic and layout database for your particular isolation requirements from www.silabs.com/PoE.
    c. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3402 into your system design process.
    d. Determine your load's power requirements (i.e., V_{OUT} and I_{OUT} consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3402, choose the highest voltage used in your PD and then post regulate to the lower supply rails, if necessary.
    e. If your PD design consumes $\geq$10 W, bypass the Si3402's on-chip diode bridges with external diode bridges or discrete diodes. Bypassing the Si3402's on-chip diode bridges with external bridges or discrete diodes is required to help spread the heat generated in designs dissipating $\geq$10 W.
    f. Based on your required PD power level, select the appropriate class resistor value by referring to Table 2 of AN296. This sets the Rclass resistor (R3 in Figure 1 on page 2).

2. **Calculate design-specific external components (for all designs that are not for a 5 V, Class 3 output configuration):**
    a. To help guide the selection of the other application-specific external component values needed for your design's isolation requirements, access the Excel spreadsheet utility at the following address: https://www.silabs.com/products/power/poe/Pages/default.aspx
        i. Use the "Non-isolated" worksheet if your design is intended for a non-isolated output supply.
        ii. Use either the "Isolated Continuous" or the "Isolated Discontinuous" worksheets if your design is for an isolated output supply ("continuous" versus "discontinuous" mode is determined by the current value calculated in cell H11 of the spreadsheet).
    b. If your design is a 5 V output Class 3 design, you do *not* need to change any external components.
    c. To avoid potential performance issues for non 5 V output configurations, Silicon Labs strongly recommends using the exact components and component values shown and calculated in the Excel worksheets.

d. Begin entering your design targets in cells B9 through B13 of the worksheet:

    i. If appropriate, select the on-chip "diode bypass" option in cell B9 in the Excel spreadsheet utility. By entering a "1" in this cell, the Si3402's on-chip diodes are assumed to be bypassed with external diode bridges in your schematic. A "0" in this cell means the Si3402's on-chip diode bridges will be used.

    ii. Enter V_{IN} into cell B10. This voltage is the input voltage at the diode bridge output, which is 2 to 3 V less than the PSE input voltage or, typically, 46 V.

    iii. Enter your design's desired output current, I_O, in amperes, into cell B11.

    iv. Enter your design's desired output voltage, V_O, in volts, into cell B12.

    v. Enter your design's maximum ambient operating temperature in °C into cell B13.

e. If you are using the "Non-isolated" worksheet:

    i. The feedback resistor network values (R5 and R6) for your design are calculated and displayed in cells G13 and G12. Use these resistor values to update your schematic.

    ii. To use the default diode and inductor components used in the Si3402-EVB non-isolated schematic, Silicon Labs strongly recommends leaving each default values "as-is" in cells B15 through B18.

    iii. To ensure your design is operating within the acceptable operating ranges for all the external components used in your schematic, carefully review the calculated values found in cells B20 through B27.

    iv. Carefully review the calculated values in the Summary section (cells B29 through B33).

        1. Cell B29: PSE input voltage. Make sure the PSE input voltage is compatible with the PSE intended to power your PD.

        2. Cell B30: PSE input power. If the power is >12.95 W (more than the IEEE 802.3af limits), then this cell is shaded in light RED and your PSE must be capable of sourcing the power level shown in cell B30.

        3. Cell B33: If the calculated junction temperature is $\geq$140 °C, this cell is shaded in light red. Consider bypassing the on-chip diodes to lower the effective junction temperature, or consider reducing the output current (if possible). Other inputs in cells B9 through B13 may also need to be adjusted to lower the calculated junction temperature.

f. If you are using either of the "Isolated" worksheets, enter the input values to determine if your design will be operating in the "continuous" or "discontinuous mode":

    i. Check the value of the current calculated in cell H11.

        1. If your desired output current (B11) is *less than* the value shown in cell H11, use the "Isolated Discontinuous" worksheet.

        2. If your desired output current (B11) is *greater than* the value shown in cell H11, use the "Isolated Continuous" worksheet.

    ii. The feedback resistor network values (R5 and R6) for your design are calculated and displayed in cells E12 and E13. Use these resistor values to update your schematic.

    iii. Select transformer turns ratio: use 3.3, 2.5, or 1 as standard choices for 3.3, 5, and 12 V output, respectively. Leave the rest of the options as defaults. If you have different output voltage, contact Silicon Labs for recommendations.

    iv. To use the default transformer, snubber, and diode components used in the Si3402ISO-EVB isolated schematic, Silicon Labs strongly recommends leaving each default values "as-is" in cells B15 through B23. Always select the EP13 core if you require short-circuit protection.

    v. To ensure your design is operating within the acceptable operating ranges for all the external components used in your schematic, carefully review the calculated values found in cells B25 through B35.

      vi. Carefully review the calculated values in the Summary section (cells B37 through B41):

         1. Cell B37: PSE input voltage. Make sure the PSE input voltage is compatible with the PSE intended to power your PD.

         2. Cell B38: PSE input power. If the power is >12.95 W (more than the IEEE 802.3af limits), then this cell is shaded in light red, and your PSE must be capable of sourcing the power level shown in cell B30.

         3. Cell B41: If the calculated junction temperature is $\geq$140 °C, then this cell is shaded in light red. Consider bypassing the on-chip diodes to lower the effective junction temperature, or consider reducing the output current (if possible). Other inputs in cells B9 through B13 may also need to be adjusted to lower the calculated junction temperature.

3. **General design checklist items:**

   a. ESD caps (C10–C17 in Figure 1) are strongly recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.

   b. Never disable the soft start features. Make sure the soft start capacitor is in your schematics and connected correctly.

   c. If your design uses an AUX supply, be sure to include a 3 Ω surge limiting resistor in series with the AUX supply for hot insertion. Refer to AN296 when AUX supply is 48 V.

   d. Silicon Labs strongly recommends the inclusion of a minimum load (250 mW) to avoid switcher pulsing when no load is present and to avoid false disconnection when less than 10 mA is drawn from the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.

   e. If using PLOSS function, make sure it's properly terminated for connection in your PD subsystem. If PLOSS is not needed, float this pin.

4. **Layout guidelines:**

   a. Make sure VNEG pin of the Si3402 is connected to the backside of the QFN package with an adequate thermal plane, as noted in the data sheet and AN296.

   b. Keep the trace length from connecting to SWO and retuning to Vss1 and Vss2 as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere.

   c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.

   d. Keep the circular area of the loop from the Switcher FET output to the inductor or transformer and returning from the input filter capacitors (C1–C4) to Vss1 and Vss2 as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor or transformer to the Schottky diode and returning through the first stage output filter capacitor back to the inductor or transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.

   e. Connect the sense points to the output terminals directly to avoid load regulation issues related to IR drops in the PSB traces. For the non-isolated case, the sense points are Vposs, and the sense resistor is R6. For the non-isolated case, the sense points are R5, and the TLV431 is pin 3.

   f. Keep the feedback and loop stability components as far from the transformer/inductor and noisy power traces as possible.

   g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

   h. As a convenience in layout, please note that the IC is symmetrical with respect to CT1, CT2, SP1, and SP2. These leads can be interchanged.

To help ensure first-pass success, submit your schematics and layout files to PoEInfo@silabs.com for review. Other technical questions may be sent to this e-mail address as well.

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 0.5

- Updated layout to Revision 1.1.
- Updated BOM for Revision C Si3400.

Revision 0.5 to Revision 0.6

- Updated layout to Revision 1.2.
- Updated BOM for Revision D Si3400/01.
- Added Si3401.

Revision 0.6 to Revision 0.7

- Updated Figure 1, "Si3402 Schematic—5 V, Class 3 PD," on page 2 to include ISOSSFT (pin 4) for the isolated mode soft start feature (for revisions beginning with Rev. E), Vssa support and ESD improvements.
- Updated "4. Bill of Materials," on page 8 per schematic.

Revision 0.7 to Revision 0.8

- Updated "2. Si3402 Board Interface," on page 1.
- Updated "3. Schematics," on page 1.
- Updated Figure 1, "Si3402 Schematic—5 V, Class 3 PD," on page 2 to include ISOSSFT (pin 4) for the isolated mode soft start feature (for revisions beginning with Rev. E), Vssa support and ESD improvements.
- Updated Figure 2, "Top Silkscreen," on page 3.
- Updated Figure 3, "Top Layer," on page 4.
- Updated Figure 4, "Internal 1," on page 5.
- Updated Figure 5, "Internal 2," on page 6.
- Updated Figure 6, "Bottom Layer," on page 7.
- Updated "4. Bill of Materials," on page 8 per schematic.
- Added "5. BOM Options," on page 9.
- Added " Appendix—Si3402 Design and Layout Checklist," on page 10.

Revision 0.8 to Revision 0.81

- Changed C8 to C5 in the third column heading of the table on page 6.

Revision 0.81 to Revision 0.82

- Changed document title from Si3400/Si3401-EVB to Si3400/1/2-EVB.
- Updated Figure 1, "Si3402 Schematic—5 V, Class 3 PD," on page 2.
- Updated "4. Bill of Materials," on page 8.
- Updated silkscreen layers in Figures 2 through 6.

Revision 0.82 (Si3400/1/2-EVB) to Revision 1.0 (Si3402-EVB)

- Added Si3402-C4-EVB.
- Removed Si3400/1/2 as the Si3402 replaces these.
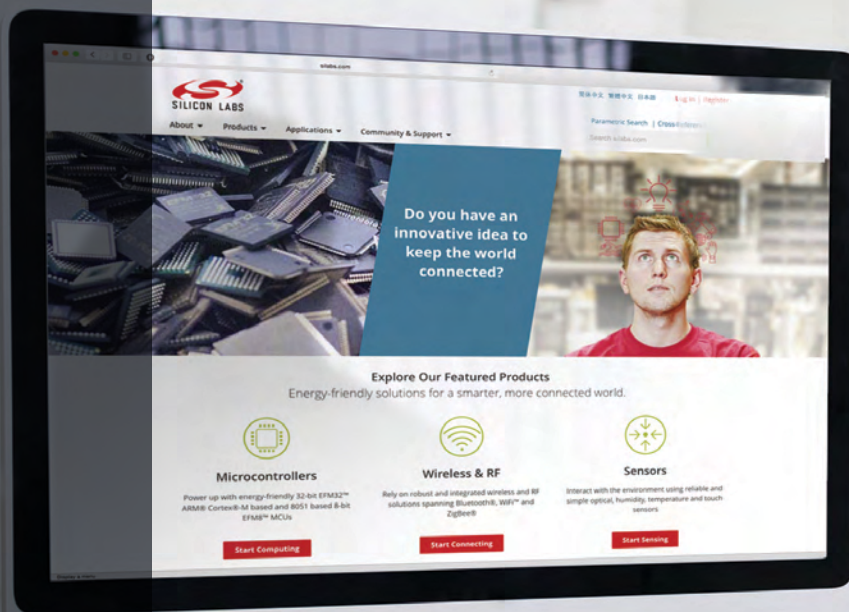
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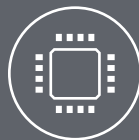
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