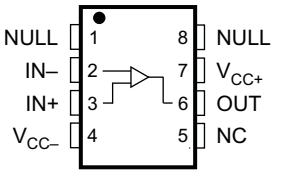
SLOS265C–SEPTEMBER 1999–REVISED JULY 2007

350-MHz LOW-NOISE HIGH-SPEED AMPLIFIERS

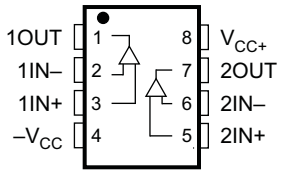
FEATURES

- **Ultralow 1.5-nV/√Hz Voltage Noise**
- **High Speed:**
  - **350-MHz Bandwidth (G = 10, –3 dB)**
  - **470-V/µs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **Stable at a Gain of 10 (–9) or Greater**
- **High Output Drive, I_O = 100 mA (typ)**
- **Excellent Video Performance:**
  - **17-MHz Bandwidth (0.1 dB, G = 10)**
  - **0.02% Differential Gain**
  - **0.08° Differential Phase**
- **Very Low Distortion:**
  - **THD = –68 dBc (f = 1 MHz, R_L = 150 Ω)**
- **Wide Range of Power Supplies:**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS4021
D and DGN Package
(Top View)



THS4022
D and DGN Package
(Top View)



NC - No internal connection

Cross Section View Showing
PowerPAD Option (DGN)

VOLTAGE AND CURRENT NOISE vs FREQUENCY

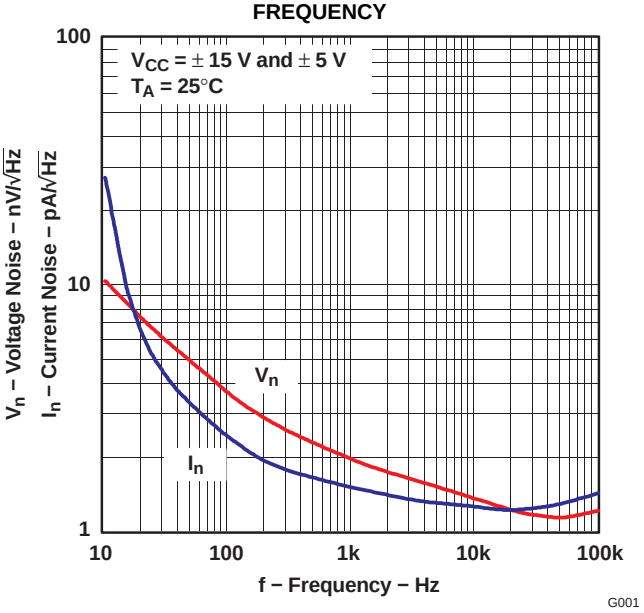


Figure 1.

DESCRIPTION

The THS4021 and THS4022 are ultralow voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communication and imaging. The single-amplifier THS4021 and the dual-amplifier THS4022 offer very good ac performance with 350-MHz bandwidth, 470-V/µs slew rate, and 40-ns settling time (0.1%). The THS4021 and THS4022 are stable at gains of 10 (–9) or greater. These amplifiers have a high drive capability of 100 mA and draw only 7.8-mA supply current per channel. With total harmonic distortion (THD) of –68 dBc at f = 1 MHz, the THS4021 and THS4022 are ideally suited for applications requiring low distortion.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/4012	290-MHz Low-Distortion High-Speed Amplifiers
THS4031/4032	100-MHz Low-Noise High-Speed Amplifiers
THS4061/4062	180-MHz High-Speed Amplifiers

CAUTION: The THS4021 and THS4022 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

AVAILABLE OPTIONS(1)

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE(2) (D)	PLASTIC MSOP(2) (DGN)		
0°C to 70°C	1	THS4021CD	THS4021CDGN	ACK	THS4021EVM
	2	THS4022CD	THS4022CDGN	ACA	THS4022EVM
–40°C to 85°C	1	THS4021ID	THS4021CIDGN	ACL	–
	2	THS4022ID	THS4022CIDGN	ACB	–

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI Web site at www.ti.com.
(2) The D and DGN packages are available taped and reeled. Add an R suffix to the device type (for example, THS4021CDGN).

FUNCTIONAL BLOCK DIAGRAMS

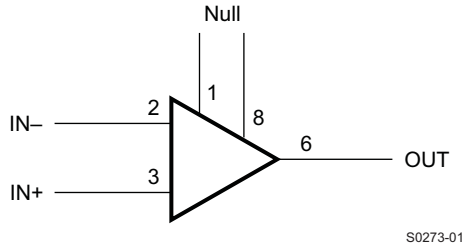


Figure 2. THS4021—Single Channel

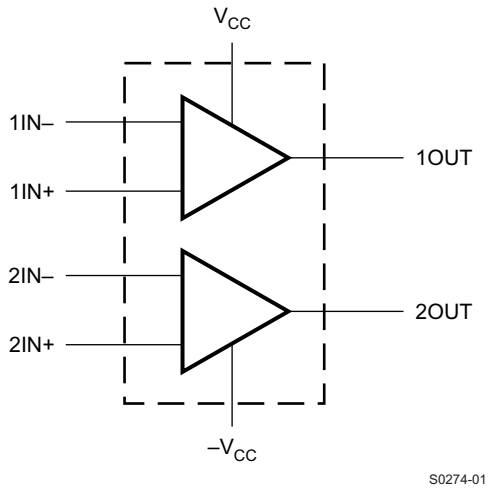


Figure 3. THS4022—Dual Channel

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage	±16.5	V
V_I	Input voltage	$\pm V_{CC}$	V
I_O	Output current	150	mA
V_{IO}	Differential input voltage	±4	V
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Maximum junction temperature	150	°C
T_A	Operating free-air temperature: C-suffix	0 to 70	°C
	I-suffix	–40 to 85	
T_{stg}	Storage temperature	–65 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D(1)	167	38.3	740 mW
DGN(2)	58.4	4.7	2.14 W

(1) This data was taken using the JEDEC standard low-K test PCB. For the JEDEC proposed high-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
(2) This data was taken using 2-oz. (0.071-mm thick) trace and copper pad on a 3-in. × 3-in. (7.62-cm × 7.62-cm) PCB, with the device soldered directly to the board. For further information, see the *Application Information* section of this data sheet.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC+} and V_{CC-}	Supply voltage	Dual supply	±4.5		±16	V
		Single supply	9		32	
T_A	Operating free-air temperature	C-suffix	0		70	°C
		I-suffix	–40		85	

ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dynamic Performance							
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	Gain = 10		350		MHz
		V_{CC} = ±5 V			280		
		V_{CC} = ±15 V	Gain = 20		80		
		V_{CC} = ±5 V			70		
	Bandwidth for 0 1-dB flatness	V_{CC} = ±15 V	Gain = 10		17		
		V_{CC} = ±5 V			17		
	Full power bandwidth(1)	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V			3.7		
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			11.8		
SR	Slew rate(2)	V_{CC} = ±15 V, 10-V step	Gain = 10		470		V/µs
		V_{CC} = ±5 V, 5-V step			370		

(1) Full-power bandwidth = slew rate / 2π $V_{O(Peak)}$.
(2) Slew rate is measured from an output level range of 25% to 75%.

ELECTRICAL CHARACTERISTICS (continued)

at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = –10		40		ns
		V_{CC} = ±5 V, 2-V step			50		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = –10		145		
		V_{CC} = ±5 V, 2-V step			150		
Noise/Distortion Performance							
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, gain = 2, V_{CC} = ±15 V	R_L = 150 Ω		–68		dBc
			R_L = 1 kΩ		–77		
		$V_{O(pp)}$ = 2 V, f = 1 MHz, gain = 2, V_{CC} = ±5 V	R_L = 150 Ω		–69		
			R_L = 1 kΩ		–78		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			1.5		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f > 10 kHz			2		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE modulation, ±100 IRE ramp	V_{CC} = ±15		0.02%		
			V_{CC} = ±5 V		0.02%		
	Differential phase error	Gain = 2, NTSC, 40 IRE modulation, ±100 IRE ramp	V_{CC} = ±15		0.08		°
			V_{CC} = ±5 V		0.06		
X_T	Channel-to-channel crosstalk (THS4022 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHz			–60		dB
DC Performance							
	Open-loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	40	60		V/mV
			T_A = full range	35			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	20	35		
			T_A = full range	15			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		0.5	2	mV
			T_A = full range			3	
	Offset voltage drift		T_A = full range		15		µV/°C
I_{IB}	Input bias current		T_A = 25°C		3	6	µA
			T_A = full range			6	
I_{OS}	Input offset current		T_A = 25°C		30	250	nA
			T_A = full range			400	
	Offset current drift	T_A = full range			0.3		nA/°C
Input Characteristics							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.8	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V, T_A = full range		74	95		dB
r_i	Input resistance				1		MΩ
C_i	Input capacitance				1.5		pF
Output Characteristics							
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.5		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.3		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		
		V_{CC} = ±5 V		±3.4	±3.8		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	80	100		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current(3)	V_{CC} = ±15 V			150		mA
R_O	Output resistance(3)	Open loop			13		Ω

(3) Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the *Absolute Maximum Ratings* table of this data sheet for more information.

ELECTRICAL CHARACTERISTICS (continued)

at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		7.8	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.7	9	
			T_A = full range			10.5	
PSRR	Power-supply rejection ratio	V_{CC} = ±5 V or ±15 V, T_A = full range		80	95		dB

TYPICAL CHARACTERISTICS

CROSSTALK VS FREQUENCY

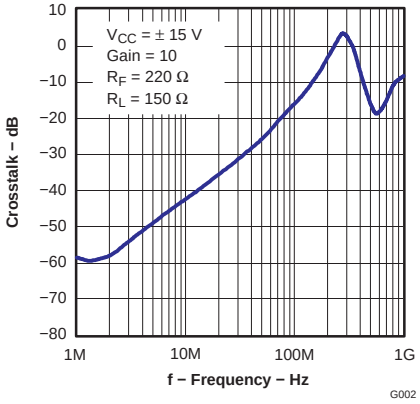


Figure 4.

OPEN LOOP GAIN AND PHASE RESPONSE VS FREQUENCY

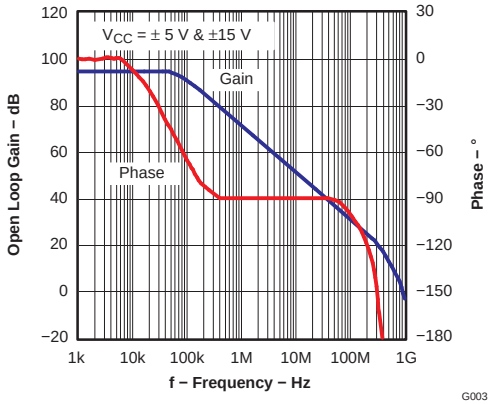


Figure 5.

TOTAL HARMONIC DISTORTION VS FREQUENCY

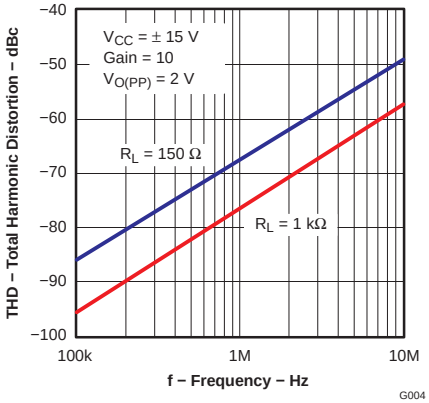


Figure 6.

DISTORTION VS OUTPUT VOLTAGE

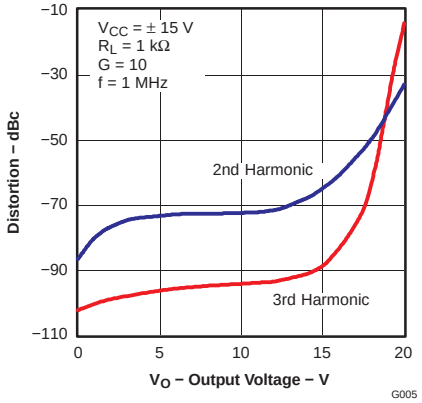


Figure 7.

DISTORTION VS OUTPUT VOLTAGE

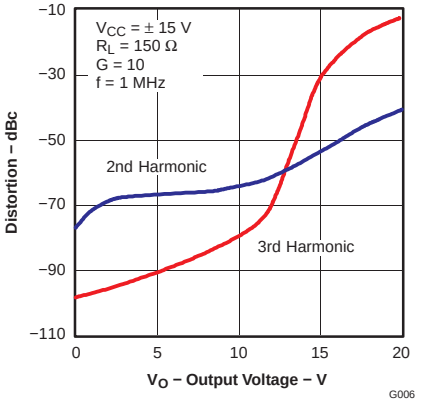


Figure 8.

TYPICAL CHARACTERISTICS (continued)

DISTORTION vs FREQUENCY

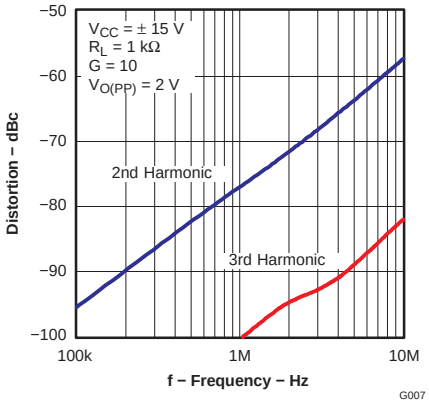


Figure 9.

DISTORTION vs FREQUENCY

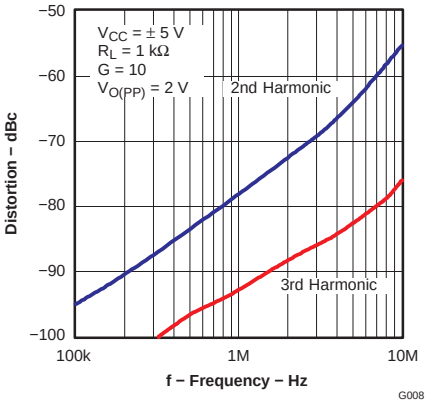


Figure 10.

DISTORTION vs FREQUENCY

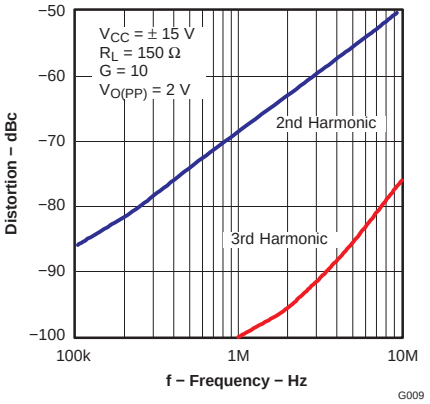


Figure 11.

DISTORTION vs FREQUENCY

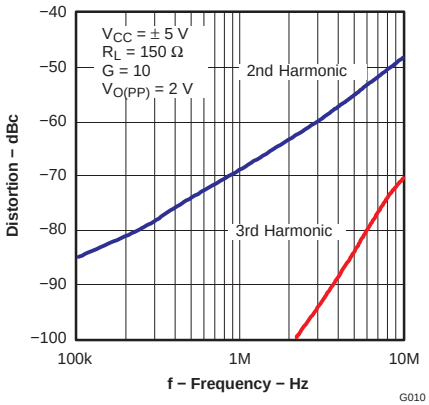


Figure 12.

OUTPUT AMPLITUDE vs FREQUENCY

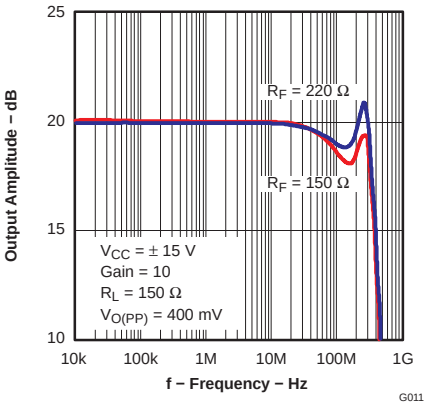


Figure 13.

OUTPUT AMPLITUDE vs FREQUENCY

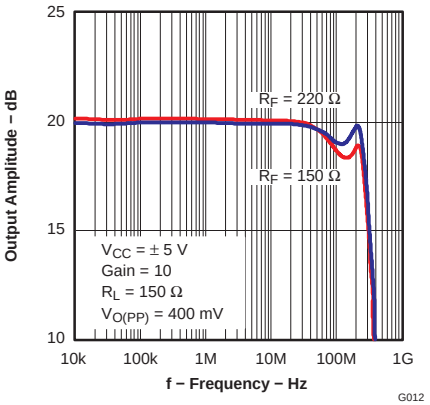


Figure 14.

OUTPUT AMPLITUDE vs FREQUENCY

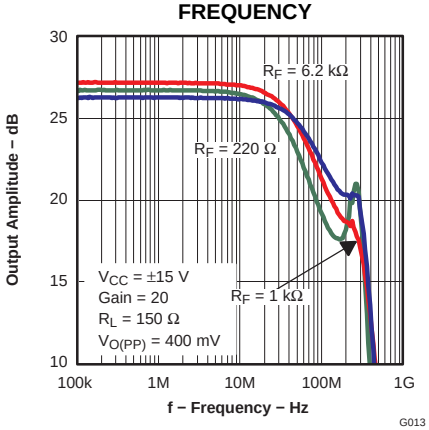


Figure 15.

OUTPUT AMPLITUDE vs FREQUENCY

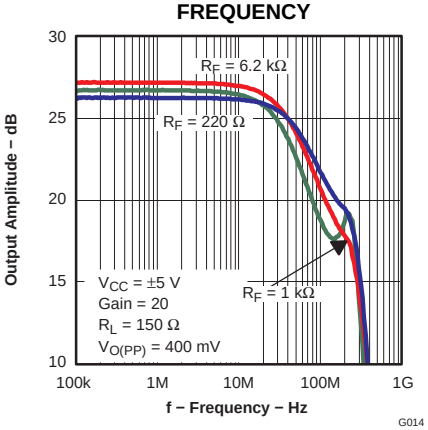


Figure 16.

1-V STEP RESPONSE

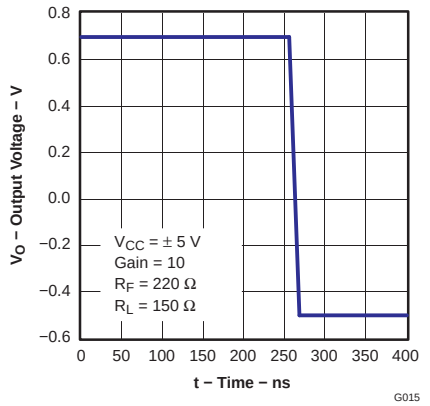


Figure 17.

TYPICAL CHARACTERISTICS (continued)

5-V STEP RESPONSE

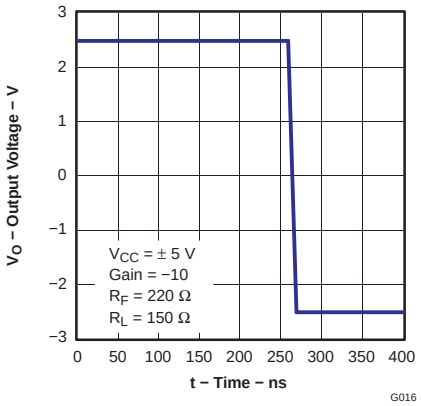


Figure 18.

1-V STEP RESPONSE

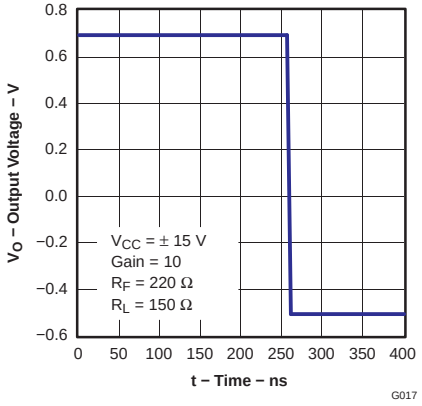


Figure 19.

10-V STEP RESPONSE

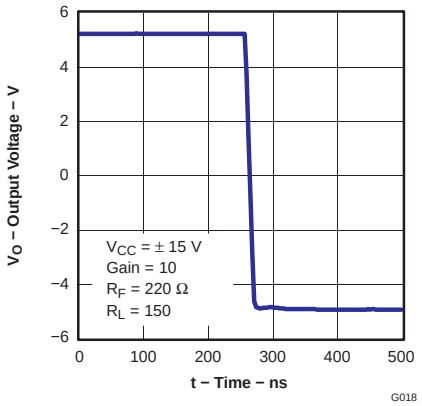


Figure 20.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

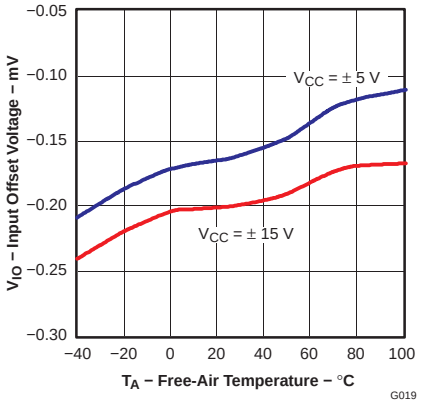


Figure 21.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

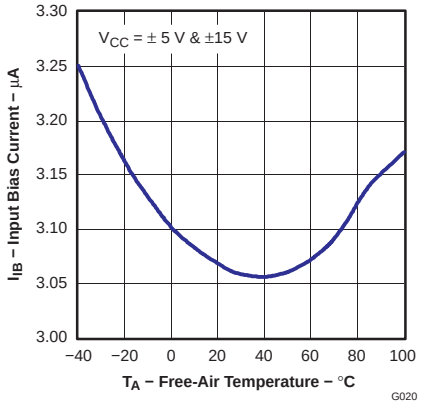


Figure 22.

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

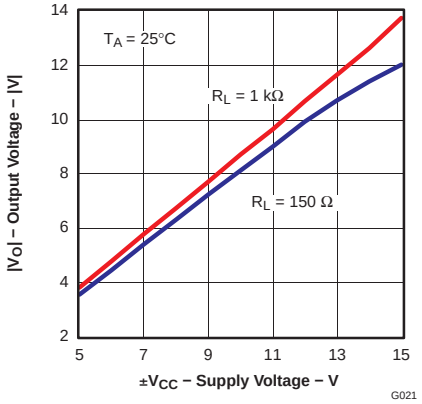


Figure 23.

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

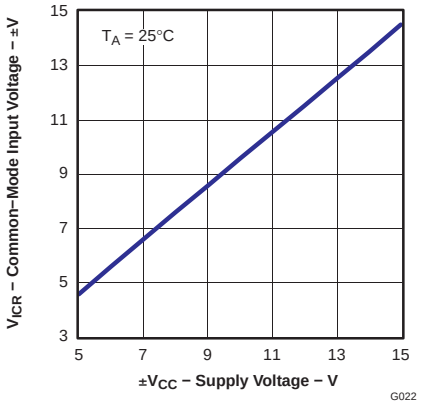


Figure 24.

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

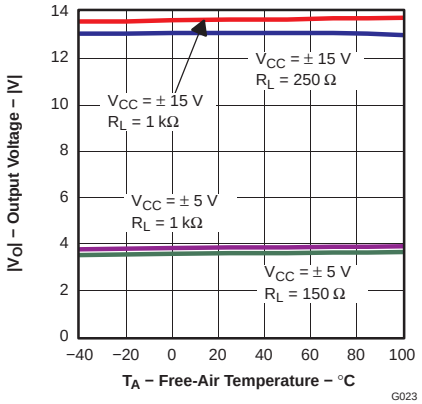


Figure 25.

SUPPLY CURRENT vs SUPPLY VOLTAGE

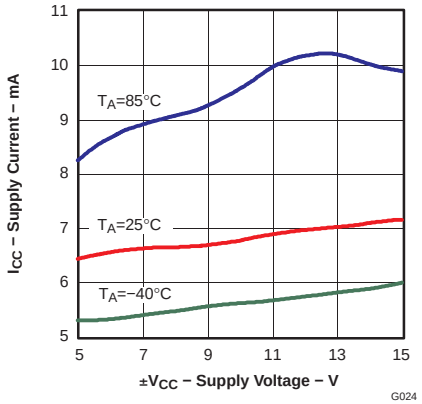


Figure 26.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE AND CURRENT NOISE VS FREQUENCY

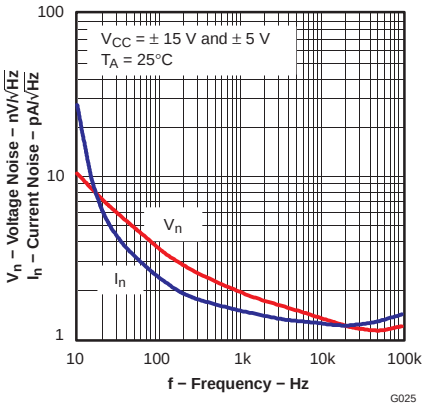


Figure 27.

POWER SUPPLY REJECTION RATIO VS FREQUENCY

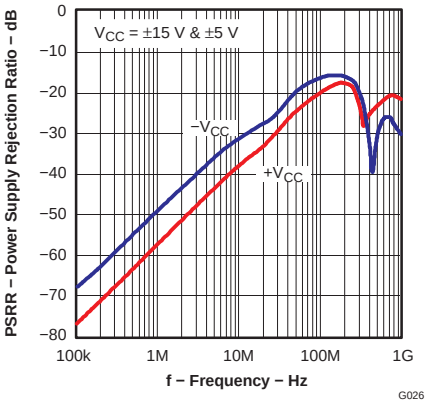


Figure 28.

COMMON MODE REJECTION RATIO VS FREQUENCY

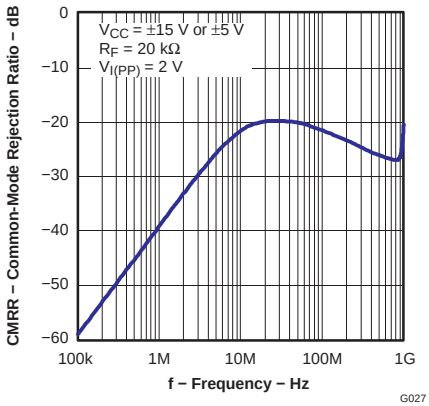


Figure 29.

APPLICATION INFORMATION

Theory of Operation

The THS402x is a high-speed operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_T of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 30.

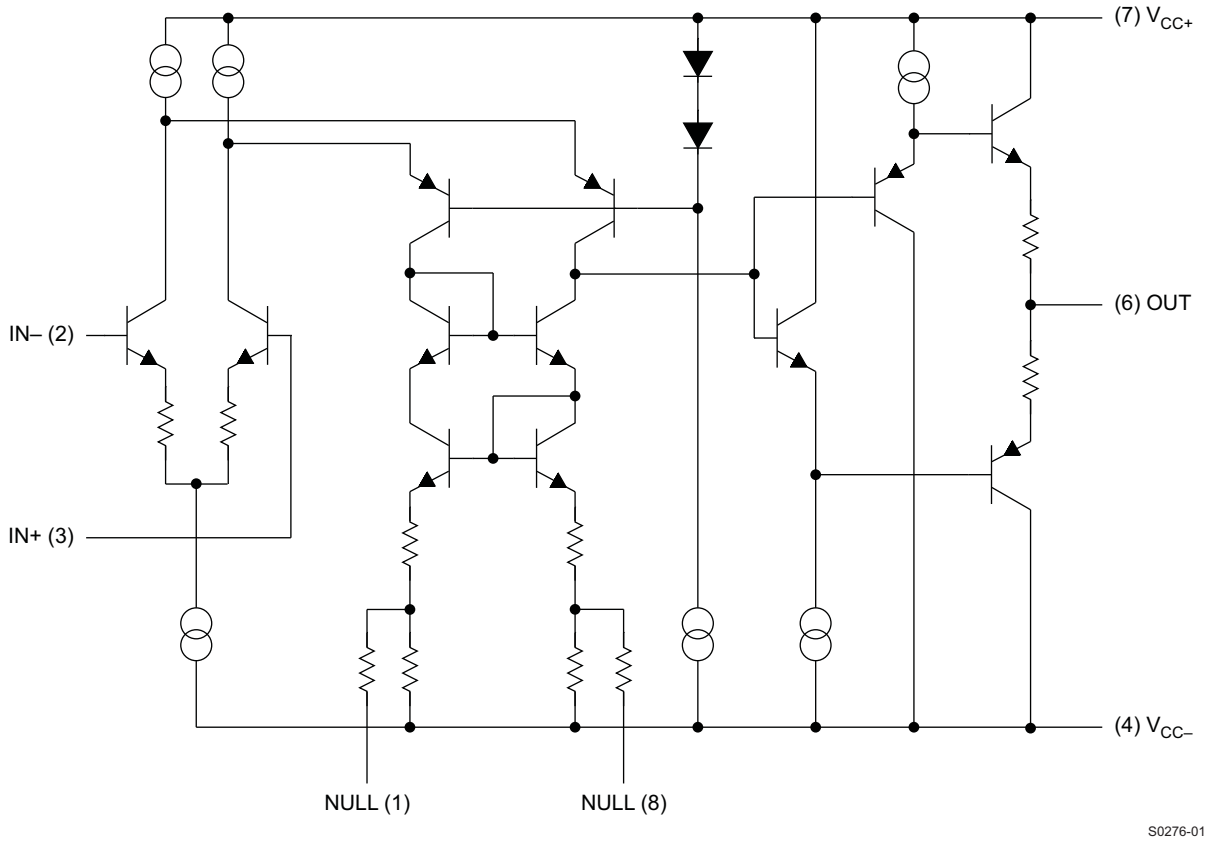


Figure 30. THS4021 Simplified Schematic

Noise Calculations and Noise Figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS402x is shown in Figure 31. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

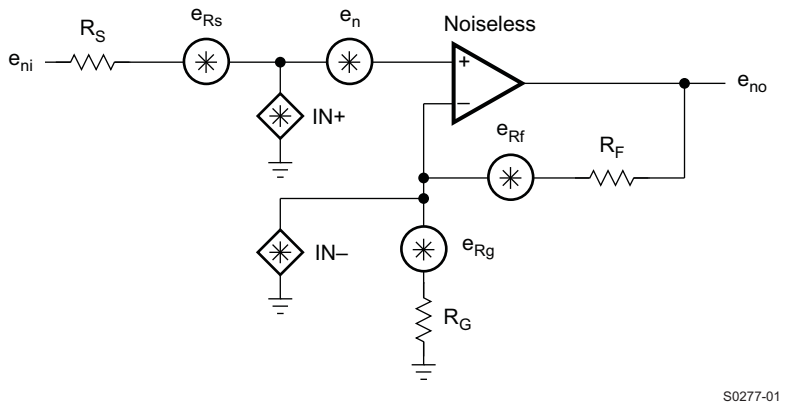


Figure 31. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

where:

k = Boltzmann's constant = 1.380658×10^{-23}

T = Temperature in degrees Kelvin (273 + °C)

$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, see the *Noise Analysis in Operational Amplifier Circuits* application report (SLVA043).

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left(\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2\right)}{4\,kTR_S}\right]$$

Figure 32 shows the noise figure graph for the THS402x.

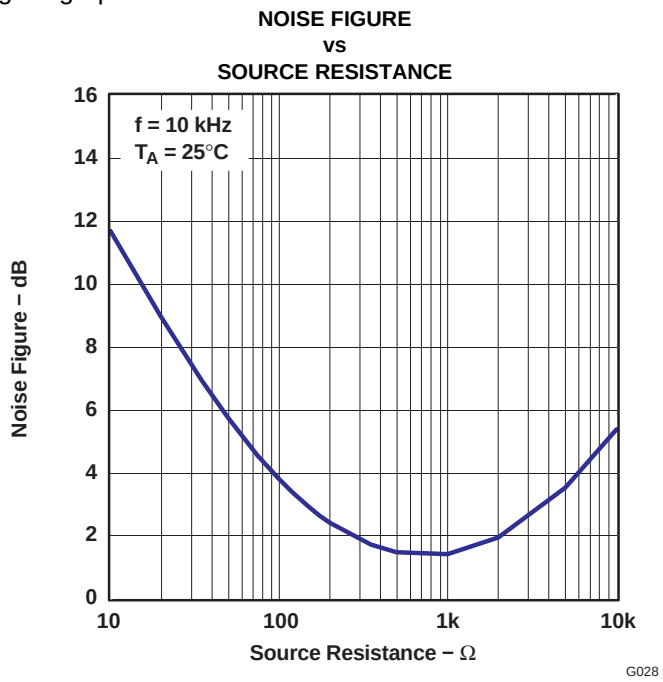


Figure 32. Noise Figure vs Source Resistance

Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS402x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 33. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

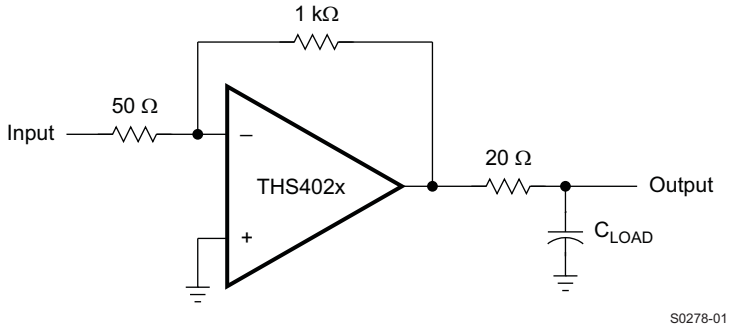


Figure 33. Driving a Capacitive Load

Offset Nulling

The THS402x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4021. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 34.

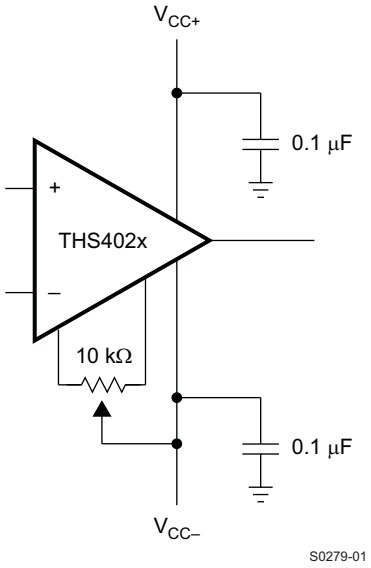
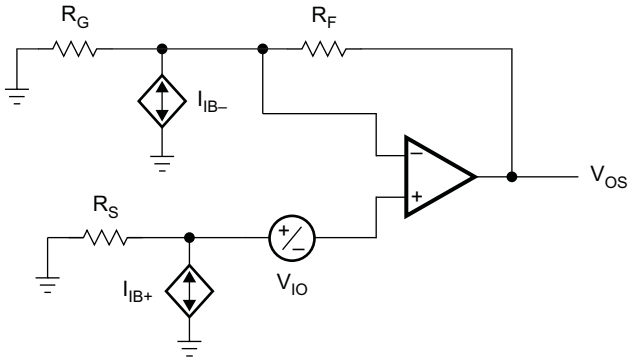


Figure 34. Offset Nulling Schematic

Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula of Figure 35 can be used to calculate the output offset voltage.



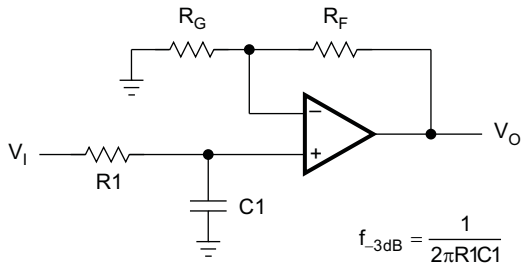
$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} \times R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} \times R_F$$

S0280-01

Figure 35. Output Offset Voltage Model

General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 36).



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

S0281-01

Figure 36. Single-Pole Low-Pass Filter

Circuit Layout Considerations

To achieve the levels of high-frequency performance of the THS402x, follow proper printed-circuit board high-frequency design techniques. A general set of guidelines is given as follows. In addition, a THS402x evaluation board is available to use as a guide for layout or for evaluating the device performance.

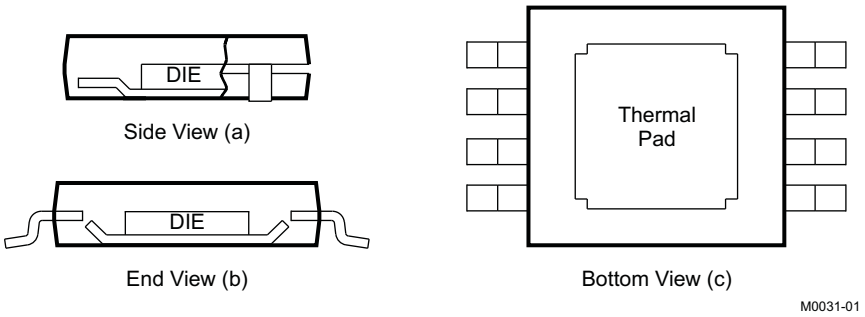
- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low-inducance ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch (2.54 mm) between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often produces stability problems. Surface-mount packages soldered directly to the PCB is the best implementation.
- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

General Thermal Pad Design Considerations

The THS402x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 37(a) and Figure 37(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 37(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a design breakthrough, combining the small area and ease of the surface mount assembly method to eliminate the previously difficult mechanical methods of heatsinking.



NOTE: The thermal pad is electrically isolated from all terminals in the package.

Figure 37. Views of Thermally Enhanced DGN Package

Although there are many ways to heatsink this device properly, the following steps illustrate the recommended approach.

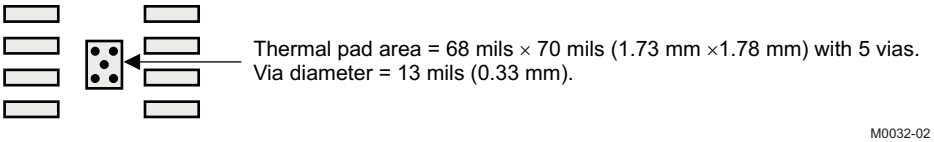


Figure 38. Thermal Pad PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 38. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils (0.33 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the THS402xDGN IC. These additional vias may be larger than the 13-mil (0.33-mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS402xDGN package should connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

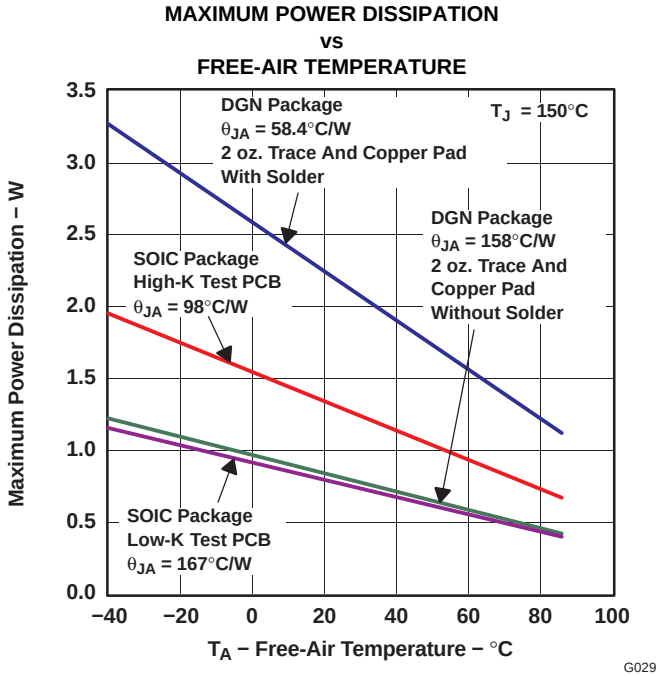
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS402xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS402xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches (7.62 cm × 7.62 cm), then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS402x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

where:

P_D = Maximum power dissipation of THS402x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE: Results are with no air flow and PCB size = 3 in. × 3 in. (7.62 cm × 7.62 cm).

Figure 39. Maximum Power Dissipation vs Free-Air Temperature

More-complete details of the thermal pad installation process and thermal management techniques can be found in the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially with multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 40 through Figure 43 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line exceeds the amplifier limits and failure may result. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to use fully the heat dissipation properties of the thermal pad. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual-amplifier package (THS4022), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier outputs are identical.

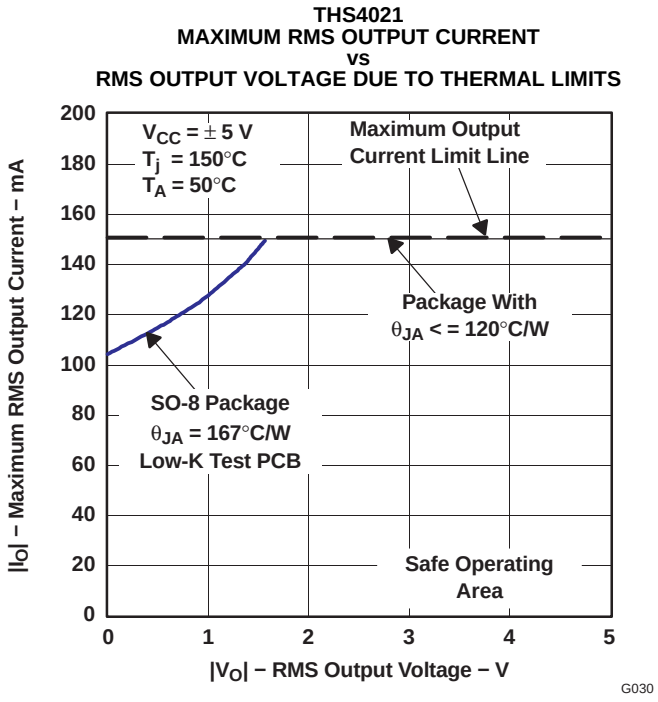


Figure 40.

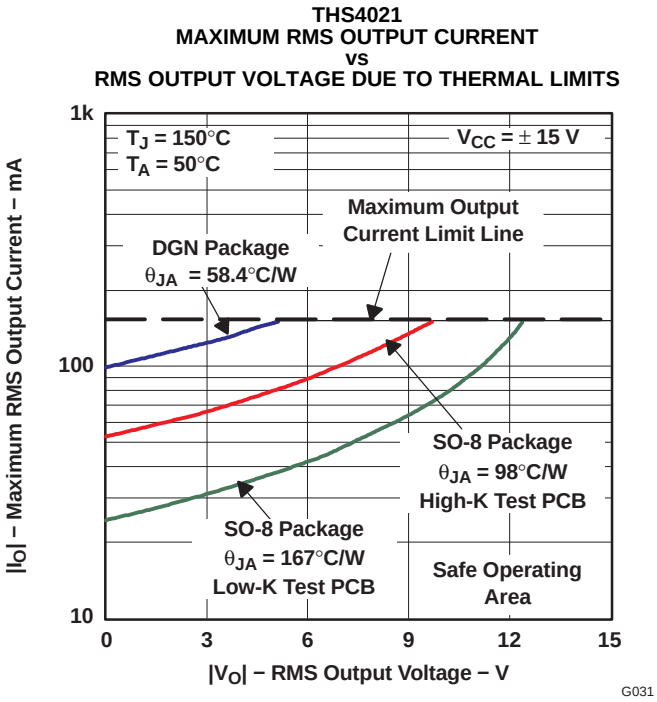


Figure 41.

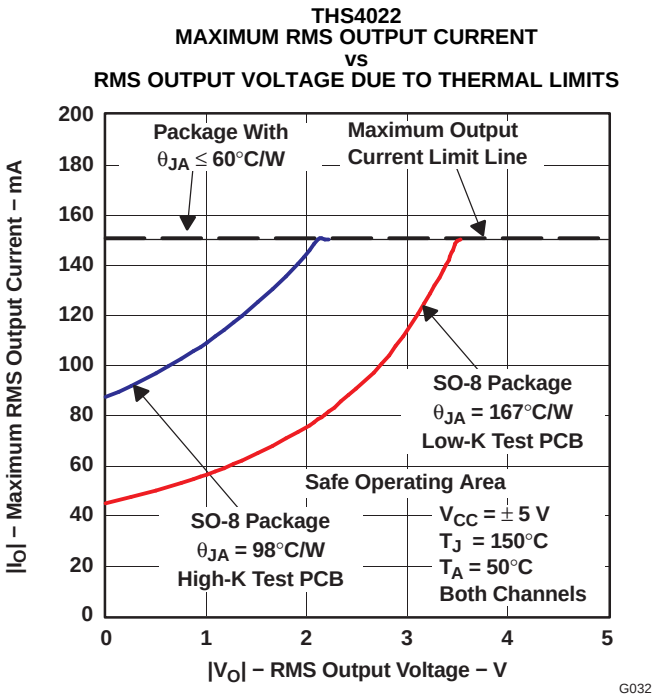


Figure 42.

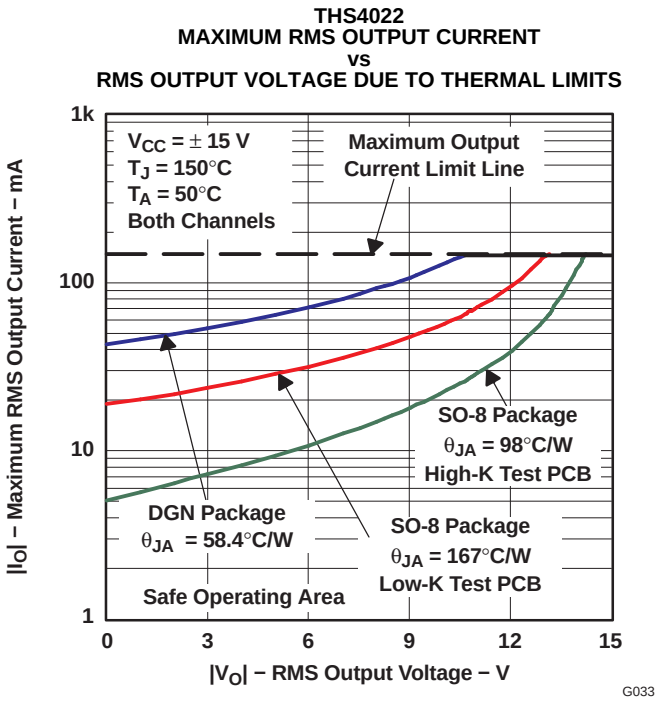


Figure 43.

Evaluation Board

Evaluation boards are available for the THS4021 (literature number SLOP129) and THS4022 (literature number SLOP231). These boards have been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the THS4021 evaluation board is shown in Figure 44. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, see the *THS4021 High-Speed Operational Amplifier Evaluation Module* user's guide (SLOU063) or the *THS4022 Dual High-Speed Operational Amplifier Evaluation Module* user's guide (SLOU064). To order the evaluation board, contact your local TI sales office or distributor or visit the Texas Instruments Web site at www.ti.com.

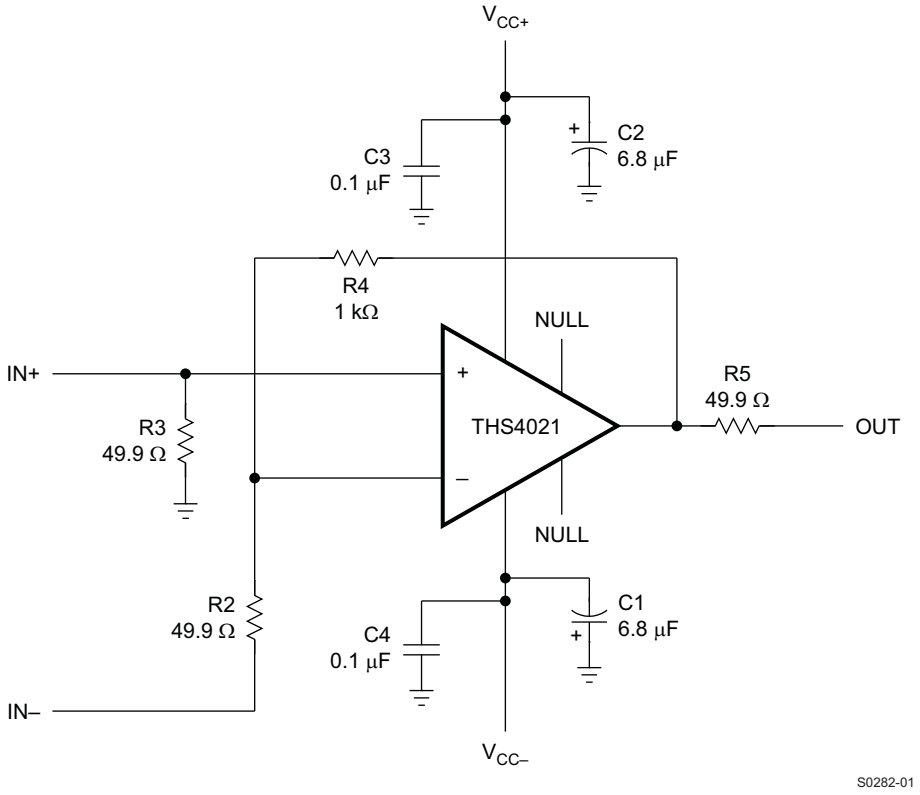


Figure 44. THS4021 Evaluation Board

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4021CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4021C	Samples
THS4021CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK	Samples
THS4021CDGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK	Samples
THS4021CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACK	Samples
THS4021ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4021I	Samples
THS4021IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL	Samples
THS4021IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACL	Samples
THS4021IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4021I	Samples
THS4022CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4022C	Samples
THS4022CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACA	Samples
THS4022CDGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACA	Samples
THS4022CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACA	Samples
THS4022ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4022I	Samples
THS4022IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACB	Samples
THS4022IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

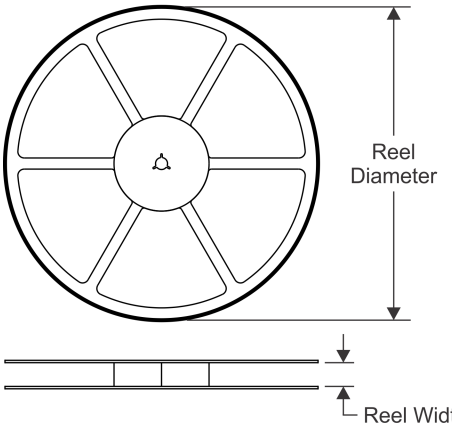
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

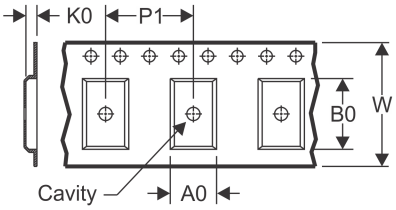
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

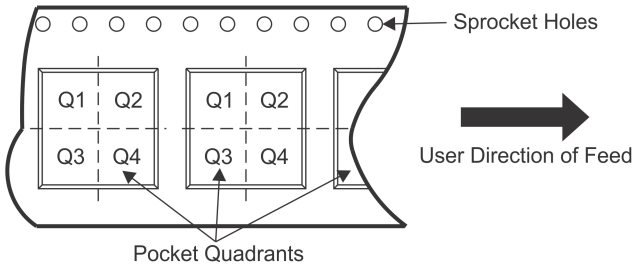


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

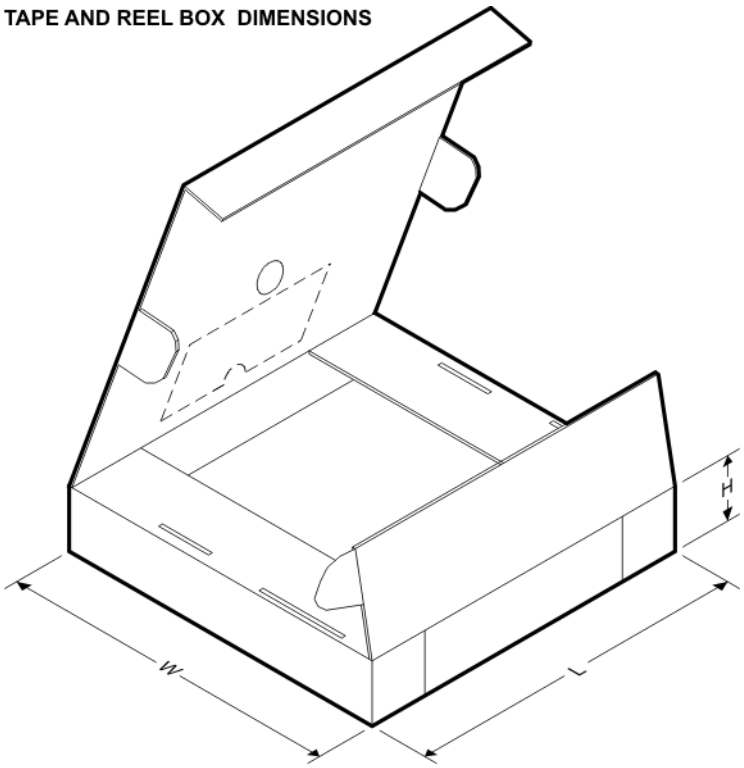
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4021CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4021IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4021IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4022CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

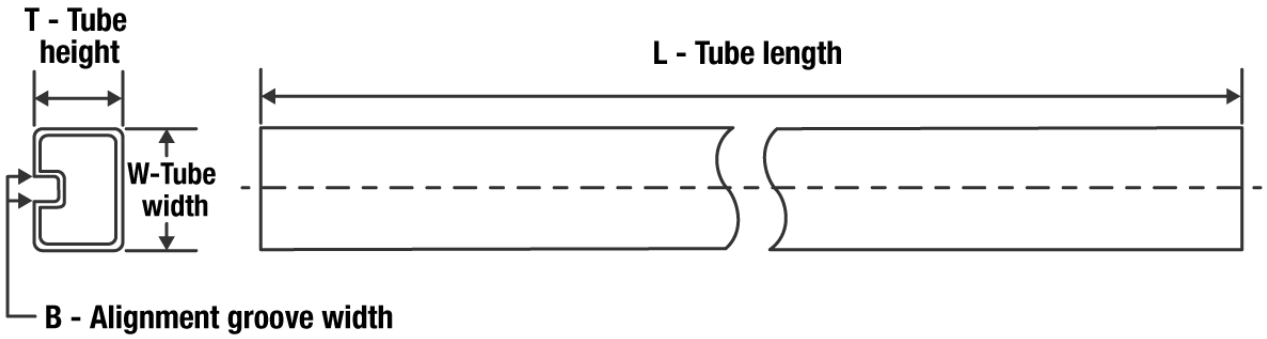
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4021CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4021IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4021IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4022CDGNR	HVSSOP	DGN	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4021CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4021ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4022CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4022CDGN	DGN	HVSSOP	8	80	331.47	6.55	3000	2.88
THS4022CDGNG4	DGN	HVSSOP	8	80	331.47	6.55	3000	2.88
THS4022ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4022IDGN	DGN	HVSSOP	8	80	331.47	6.55	3000	2.88

GENERIC PACKAGE VIEW

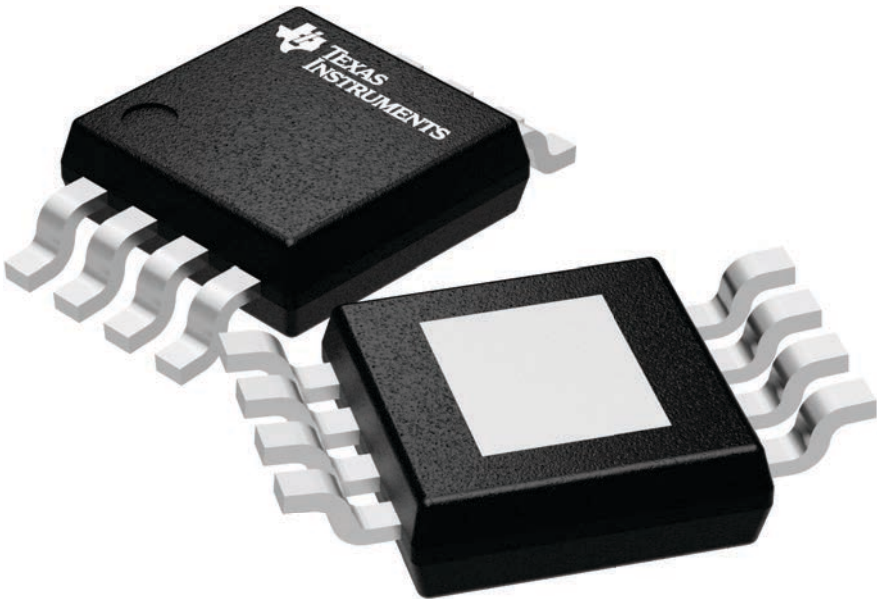
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

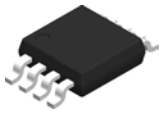
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

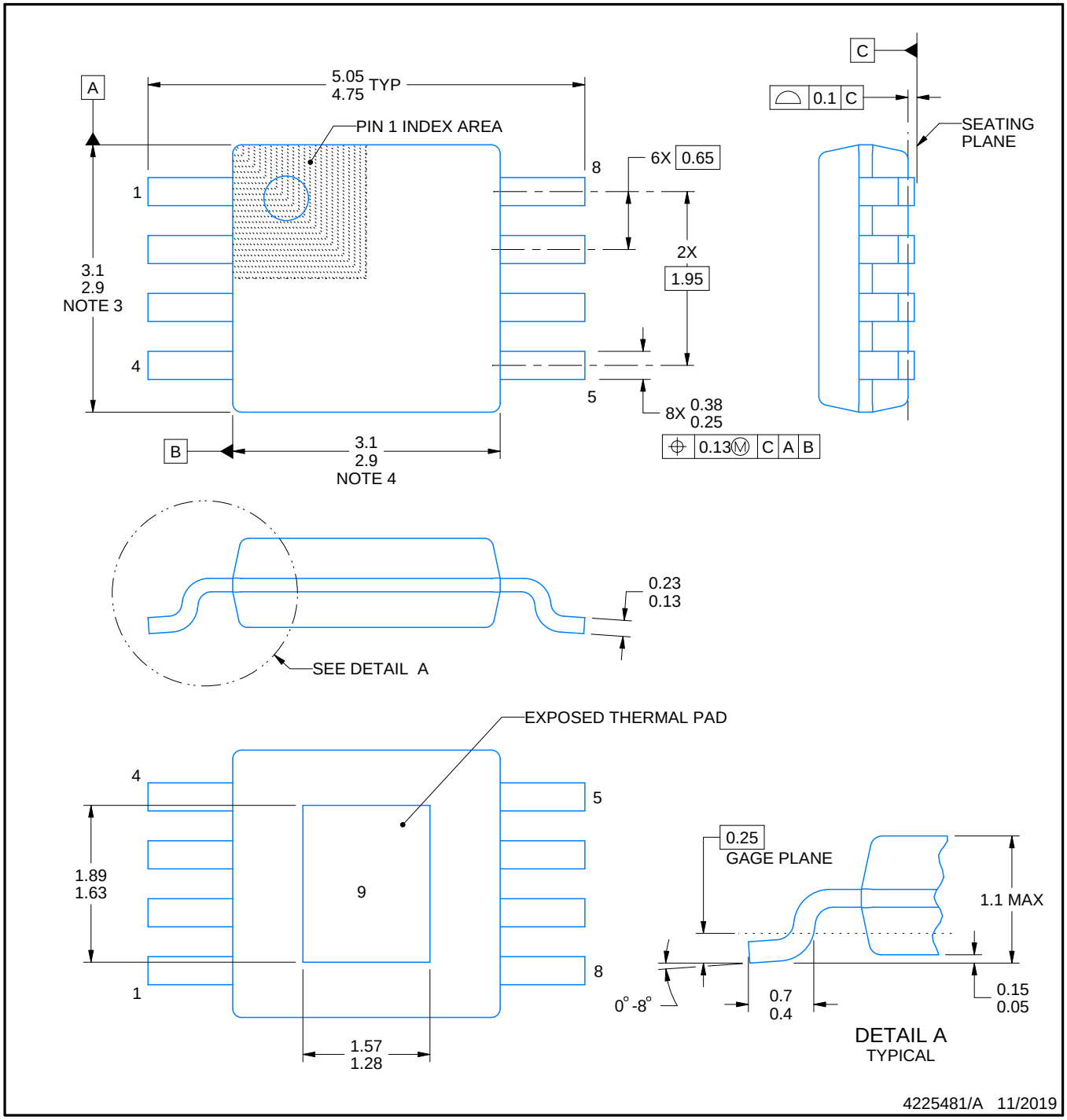
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

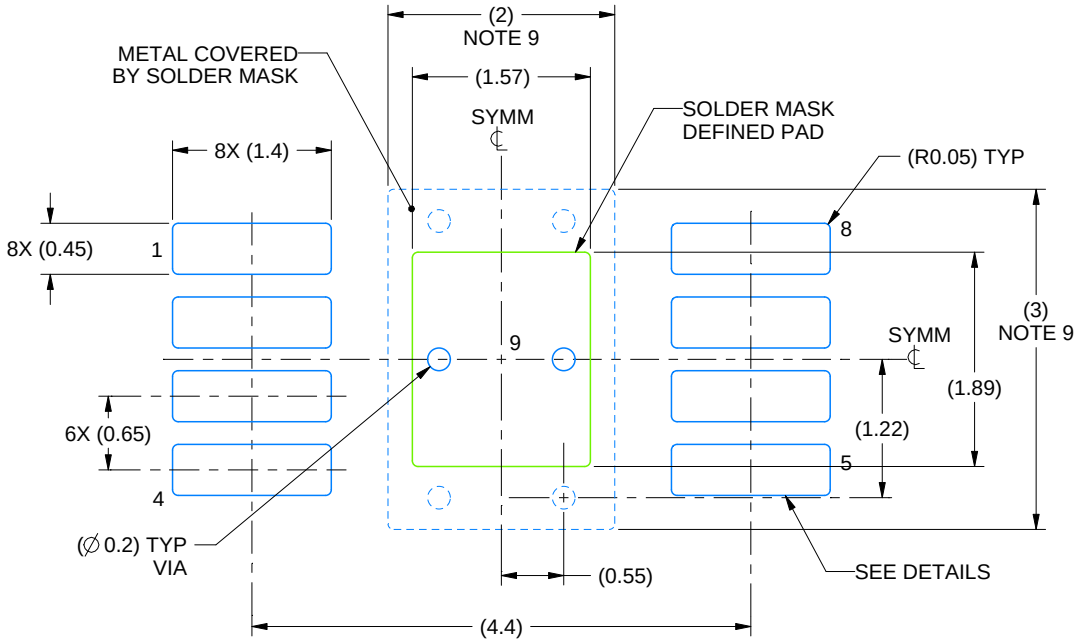
SMALL OUTLINE PACKAGE



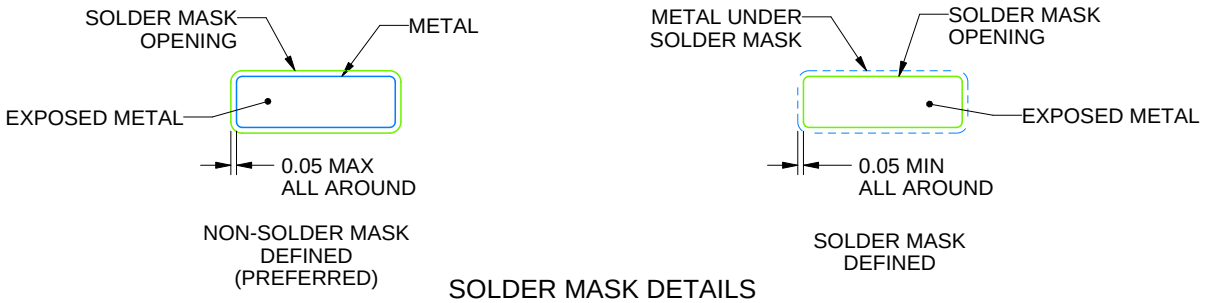
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

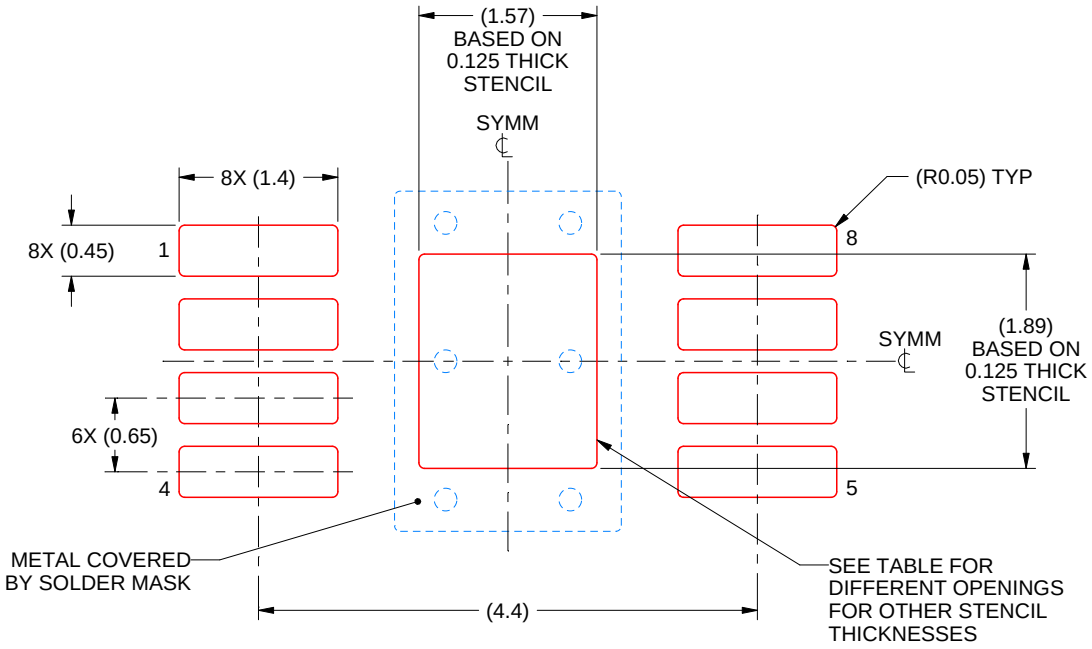


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



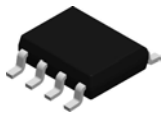
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

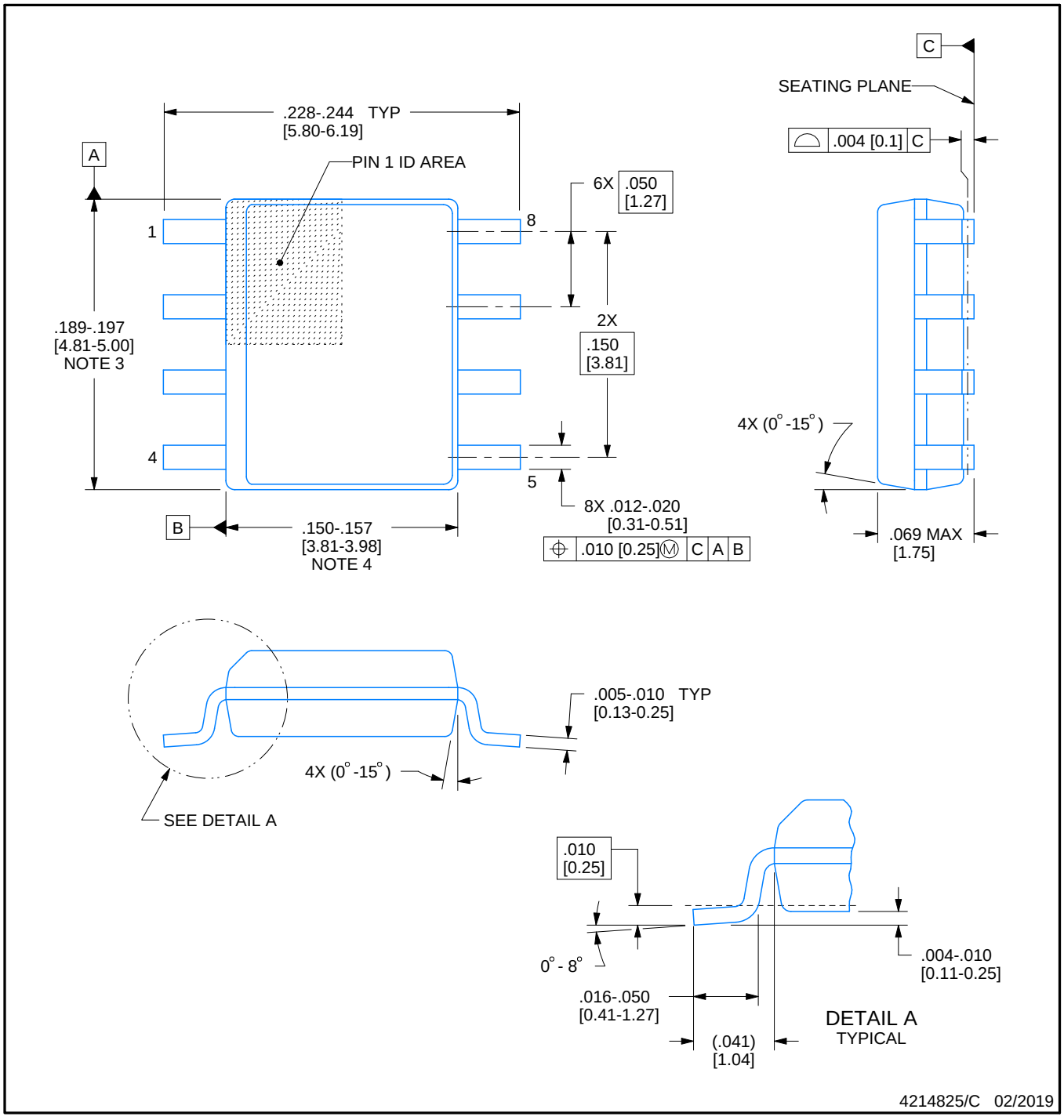


PACKAGE OUTLINE

D0008A

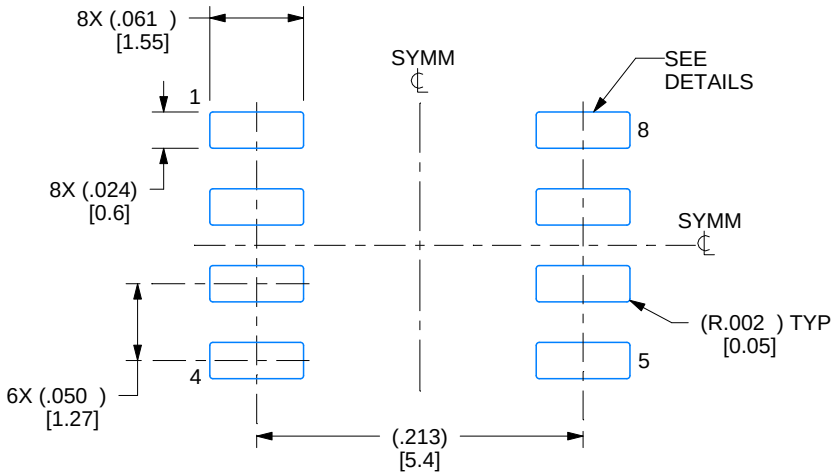
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

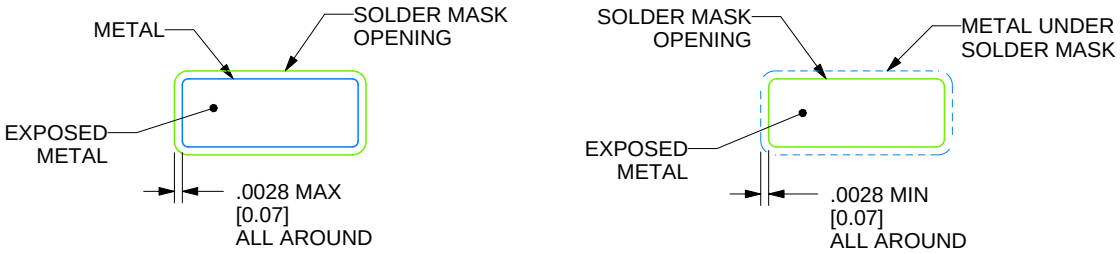


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

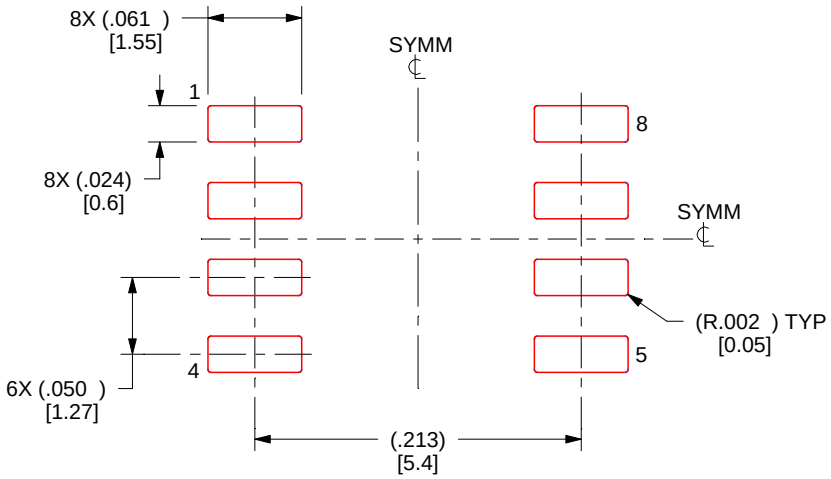
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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