PIC18CXX2

PIC18CXX2 Rev. B Silicon/Data Sheet Errata

The PIC18CXX2 (Rev. B) parts you have received conform functionally to the Device Data Sheet (DS39026**C**), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC18CXX2 silicon.

1. Module: CPU

Using the LFSR instruction to load a value into the specified FSR register, may also corrupt a RAM location.

Work around

Do not use the LFSR instruction. The use of MOVLW and MOVWF instructions can be implemented to load the FSR registers. The WREG register may need to be saved before these operations and restored afterwards.

EXAMPLE 1: DEFINED OPERATION

```
    LFSR      FSR1, Pointer
```

EXAMPLE 2: WORK AROUND

```
;
; Optionally save the WREG register
;
    MOVLW     HIGH (Pointer)
    MOVWF     FSR1H
    MOVLW     LOW (Pointer)
    MOVWF     FSR1L
;
; Optionally restore the WREG register
;
```

2. Module: CCP

When the CCP module is configured to Compare mode toggle output pin (CCPxCON = b'00xx0010'), unexpected pin operation may be observed.

When the timer used for the CCP module time-base is configured to have a prescale ratio greater than 1:1, the output on the CCP pin will toggle the prescaled number of times for each compare match. That is, for a n:1 timer prescale ratio, the CCP output pin will toggle n times at each compare match. The toggle occurs each instruction cycle (T_{CY}).

Work around

The prescale ratio for the timer used as the CCP module time-base must be 1:1. If a longer compare time is needed, the timer must be running in Timer mode or Synchronized Counter mode (external clock source).

Date Codes that pertain to this issue:

ALL

Note: When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur, will be specified.

3. Module: Oscillator

In-Circuit Serial Programming™ (ICSP™) may become unpredictable when a free-running clock source is present on OSC1.

When entering ICSP mode, the PIC18C452 switches from OSC1 to RB6 for its external clock source. Refer to the PIC18CXXX Programming Specification (DS39028) for additional information. If OSC1 is high at the time, a high-to-low transition occurs upon the transition to RB6.The ICSP logic interprets this as a clock, and advances the internal clock logic to Q2. This causes an unrecoverable mismatch between ICSP logic and the clock.

Work around

Before entering ICSP mode, OSC1 must be driven to and held in a low state. This must occur before changing states on $\overline{MCLR}/V_{PP}$, RB6 and RB7.

Note: As with any windowed EPROM device, please cover the window at all times, except when erasing.

4. Module: CCP (Compare Mode)

The Compare mode may not operate as expected when configuring the compare match to drive the I/O pin low (CCPxM<3:0> = 1001).

When the CCP module is changed to compare output low (CCPxM<3:0> = 1001) from any other non-compare CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will remain low when the compare match occurs (see Table 1).

However, when the CCP module is changed to compare output high (CCPxM<3:0> = 1000) from any other CCP mode, the I/O pin will immediately be driven low, regardless of the state of the I/O data latch. The pin will be driven high when the compare match occurs.

TABLE 1: COMPARE OUTPUT LOW SWITCHING

CCP Mode CCPxM<3:0> =	I/O Pin State	Change CCP to CCPxM<3:0> =	
		1001	1000
0xxx	H	L	L
	L	L	L
1000	H	H	—
	L	L	—
1001	H	—	L
	L	—	L
101x	H	L	L
	L	L	L
11xx	H	L	L
	L	L	L

Work around

To have the I/O pin high until the compare match low occurs, force a compare match high to get the I/O pin into the high state, then reconfigure the compare match to force the I/O low when the compare condition occurs.

5. Module: Timer1 and Timer3

When the prescaler select bits (bits 5:4 of the T1CON or T3CON registers) are modified, the timer may inadvertently increment. This can occur even if the timer is in the OFF state. Changing the prescaler may cause clock glitches, which may cause the counter to increment improperly.

Work around

Always re-initialize the timer registers (either TMR1H and TMR1L, or TMR3H and TMR3L) after changing the prescaler bits of registers T1CON or T3CON.

As an alternative, store the timer value before changing the prescaler bits of the timer control registers, and restore the timer value after changing the bits.

6. Module: I/O (Parallel Slave Port)

The Input Buffer Status bit of the TRISE register (TRISE<7>) may be inadvertently cleared, even when the PORTE input buffer has not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = '1111'), and
- Any instruction that contains 83h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5 and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contains 83h in the 8 Least Significant bits while the BSR points to Bank 15 (BSR = 0Fh).

7. Module: MSSP (I^2C Master Mode)

The BF Status bit (SSPSTAT<0>) may be inadvertently cleared, even if the buffer has not been read. This will occur when both of the following two conditions are met:

- The four Least Significant bits of the BSR are equal to 0Fh (BSR<3:0> = '1111'), and
- Any instruction that contains C9h in its 8 Least Significant bits (i.e., register file address, literal data, instruction address offset, etc.) is executed.

Work around

All work arounds involve setting the BSR to some value other than 0Fh. Other solutions may exist in addition to the work arounds proposed below.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5 and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instruction contains C9h in the 8 Least Significant bits while BSR points to Bank 15 (BSR = 0Fh).

8. Module: Interrupts

High priority interrupts may become improperly enabled, while low priority interrupts become improperly disabled at the same time. This may occur when low priority interrupts are in an enabled state and the following conditions occur simultaneously:

- High priority interrupts are being changed from an enabled to a disabled state
- One or more low priority interrupts occur

Work around

Always disable low priority interrupts before disabling high priority interrupts. Re-enable the low priority interrupts afterward, if necessary.

9. Module: Watchdog Timer

After the WDT is allowed to time-out, all subsequent WDT periods following the very first, may double in duration. This can occur if the CLRWDT instruction is not executed prior to the timer timing out.

Work around

Always execute the CLRWDT instruction prior to entering a potential WDT time-out condition.

10. Module: WDT

When the device is configured for either EC or RC oscillator modes, with the Power-up Timer enabled, bit $\overline{TO}$ of the RCON register (RCON<3>) may default to '0', even though no WDT time-out has occurred.

The $\overline{TO}$ bit functions normally in all other configurations.

Work around

1. Use bit $\overline{TO}$ in conjunction with bit $\overline{POR}$ (RCON<1>), to determine if a RESET condition has occurred.

11. Module: I/O (PORTB Interrupt-on-Change)

The RB Port Change Flag bit of the INTCON register (RBIF, INTCON<0>) may be inadvertently cleared, even when the PORTB<7:4> pins have not been read. This will occur only when the following two conditions occur simultaneously:

- The four Least Significant bits of the BSR register are equal to 0Fh (BSR<3:0> = '1111'), and
- Any instruction that contains 81h in its 8 Least Significant bits (i.e., register file addresses, literal data, address offsets, etc.) is executed.

Work around

All work arounds will involve setting the contents of BSR<3:0> to some value other than 0Fh. In addition to those proposed below, other solutions may exist.

1. When developing or modifying code, keep these guidelines in mind:
   - Assign 12-bit addresses to all variables. This allows the assembler to know when Access Banking can be used.
   - Do not set the BSR to point to Bank 15 (BSR = 0Fh).
   - Allow the assembler to manipulate the Access bit present in most instructions. Accessing the SFRs in Bank 15 will be done through the Access Bank. Continue to use the BSR to select Banks 1 through 5, and the upper half of Bank 0.
2. If accessing a part of Bank 15 is required and the use of Access Banking is not possible, consider using indirect addressing.
3. If pointing the BSR to Bank 15 is unavoidable, review the absolute file listing. Verify that no instructions contain 81h in the 8 Least Significant bits, while the BSR points to Bank 15 (BSR = 0Fh).

12. Module: Interrupts

When an interrupt occurs simultaneously with the clearing of one or more interrupt enable flags in the INTCON, PIE1 or PIE2 registers, the instruction immediately following the interrupted instruction may be executed before vectoring to the Interrupt Service Routine (ISR). If that instruction is a control operation, the ISR may not execute as intended.

In the case of conditional branch instructions, the first instruction of the ISR may be skipped if the tested condition would have resulted in a branch.

In the case of GOTO, CALL, or BRA instructions, program execution may vector to the address encoded in the instruction; the ISR will not be executed at all. The GIE bit will still be cleared, disabling all interrupts.

Additionally, on return from the interrupt (by executing RETFIE), the instruction following the interrupted instruction may be executed again.

There may be other interrupt related symptoms.

Work around

Three possible solutions are presented here. Other solutions may exist. None of these require special attention when setting interrupt enable bits.

1. All instructions that clear interrupt enable bits should be followed by a NOP instruction.
2. Prior to disabling any interrupt source, disable all interrupts by clearing the GIE bit (INTCON<7>). After disabling the desired interrupts, re-enable all interrupts by setting GIE.
3. If interrupt priority is being used:
   a) clear both GIEL and GIEH (in order) bits (INTCON<7:6>) to disable all peripheral interrupts
   b) clear the desired interrupt enable bits
   c) set both GIEH and GIEL, in order to re-enable peripheral interrupts

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39026**C**), the following clarifications and corrections should be noted.

1. Module: Brown-out Reset (BOR)

The voltage selection ranges for the BOR module (parameter D005) have changed. The new values are shown in Table 1 (below).

2. Module: Low Voltage Detect (LVD)

The voltage selection ranges for the LVD module (parameter D420) have changed. The new values are shown in Table 2 (below).

3. Module: Timer1

Section 11.1 (Timer1 Operation) is amended with the following clarification:

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become unpredictable.

If an application requires that Timer1 be turned off and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first, by clearing the T1SYNC bit of register T1CON. Please note that this may cause Timer1 to miss up to one count.

TABLE 1: MINIMUM AND MAXIMUM BROWN-OUT RESET VOLTAGE SPECIFICATIONS

Param No	Symbol	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D005	V_{BOR}	Brown-out Reset Voltage	BORV<1:0> = 11	2.35	—	2.80	2.50	—	2.66	V
			BORV<1:0> = 10	2.55	—	3.02	2.70	—	2.86	V
			BORV<1:0> = 01	3.95	—	4.71	4.20	—	4.46	V
			BORV<1:0> = 00	4.23	—	5.05	4.50	—	4.78	V

TABLE 2: MINIMUM AND MAXIMUM LOW VOLTAGE DETECT SPECIFICATIONS

Param No	Symbol	Characteristic		New Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D420	V_{LVD}	Low Voltage Detect	LVV<3:0> = 0100	2.35	—	2.80	2.5	—	2.66	V
			LVV<3:0> = 0101	2.55	—	3.02	2.7	—	2.86	V
			LVV<3:0> = 0110	2.64	—	3.14	3.0	—	2.98	V
			LVV<3:0> = 0111	2.83	—	3.37	3.0	—	3.20	V
			LVV<3:0> = 1000	3.11	—	3.71	3.3	—	3.52	V
			LVV<3:0> = 1001	3.29	—	3.93	3.5	—	3.72	V
			LVV<3:0> = 1010	3.39	—	4.04	3.6	—	3.84	V
			LVV<3:0> = 1011	3.58	—	4.26	3.8	—	4.04	V
			LVV<3:0> = 1100	3.77	—	4.49	4.0	—	4.26	V
			LVV<3:0> = 1101	3.95	—	4.71	4.2	—	4.46	V
			LVV<3:0> = 1110	4.23	—	5.05	4.5	—	4.78	V

4. Module: Electrical Specifications

The operating frequency range for extended temperature devices has been changed.

The maximum external clock frequency (EC and ECIO modes) and oscillator frequency (HS mode) for extended temperature devices has been changed to 25 MHz. When the PLL is used (HS+PLL mode), the maximum clock and oscillator frequency has been changed to 6.25 MHz. Other values of related parameters have changed accordingly.

Table 21-4, Parameters 1 and 1A of the Device Data Sheet are amended in part, as follows (changes and additions in **bold**):

TABLE 21-4: EXTERNAL CLOCK TIMING REQUIREMENTS

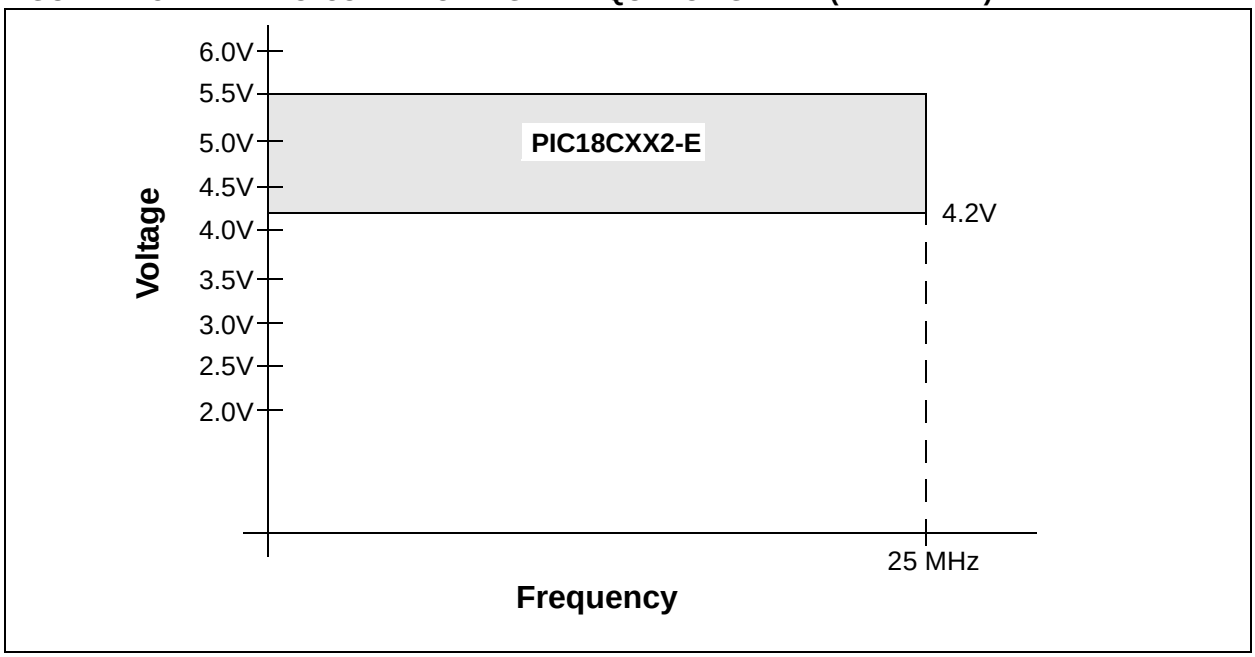
Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKIN Frequency	DC	40	MHz	XT osc **(Industrial)**
			DC	**25**	**MHz**	**XT osc (Extended)**
			DC	40	MHz	HS osc **(Industrial)**
			DC	**25**	**MHz**	**HS osc (Extended)**
			4	10	MHz	HS + PLL osc **(Industrial)**
			4	**6.25**	**MHz**	**HS + PLL osc (Extended)**
			DC	40	**MHz**	LP osc **(Industrial)**
			DC	**6.25**	**MHz**	**LP osc (Extended)**
			DC	40	MHz	EC, ECIO **(Industrial)**
			DC	**25**	**MHz**	**EC, ECIO (Extended)**
		Oscillator Frequency	DC	4	MHz	RC osc **(Industrial, Extended)**
			0.1	4	MHz	XT osc **(Industrial, Extended)**
			4	40	MHz	HS osc **(Industrial)**
			4	25	MHz	HS osc (Extended)
			4	10	MHz	HS + PLL osc **(Industrial)**
			4	**6.25**	**MHz**	**HS + PLL osc (Extended)**
			5	200	kHz	LP osc mode **(Industrial, Extended)**
1	TOSC	External CLKIN Period	**25**	—	ns	XT osc **(Industrial)**
			40	—	ns	XT osc (Extended)
			25	—	ns	HS osc **(Industrial)**
			40	**—**	**ns**	**HS osc (Extended)**
			100	**250**	ns	HS + PLL osc **(Industrial)**
			160	**250**	**ns**	**HS + PLL osc (Extended)**
			250	—	**ns**	LP osc **(Industrial, Extended)**
			25	—	ns	EC, ECIO **(Industrial)**
			40	**—**	**ns**	**EC, ECIO (Extended)**
		Oscillator Period	250	—	ns	RC osc **(Industrial, Extended)**
			250	**—**	ns	XT osc **(Industrial, Extended)**
			25	**—**	ns	HS osc **(Industrial)**
			40	**—**	**ns**	**HS osc (Extended)**
			100	250	ns	HS + PLL osc **(Industrial)**
			160	**250**	**ns**	**HS + PLL osc (Extended)**
			5	—	µs	LP osc **(Industrial)**

Note: Footnotes in original table omitted for the sake of brevity.

4. Module: Electrical Specifications (Continued)

Figure 21-3 (below), reflecting the voltage-frequency performance of extended temperature devices, is added to the Device Data Sheet:

FIGURE 21-3: PIC18CXX2 VOLTAGE-FREQUENCY GRAPH (EXTENDED)



In addition, the title of Figure 21-1 is amended to read:

"PIC18CXX2 Voltage-Frequency Graph (Industrial)"

5. Module: Interrupts

The operation of the GIE/GIEH bit (INTCON<7>) is clarified as follows: when the bit is cleared, all interrupts are disabled. This is regardless of the state of the IPEN bit (RCON<7>), the priority of the interrupt, or whether or not the interrupt is unmasked. This varies from the original description, in which clearing the bit when IPEN = '1' would only disable high priority interrupts.

The seventh paragraph in Section 7.0 of the Device Data Sheet (beginning "When an interrupt is responded to....") is amended by adding the following sentence to the end:

"It is important to note, however, that clearing the GIE/GIEH bit, regardless of the state of the IPEN bit, will disable **all** interrupts."

The changes to the bit descriptions in Register 7-1 in the Device Data Sheet are shown in the excerpt below (changes in **bold**).

Also, the interrupt logic funnel shown in Figure 7-1 of the Device Data Sheet is amended with the addition of a GIE/GIEH control line, as shown in Figure 1 (new material in **bold line**).

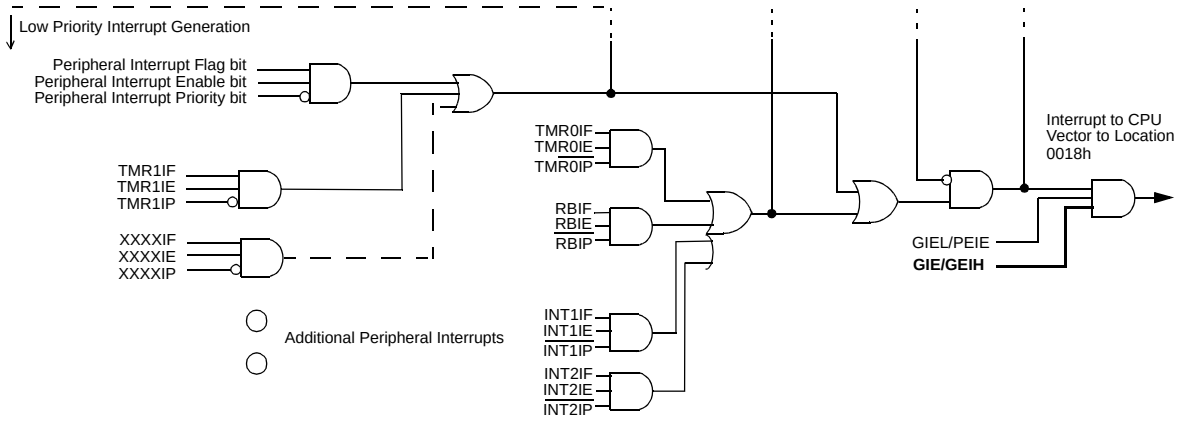
REGISTER 21-3: INTCON REGISTER (EXCERPT)

bit 7 **GIE/GIEH:** Global Interrupt Enable bit

When IPEN (RCON<7>) = 0:
1 = Enables all unmasked interrupts
0 = Disables all interrupts

When IPEN (RCON<7>) = 1:
1 = Enables all high priority interrupts
0 = **Disables all interrupts**

FIGURE 1: INTERRUPT LOGIC (EXCERPT)



6. Module: USART

The operation of the USART Transmit Interrupt flag bit TXIF (PIR1<4>) is clarified as follows:

TXIF is not cleared immediately upon loading data into the transmit buffer TXREG. The flag bit becomes valid in the second instruction cycle following the load instruction (see Example 1). Polling TXIF immediately following a load of TXREG will give invalid results (Example 2).

This clarification applies to **all** USART transmission modes (master or slave, synchronous or asynchronous, 8-bit or 9-bit).

EXAMPLE 1: CORRECTLY POLLING THE TXIF BIT

```
movwf   TXREG       ;load the register
nop                 :first instruction--
                    ;just a placeholder, it
                    ;could be any instruction
btfss   PIR1,TXIF   ;second instruction--
                    ;now TXIF is valid
```

EXAMPLE 2: POLLING THE TXIF BIT IMMEDIATELY AFTER LOADING THE TRANSMIT BUFFER

```
movwf   TXREG       ;load the register
btfss   PIR1,TXIF   ;first instruction--
                    ;reading TXIF now will
                    ;give invalid results
```

REVISION HISTORY

Rev H Document

Under Clarifications/Corrections to the Data Sheet, added Interrupt issue for GIE/GIEH bit (page 8, item 5).

Added USART issue (page 9, issue 6).

Rev G Document

Added Interrupt issue (page 4, item 12)

Under Clarifications/Corrections to the Data Sheet, added Electrical Specifications issue for extended temperature devices (pages 6 and 7, item 4).

Rev F Document

Added I/O Port (PORTB - Interrupt-on-Change) issue (page 4, item 11).

Rev E Document

Added Parallel Slave Port issue (page 2, item 6).

Added MSSP issue (page 3, item 7).

Added Interrupts issue (page 3, item 8).

Added Watchdog Timer (`CLRWDT`) issue (page 3, item 9).

Added WDT (osc modes) issue (page 3, item 10).

Under Clarifications/Corrections to the Data Sheet, added Timer1 issue (page 5, item 3).

Rev D Document

Added Corrections to BOR and LVD modules (page 3, items 1 and 2).

Rev C Document

Added ICSP issue (page 1, issue 3).

Added CCP (Compare mode) issue (page 2, issue 4).

Added Timer issue (page 2, issue 5).

Rev B Document

Added CCP silicon issue (page 1, issue 2).

Rev A Document

1st revision of this document.

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Detroit
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Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

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Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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