ALPHA & OMEGA SEMICONDUCTOR

AON6544
30V N-Channel AlphaMOS

General Description

• Latest Trench Power AlphaMOS (αMOS LV) technology
• Very Low $R_{DS(ON)}$ at 4.5V V_{GS}
• Low Gate Charge
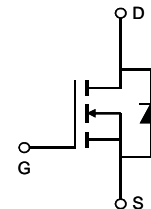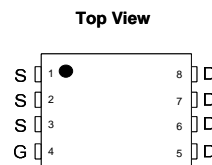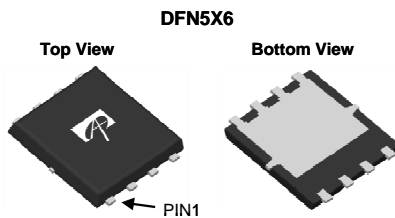• High Current Capability
• RoHS and Halogen-Free Compliant

Application

• DC/DC Converters in Computing, Servers, and POL
• Isolated DC/DC Converters in Telecom and Industrial

Product Summary

V_{DS}	30V
I_D (at V_{GS}=10V)	85A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 1.4mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 1.9mΩ

100% UIS Tested
100% R_g Tested

Green Product

DFN5X6

Top View   Bottom View

PIN1

Top View

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S [ 1 ●        8 ] D
S [ 2          7 ] D
S [ 3          6 ] D
G [ 4          5 ] D
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Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	85	A
	T_C=100°C		66	
Pulsed Drain Current [C]		I_{DM}	340	
Continuous Drain Current	T_A=25°C	I_{DSM}	60	A
	T_A=70°C		49	
Avalanche Current [C]		I_{AS}	75	A
Avalanche energy L=0.1mH [C]		E_{AS}	281	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	V
Power Dissipation [B]	T_C=25°C	P_D	83	W
	T_C=100°C		33	
Power Dissipation [A]	T_A=25°C	P_{DSM}	7.4	W
	T_A=70°C		4.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14	17	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1	1.5	°C/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	ID=250µA, V$_{GS}$=0V		30			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=30V, V$_{GS}$=0V				1	µA
			T$_J$=125℃			5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS,}$ I$_D$=250µA		1.4	1.8	2.2	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=20A			1.1	1.4	mΩ
			T$_J$=125℃		1.5	1.9	
		V$_{GS}$=4.5V, I$_D$=20A			1.5	1.9	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=20A			102		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.64	1	V
I$_S$	Maximum Body-Diode Continuous Current ^{G}					85	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=15V, f=1MHz			5910		pF
C$_{oss}$	Output Capacitance				2320		pF
C$_{rss}$	Reverse Transfer Capacitance				335		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		0.5	1	1.5	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=15V, I$_D$=20A			88	120	nC
Q$_g$(4.5V)	Total Gate Charge				41	56	nC
Q$_{gs}$	Gate Source Charge				13		nC
Q$_{gd}$	Gate Drain Charge				18.5		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=15V, R$_L$=0.75Ω, R$_{GEN}$=3Ω			13		ns
t$_r$	Turn-On Rise Time				10		ns
t$_{D(off)}$	Turn-Off DelayTime				51		ns
t$_f$	Turn-Off Fall Time				15		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=20A, dI/dt=500A/µs			29		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=20A, dI/dt=500A/µs			80		nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25°C. The Power dissipation P$_{DSM}$ is based on R $_{θJA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature T$_{J(MAX)}$=150°C.
D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
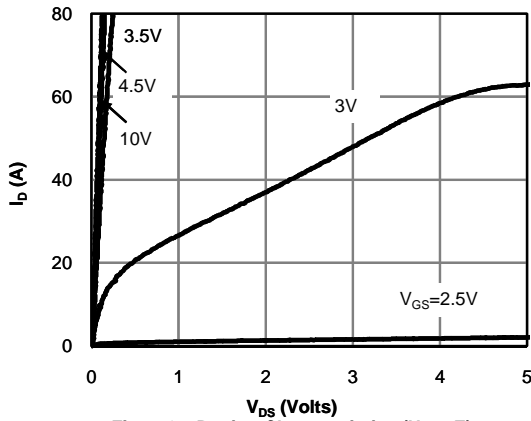F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
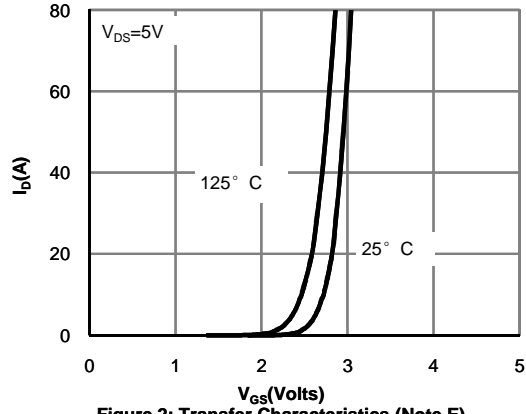G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25°C.

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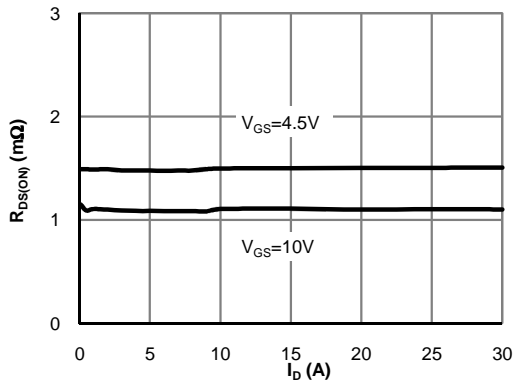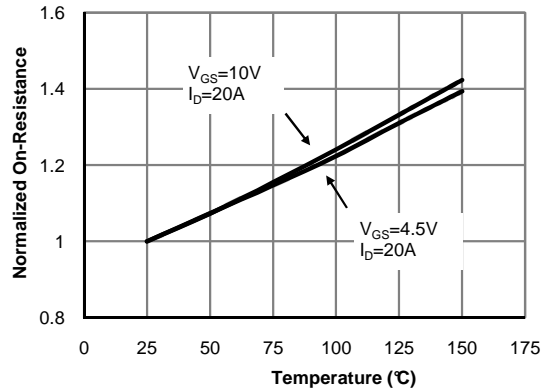
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics (Note E)
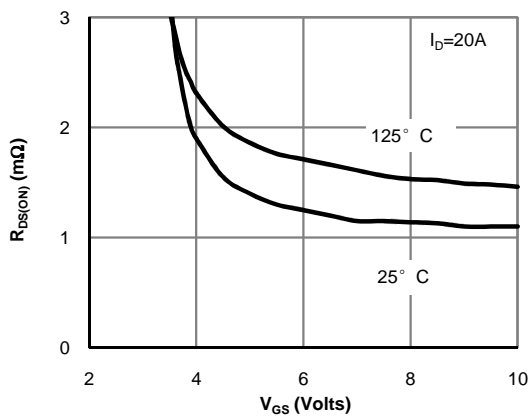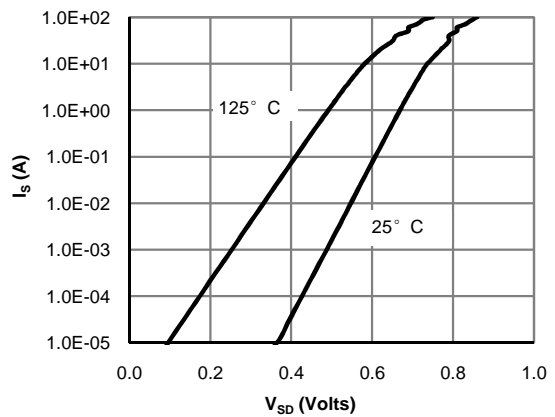
Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)
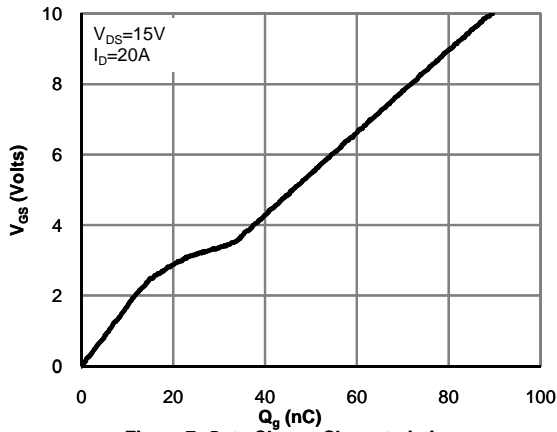
Figure 4: On-Resistance vs. Junction Temperature (Note E)
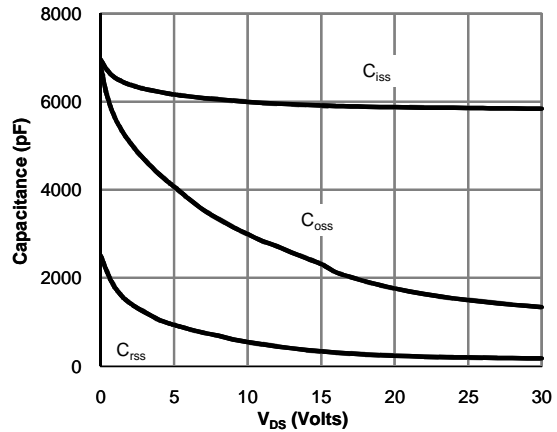
Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

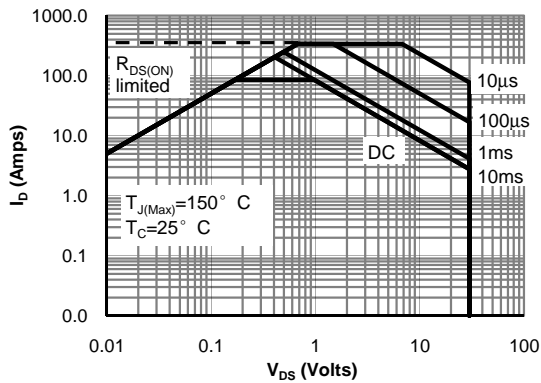# ALPHA & OMEGA SEMICONDUCTOR

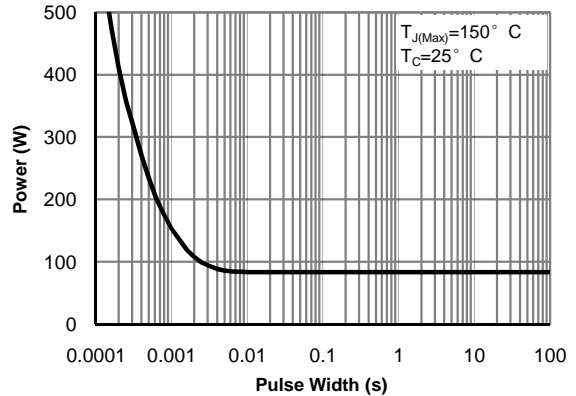## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
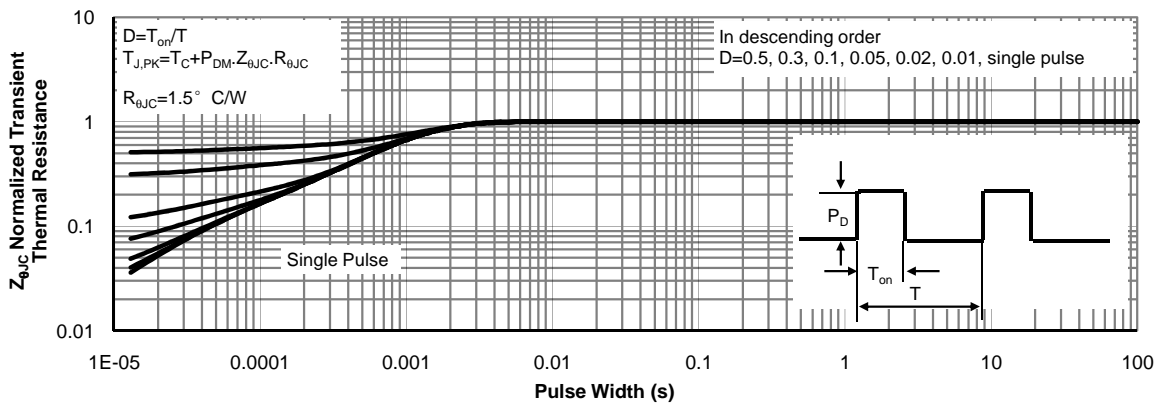

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics

VGS> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

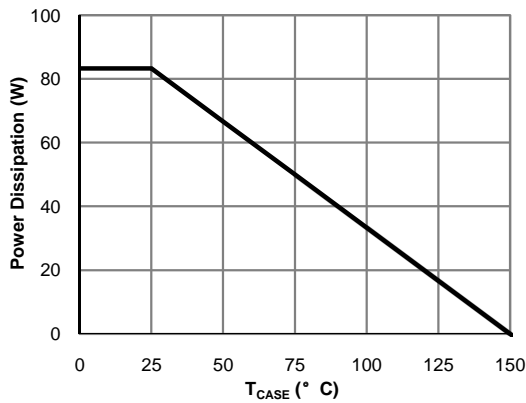**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**
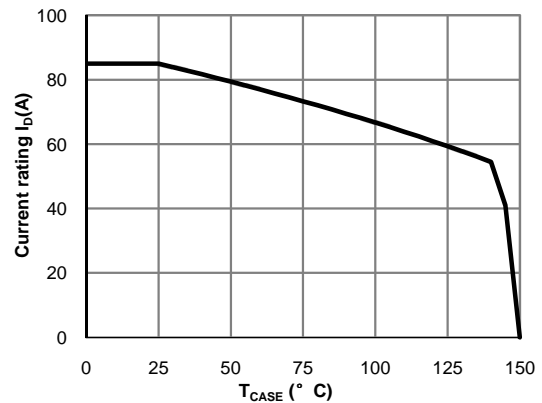

Figure 12: Power De-rating (Note F)
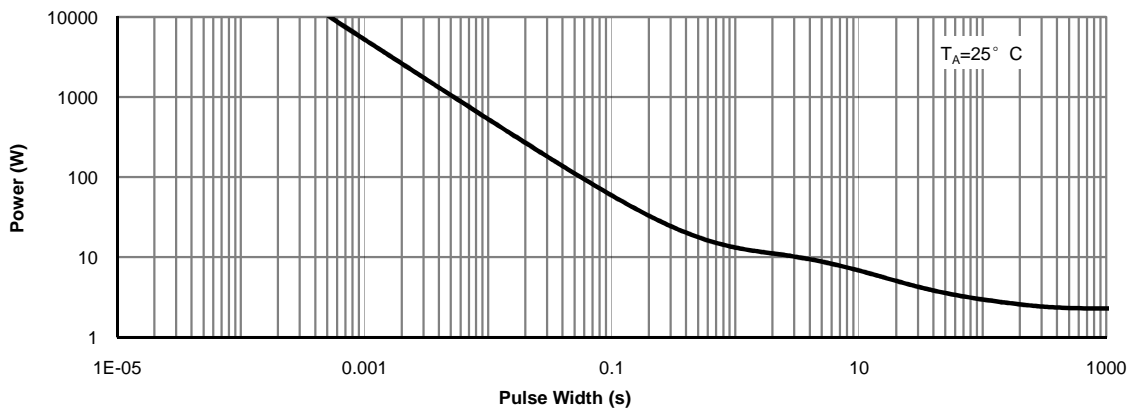

Figure 13: Current De-rating (Note F)

Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

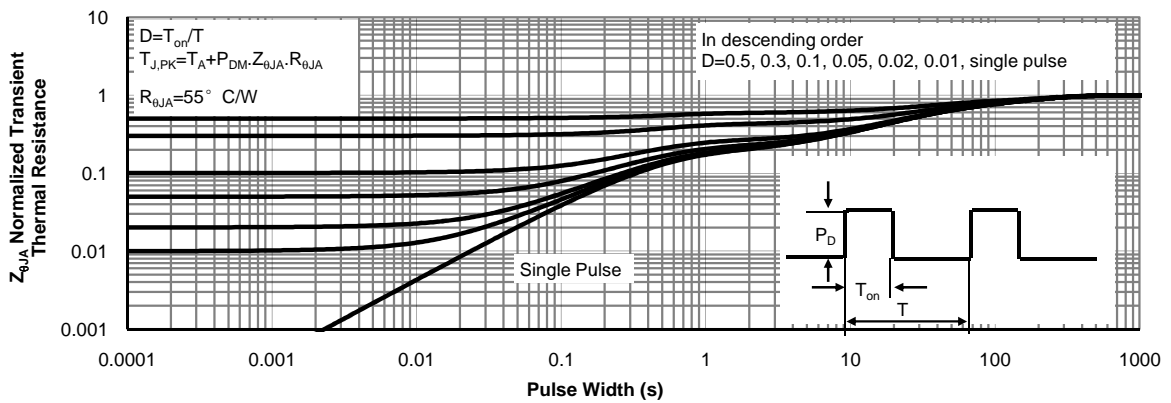$D=T_{on}/T$
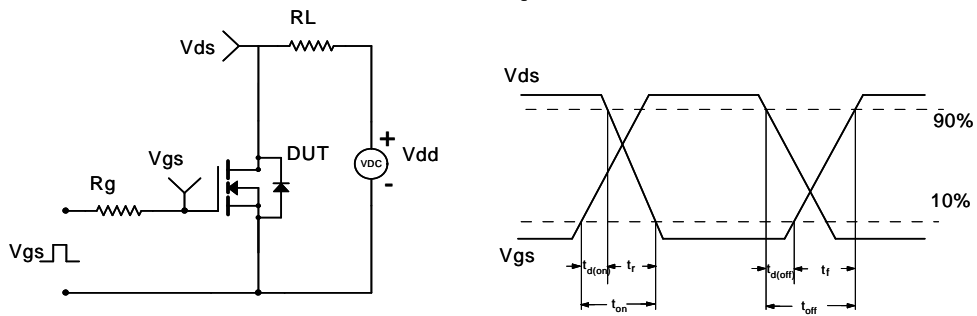$T_{J,PK}=T_A+P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA}=55°$ C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

ALPHA & OMEGA
SEMICONDUCTOR

Gate Charge Test Circuit & Waveform

VDC

DUT

Vgs

Ig

VDC

+ Vds -

Vgs

10V

Qg

Qgs Qgd

Charge

Resistive Switching Test Circuit & Waveforms

RL

Vds

Rg   Vgs   DUT   VDC   + Vdd -

Vgs

Vds

90%

10%

Vgs

$t_{d(on)}$ t_r

t_{on}

$t_{d(off)}$ t_f

t_{off}

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

L

Vds

Id

$\overline{Vgs}$

Rg   Vgs   DUT   VDC   + Vdd -

Vgs

$E_{AR} = 1/2\ LI^2_{AR}$

BV_{DSS}

Vds

Id

I_{AR}

Vgs

Diode Recovery Test Circuit & Waveforms

Vds +

DUT

Vds -

Isd

L

Vgs

Ig

VDC

+ Vdd -

$Q_{rr} = -\int Idt$

Vgs

Isd

I_F

dI/dt

t_{rr}

I_{RM}

Vds

Vdd