KIT33982CEVBE Evaluation Board
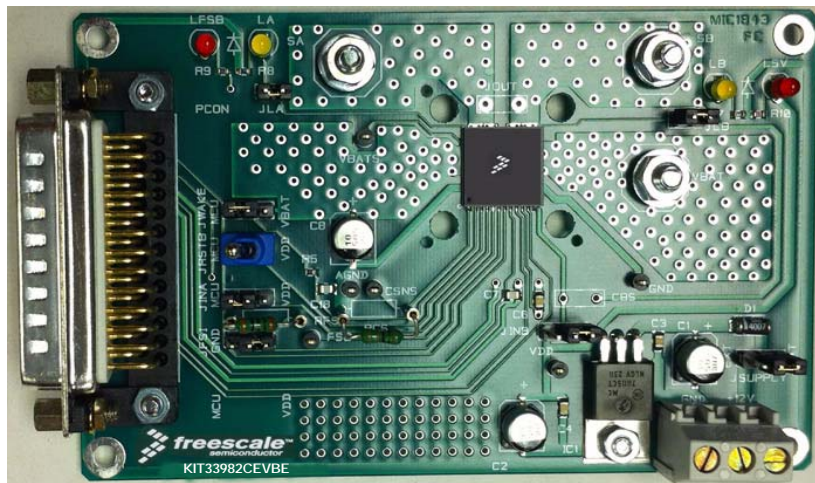

Figure 1. KIT33982CEVBE Evaluation Board

Table of Contents

1   Kit Contents / Packing List

- KIT33982CEVBE Evaluation Board (1)
- CD33982 (1)

2   Important Notice

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This EVB may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This EVB is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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3 Introduction

3.1 EVB Features

- Single 2.0mΩ max. high side switch with parallel input or SPI control
- 6.0 to 27V operating voltage with standby currents < 5.0µA
- Output current monitoring with two SPI-selectable current ratios
- SPI control of over-current limit, over-current fault blanking time, output-OFF open load detection, output ON/OFF control, watchdog timeout, slew rates, and fault status reporting
- SPI status reporting of over-current, open and shorted loads, over-temperature shutdown, under-voltage and over-voltage shutdown, fail-safe pin status, and program status
- Enhanced -16V reverse polarity V_{PWR} protection

3.2 Required Equipment

- Parallel port-enabled computer with Windows XP (or later) operating system
- Parallel cable
- Alternative: USB-enabled computer with Windows XP (or later) operating system and Freescale's USB to SPI EVB Kit (reference: KITUSBSPIEVME)

4   Hardware Description

The hardware in this evaluation kit includes an 33982 evaluation board. The evaluation board has three major blocks: the circuit related to the 33982, the remote control and accessory simulator (SPI Gen) and the parallel cable. This section describes the above three blocks.
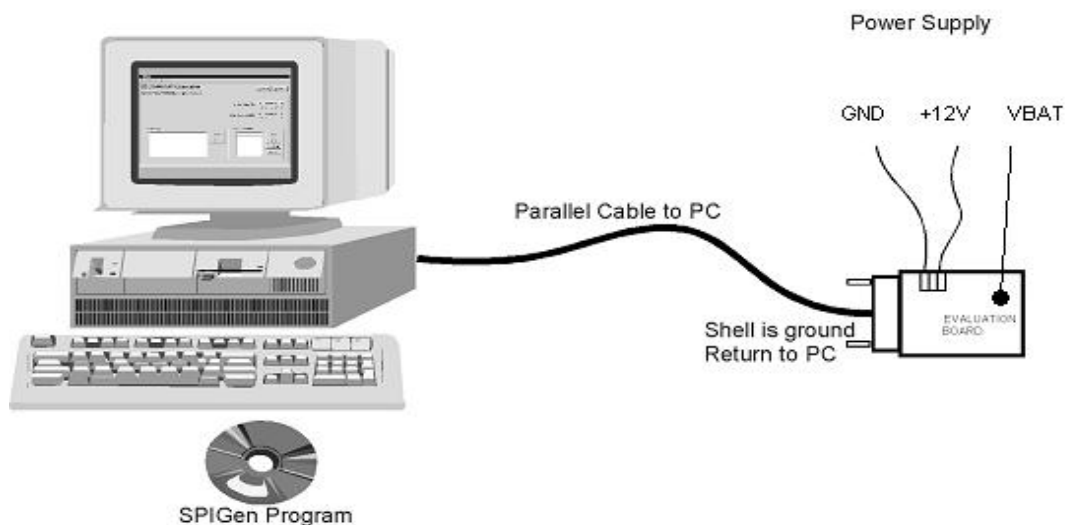
4.1   Using the EVB

Figure 2. Setup for the 33982 EVB

Warning: Always wear Safety Glasses when working around electronic modules and when soldering.

Please remove of the capacitor, C8, when testing reverse supply voltage on VBAT. Also that the thermal resistance from junction to ambience of this PCB is approximately 25°/W.

1. The 33982 Evaluation board allows the customer to quickly evaluate features of the device with a simple bench top setup. All switch inputs may be evaluated using the onboard switch banks or actual system switches connected to the switch input edge connector.

2. Using a standard 25 pin Sub-D parallel port cable and the enclosed SPIGen SPI Driver software, you can use a personal computer to provide the Serial Peripheral Interface (SPI) communication with this EVB.

3. Connect power supplies to the VBAT on the VBAT bolt. Connect GND, GNDBAT and +12 volt supply on connector X, EVB's power terminal. On-board 5 volt regulator supply can be either supplied through VBAT or +12V by selecting the jumper JSUPPLY. Make sure the voltages provided are in accordance with the device data sheet and that the supply currents are sufficient to supply the attached loads. The led L5V should light up indicating the presence of 5 volt regulated supply. Move IC from reset state by shorting jumper JRSTB to 2-3 position (It shorts RSTB PIN to VDD).

4. Connect the desired loads to (e.g. relay coils, LEDs, or panel lamps) SB and SA bolt.

5. For direct control of SA, put jumper, JINA, at position 2-3. For direct control of SB, put jumper, JINB, at position 2-3. Disable watchdog placing a jumper at JFSI on position1-2 (shorting the PIN to GND) and not placing jumper on JWAKE. (Shorting PIN to GND). Led LA and LB should light up if jumper are placed on JLA and JLB.

6. To use SPIGen, Go to the Windows Start menu, then Programs, then SPIGen, and click on the SPIGen icon. The SPIGen "Generic SPI Generator" GUI will appear. Go to the File menu in the upper left hand corner of the GUI, and select Open, then browse the CD to find and select the 33982_EVB_CONFIGURATION_FILE.spi file for the KIT33982CEVBE. Click Open, and SPIGen will open a specifically configured SPI command generator for the KIT33982CEVBE. The configuration file will set all parameters for SPI signals from the PC and provide a list of commands that may be sent to the EVB.

7. To prepare the Evaluation card for SPIGen, Place jumper JINA, JINB, JRSTB, JWAKE to 1-2 position

8. To set up the 33982 device to read switch inputs the user may use the batch commands from the "Send a Batch of Commands" tab. In the "Send a Batch of Commands" window, the Full Initialize batch will appear. To send the batch of commands to the EVB, click the Send Once tab. To quickly evaluate the EVB and device, simply click on the "Send one Command at a Time" tab, select the switch status command from the Quick Commands list, and click the Send Continuous tab. The opening and closing of switches may now be seen on the Word Received bits window field. Refer to the device data sheet for detailed information on I/O communication and device operation.

5 Jumper Connections

Name	Description
JSUPPLY	The selection between 1-2 allows the supply regulation of the 5 volt from Battery while 2-3 allows independent supply.
Diode **D1** Capacitor **C8**	Diode protects against negative transients and reverse battery. Removed when doing reverse battery test.
JWAKE	Allows wake up function of IC. 1-2 selection will give control through PCON. 2-3 selection is to wake up from battery voltage, i.e. in the case of ignition.
JINA	1-2 position: control through PCON to SPIGEN 2-3 position: shorting IN0 to VDD Floating: IN0 is short to ground
JINB	NC
JRSTB	1-2 position: control through PCON to SPIGEN/MCU 2-3 position: Short RSTB to VDD Floating: RSTB is ground. This means that the IC is in reset mode
JFSI	1-2 position: Short JFSI to ground 2-3 position: Connect to RFSI resistor Floating: JFSI is pulled to VDD
JLA	1-2 position: connect to led, LA. LA lights up when IN is pulled to VDD Floating: Not connected to LA.
JLB	1-2 position: connect to led, LB. LB lights up when IN is pulled to VDD Floating: Not connected to LB
Resistor **RCS** **RFSI**	 Value to be change according. Value to be change according.
TEST POINTS CSNS-AGND	Several test points are present on the evaluation board to check some signals if necessary: To check the current recopy output

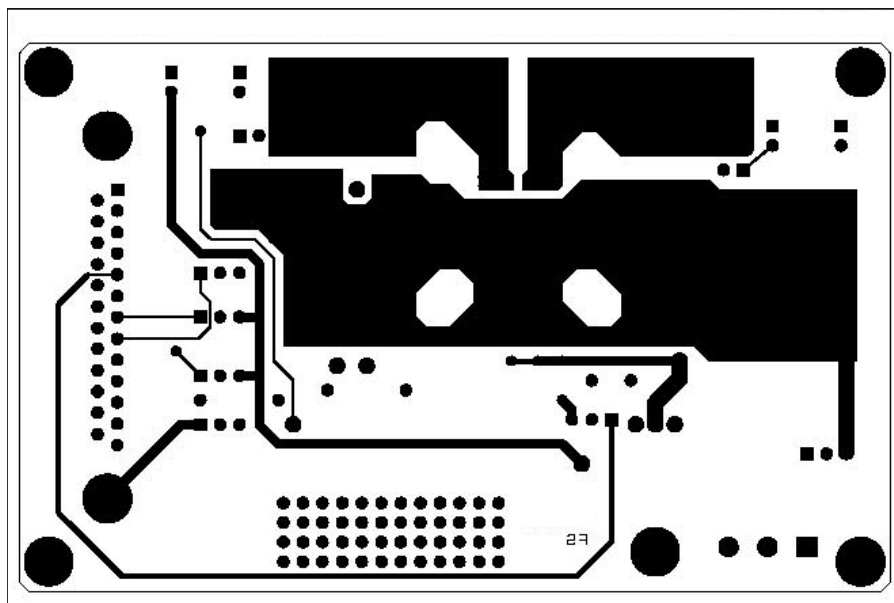# 6   Schematic Drawing

Figure 3. Evaluation Board Schematic

7   KIT33982CEVBE Board Layout

7.1   Assembly Drawing

Figure 4. Assembly Drawing

7.2   Top Layer

Figure 5. Top Layer

7.3   Bottom Layer

Figure 6. Bottom Layer

8   Bill of Material

Qty	PN	Ref. Des	Package	Description
1	**MC33982CPNA**	**MC33982**	**PQFN**	**Intelligent High Current Self-Protected Silicon High-Side Switch**
1	7805	REG	TO220	5V Regulator
3	ECEV1HA 100SP	C1, C2, C8	CMS D	10uF 50V Capacitor
3		C3, C4, C6	805	100nF 50 V Capacitor
2		C7, C18	805	100pF 50 V Capacitor
3		R5, R7, R8	603	10k 5% 0,1W Resistor
2		R9, R10	603	2k2 5%(or 2k7) Resistor
1		RCS	Thru hole NON-CMS	1k 1/4W 1% Resistor
1		RFSI	Thru hole NON-CMS	200 1/4W 5% Resistor
4	H3192		Thru hole	Connector to hold resistor RCS and RFSI
2	HLMP1719	LB, LA	Thru hole NON-CMS	2mA yellow leds
2	HLMP1700	LFSB, L5V	Thru hole NON-CMS	2mA red leds
1	MRA4007T3	D1	SMA	DIODE MRA4007 (equiv. 1N4007)
6	Type1 5001	FSB, CSNS, VDD, AGND, VBAT, GND		Testpoints for clip
1	MKDS 1,5/3-5,08	X	5,08mm	3 terminal Power connector Standard 5,08mm
3		VBAT, SA, SB	Metal with 4mm diam.	Screw connecters diam. 4mm +1 Nut + 2 washers each for power connection
1	DB25P564TX	PCON	M25H	Connector, SubD, series D, male, bent barb, to solder 25 contacts
6	M7566-05	JINA, JINB, JSUPPLY, JFSI, JWAKE, JRSTB		JUMPER : 3 PINS + 1 jumper socket 2.54mm
2	M7566-05	JLA,JLB		JUMPER : 2 PINS + 1 jumper socket 2.54mm

Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application

9   References

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10 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	10/2010	• Initial Release

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