3MHz 4A High Efficiency Step-Down Converter with I²C Interface

General Description

The RT8092 is a Peak-Current Mode Pulse-Width-Modulated (PWM) step-down DC/DC converter with I²C control interface. Capable of delivering 4A continuing output current over a wide input voltage range from 2.5V to 5.5V, the RT8092 is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals.

Internal synchronous rectifier with low $R_{DS(ON)}$ dramatically reduces conduction loss at PWM mode. No external Schottky barrier diode is required in practical application. The RT8092 enters low-dropout mode when normal PWM cannot provide regulated output voltage by continuously turning on the upper P-MOSFET. The RT8092 enters shut-down mode and consumes less than 5μA when the EN pin is pulled low. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 3MHz. This along with small WL-CSP-15B 1.2x2 (BSC) and WQFN-14L 3.5x3.5 packages provides small PCB area applications.

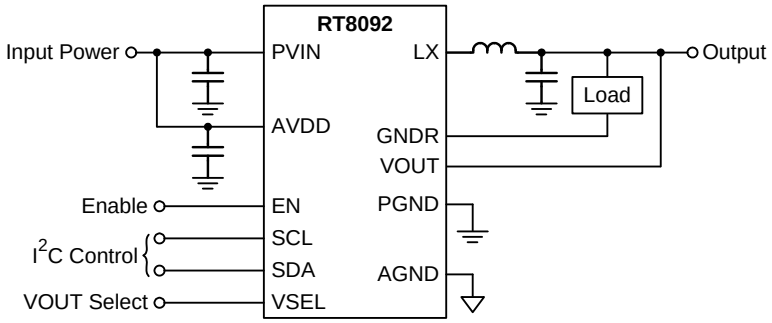
To increase battery life time, the RT8092 provides low power mode with I_Q < 15μA in standby and light-load applications. The RT8092 also includes Dynamic Voltage Scaling (DVS) for system low power applications.

The I²C interface let the RT8092 controllable flexibly to select V_{OUT} voltage level, peak current limit level, PWM control mode, and so on. Other features include soft-start, auto discharge, lower internal reference voltage, over-temperature, and over-current protection.

Features

- **2.5V to 5.5V Input Range**
- **Low Operation Quiescent Current**
  - **Normal Mode I_Q < 60μA**
  - **Low Power Mode I_Q < 15μA**
- **Output range From 0.3V to 5.5V**
  - **Bank 0 : 0.3V to 0.7V**
  - **Bank 1 : 0.6V to 1.4V**
  - **Bank 2 : 1.2V to 2.8V**
  - **Bank 3 : 2.4V to 5.5V**
  - **The Default Value is 2.8V (VSEL = High) and 1V (VSEL = Low)**
- **4A Continuing Output Current**
- **Support DVS in the Same Bank**
  - **V_{OUT} Adjusting Range (max, min) is Settable**
- **High Efficiency**
  - **90% at 5V → 2.8V with 1.5A Load**
- **3MHz Fixed-Frequency PWM Operation**
  - **Auto-PSM/PWM or Force-PWM Selectable**
- **Support Remote Ground Sensing for Accurate Output Voltage**

Simplified Application Circuit



- **Dedicated Hardware Pin to Immediately Switch Nominal Output Voltage Setting**
- **Output Discharging when Turning Off**
- **Over-Current Protection**
  - **OC Level Settable**
- **Over-Temperature Protection**
- **Integrated Soft-Start Function**
- **Enabling Control by Enable Pin and I^2C Register Setting by Software**
- **I^2C Interface**
  - **I^2C Communication allowed Even in Off-State (EN = L)**
  - **Support Fast Mode (400kbps)**
  - **Registers Setting Retained in Off-State (EN = L)**
- **RoHS Compliant and Halogen Free**

Applications

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- MP3 Players
- Portable Instruments

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Ordering Information

RT8092□□□

- Package Type
  WSC : WL-CSP-15B 1.2x2 (BSC)
  QW: WQFN-14L 3.5x3.5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  (For WQFN-14L 3.5x3.5 Only)
- VSEL Option
  VSEL = High / Low, the target voltage follows as below table.
  Default : 2.8V / 1V
  JC : 1.8V / 1.2V
  UR : 2.8V / 2.5V
  AB : 1.0V / 1.1V
  CF : 1.2V / 1.5V
  :
  :

Note :

Richtek products are :

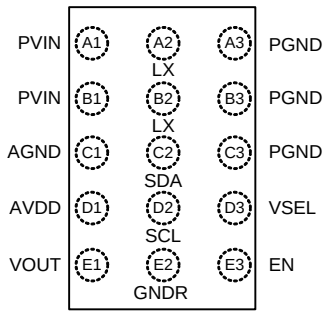
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

VSEL Option : (Unit : V)

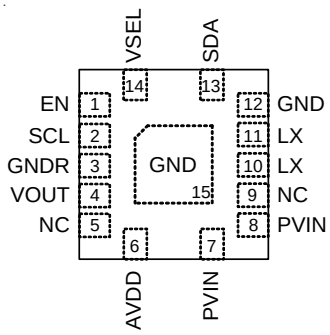
Code	Voltage	Code	Voltage	Code	Voltage
A	1.0	B	1.1	C	1.2
D	1.3	E	1.4	F	1.5
G	1.6	H	1.7	J	1.8
K	1.9	L	2.0	M	2.1
N	2.2	P	2.3	Q	2.4
R	2.5	S	2.6	T	2.7
U	2.8	V	2.9	W	3.0
X	3.3				

Pin Configurations

(TOP VIEW)



WL-CSP-15B 1.2x2 (BSC)

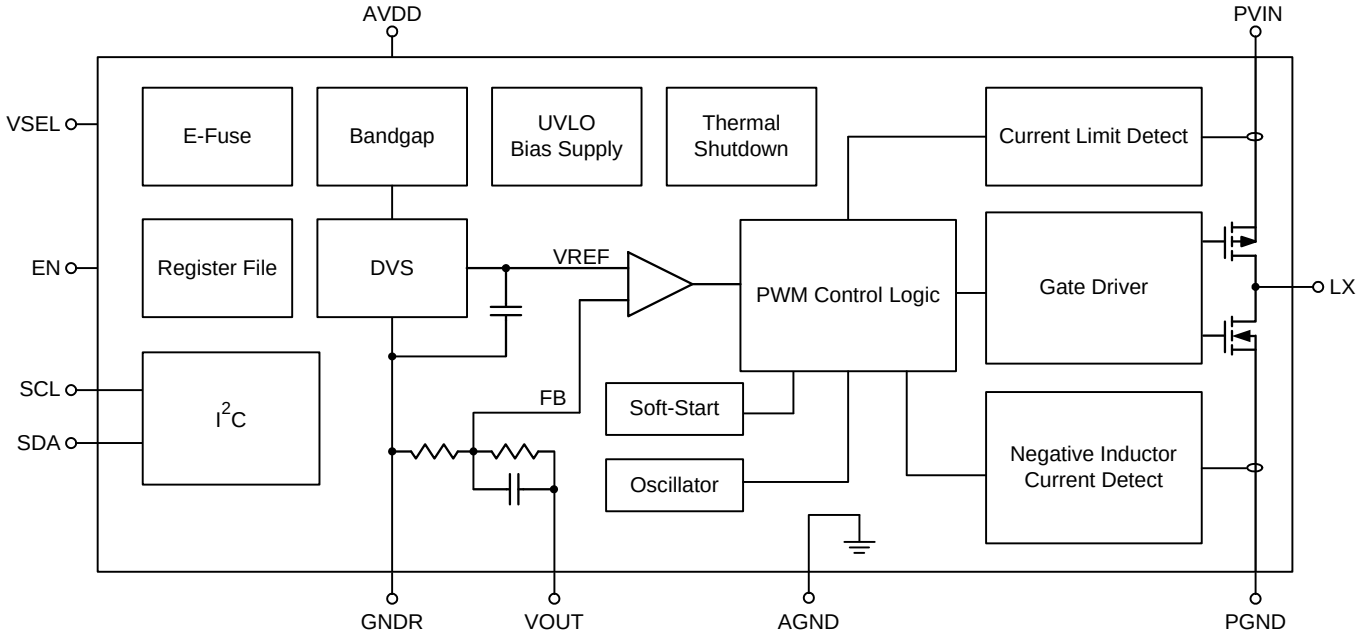


WQFN-14L 3.5x3.5

Functional Pin Description

Pin No.		Pin Name	Pin Function
WL-CSP-15B 1.2x2	WQFN-14L 3.5x3.5		
A1, B1	7, 8	PVIN	Power Input. Input capacitor C_{IN} must be placed as close to IC as possible.
A2, B2	10, 11	LX	Switch Node.
A3, B3, C3	--	PGND	Power Ground.
C1	--	AGND	Analog Ground.
C2	13	SDA	I^2C Interface Data Input.
D1	6	AVDD	Analog and I^2C Interface Power Input.
D2	2	SCL	I^2C Interface Clock Input.
D3	14	VSEL	Nominal VOUT setting select input pin. VSEL = Low selects {0x11.ENSEL0, 0x11.VoutSEL0[6:0], 0x14.PWM0}. VSEL = High selects {0x10.ENSEL1, 0x10.VoutSEL1[6:0], 0x14.PWM1}.
E1	4	VOUT	Step-Down Converter Output Voltage Sense Input.
E2	3	GNDR	Remote Ground Sense Input.
E3	1	EN	Enable Control Input. The IC enable control pin turns on the step-down converter if the internal register ENSEL bit = 1. If ENSEL = 0, EN goes high still cannot enable step-down converter. The EN pin includes a internal pull-down current about 1μA. When IC protection occurs and is latched in shutdown state, toggling EN or re-power AVDD can reset the latch state.
--	5, 9	NC	No Internal Connection.
--	12, 15 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



Operation

The RT8092 is a low voltage synchronous step-down converter that can support the input voltage range from 2.5V to 5.5V and can deliver up to 4 A at an I^2C selectable voltage ranging from 0.3 V to 5.5 V, distributed into 4 banks of output voltages. The converter can operate in Auto mode or forced PWM mode. Operating modes and output voltage can be selected via I^2C.

By adapting current mode architecture, converter decides its switching duty by inductor current sense information, compensation ramp and error amplifier output. The converter turns on the high-side P-MOSFET whenever the raising edge of the switching clock. After the decided duty time, the high-side P-MOSFET would be turned off and the low-side N-MOSFET would be turned on until the next frequency clock raising in forced PWM mode or turn off by ZC (Zero Current Detection) in auto mode. The error amplifier may adjust its output, COMP, with selected voltage reference and output feed-back voltage information. Different selection of voltage reference and different loading at output node regulate the required COMP voltage, which regulating the output voltage.

VSEL Function for Immediately Voltage Change

To address different performance operating points and startup conditions, the device offers two output voltage / mode presets, which can be chosen via a dedicated VSEL pin; this allows simple and zero latency output voltage transition.

Operating Mode Selection

The converter can operate in Auto mode or forced PWM mode. It can be selected by programming register 0x14.PWM0 for VSEL = Low or 0x14.PWM1 for VSEL = High. If Auto mode is selected, the converter automatically switches the operation mode between PWM and PSM according to the load conditions. If forced PWM mode is selected, the converter works only in PWM mode.

PWM (Pulse Width Modulation) Operating Mode

The converter operates in PWM (Pulse Width Modulation) mode from medium to heavy load. In PWM mode, the converter operates with its nominal switching frequency of 3MHz, and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM.

Forced PWM (FPWM) Operating Mode

If forced PWM mode is selected, the converter works only in PWM mode, and disables the transition from PWM to PSM as the load decreases. The advantage of forced PWM is that the switching frequency is fixed to be 3MHz, and thus it is easy for EMI immunity design. The disadvantage is that the efficiency at light load is poor due to the negative inductor current.

Pulse Skipping Modulation (PSM) Operating Mode

When in Forced PWM operating mode without output current loading, half of FPWM inductor current is negative to balance total average zero output current. If that negative inductor current could be saved, the efficiency will be improved strongly. PSM is one Buck operation mode with zero inductor current detection. Whenever zero current occur, the low-side N-MOSFET is turned off immediately and save the resident power into output capacitor (store energy in higher V_{OUT}). Then, the converter skips internal synchronous clock and keeps sleep-state until output voltage is discharged to below its target value. Once skips occurs, the power MOSFETs of converter is turned off and lots of sub-block circuits is in sleep state to save quiescent consumption. If the output loading is increasing, the discharge time is shortened, i.e. the switching frequency depends on the output loading. The switch frequency is decayed from 3MHz; the lighter output loading, the lower switch frequency. As result, PSM V_{OUT} ripple would be slightly larger than FPWM but PSM gains significant efficiency improvement.

Auto-Zero Current Detector

The Auto-Zero Current (AZC) detector circuit senses the LX waveform to adjust the inductor zero current threshold voltage automatically. In traditional trimmed zero current detectors, the zero current threshold changes due to V_{IN} / V_{OUT} variation. This would degrade efficiency due to

the extra power consumption by body diode or negative inductor current. Regard with this defect, AZC adjusts current threshold continuously when the RT8092 is operating. With AZC circuit, the RT8092 could avoid negative current in PSM mode and could achieve higher efficiency performance.

Minimum Peak Current

Minimum peak current is an evolution version from minimum on time. Rather than fixed minimum on time, Minimum peak current produce the "effective minimum on time" which could be adjusted according to V_{IN}/V_{OUT} condition.

$$T_{ON} = \frac{L}{V_{IN} - V_{OUT}} \times I_{MIN\_Peak}$$

It's an advantage to not provide too much energy at low duty; also, to not provide too less energy at high duty. When the converter is in PSM operation, every time pulse skip duration finishes, the converter will provide current energy for output loading by turning on P-MOSFET until inductor current achieve minimum peak current.

Low Power Mode (LPM)

The RT8092 provides Low Power Mode (LPM) to save more quiescent consumption. With maximum output current ability, 1mA, LPM enhances the efficiency at load below 100μA, more than the Pulse Skipping Mode (PSM) does. This extremely efficiency improvement may extend battery life, especially in stand-by mode of hand held products.

Enabling

The converter can be enabled or disabled by IC pin, EN. For more flexibility, users can turn on/off the converter by I^2C programming. There are ENSEL register bit located in register 0x10.ENSEL1 and 0x11.ENSEL0 to control internal enable signal for both VSEL selection high/low.

Dynamic Voltage Scaling (DVS)

Users can select required output voltage bank and preferred output voltage by I^2C programming. When output voltage is changed, the RT8092 provides Dynamic Voltage Scaling (DVS) skill to prevent any undershoot or overshoot when output voltage transition. The DVS means to adjust one reference voltage into another reference voltage in steps smoothly. The slew rate of the internal reference voltage is around 3mV / 10μs. Please note DVS function could only be available in the same output voltage bank.

Remote Ground Sensing

The RT8092 can deliver output current up to 4A. Inevitably, there is voltage drops due to the routing trace resistance between output node and chip location, especially when heavy loading. Also, voltage drops exist in ground trace. Remote ground sensing pin, GNDR, can tell the converter the lost drops to compensate to the correct and accuracy voltage level.

Active Output Discharge

To make sure that no residual voltage remains in the power supply rail, an active discharge path can ground the output voltage. The output gets discharged by the LX pin with a typical discharge resistor when the device shuts down. This feature can be easily disabled or enabled with register 0x12.Discharge. By default the discharge path is active. The default value of the feature is factory programmable.

Power Good

When the output voltage is higher than Power Good rising threshold, the Power Good flag, register 0x01.SEN_PG is high.

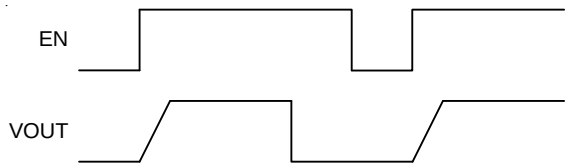
Under-Voltage Lockout (UVLO)

The UVLO continuously monitors the PVIN voltage to make sure the device works properly. When the PVIN is high enough to reach the UVLO high raising threshold voltage, 2.4V, the converter softly starts. When the PVIN decreases to its UVLO low threshold voltage, 2.3V, the device will shut down. The event is recorded in register 0x18.PVIN_UVLO. The record can be reset with I^2C interface or automatically reset by re-power-on AVDD.

Output Under-Voltage Protection (UVP)

When the output voltage is lower than UVP threshold (~50% of nominal target) after soft-start, the UVP is triggered. The converter will be latched and the output voltage will no longer be regulated during UVP latched state. Re-power-on input voltage or EN pin can unlatch

the protection state. Using I^{2}C to shutdown the system and then re-enable it will also unlatch UVP function. The event is recorded in register 0x18.SCP. The record can be reset with I^{2}C interface or automatically reset by re-power-on AVDD.



Over-Current Protection (OCP)

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, The OCP is cycle-by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit. The event is recorded in register 0x18.OCP. The record can be reset with I^{2}C interface or automatically reset by re-power-on AVDD. The OCP level can be set with 0x16.IPEAK[1:0].

Over-Temperature Protection (OTP)

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVIN and AVDD ---------- 6V
- Switch Node DC Rating, LX ---------- 6V
- EN, VOUT, SCL, SDA Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-15B 1.2x2 (BSC) ---------- 1.92W
  WQFN-14L 3.5x3.5 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  WL-CSP-15B 1.2x2 (BSC), θ_{JA} ---------- 51.9°C/W
  WQFN-14L 3.5x3.5, θ_{JA} ---------- 30°C/W
  WQFN-14L 3.5x3.5, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, AVDD and PVIN ---------- 2.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C
- Input Capacitance ---------- 10µF
- Output Capacitance ---------- 22µF
- Inductance ---------- 0.33µH

Electrical Characteristics

(V_{IN} = 3.6V, V_{OUT} = 1V, L = 0.33µH, C_{IN} = 10µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Start-up	V_{IN}	AVDD and PVIN	2.45	--	5.5	V
Input Voltage Range	V_{IN}	I_{OUT} = 2A	2.5	--	5.5	V
Quiescent Current (Normal Mode)	I_{Q_nor}	I_{OUT} = 0mA, No Switching, LPM = 0	--	60	--	µA
Quiescent Current (Low Power Mode)	I_{Q_lpm}	I_{OUT} = 0mA, No Switching, LPM = 1	--	--	15	µA
GNDR Current	I_{GNDR}	I_{OUT} = 0mA, No Switching	--	--	10	µA
Shutdown Current	I_{SHDN}	EN = GND	--	1	5	µA
Adjustable Output Range for Internal Feedback Network	V_{OUT}	SDA = SCL = High at AVDD Power On, 0x1D.VOUT_BANK[1:0] = 2'b10	1.2	--	2.8	V
Output Voltage Accuracy in Normal Mode	V_{OUT}	V_{IN} = 2.5V to 5.5V, 0A < I_{OUT} < 2.7A	–2	--	2	%

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy in Low Power Mode		V_{OUT}	$V_{IN} \geq V_{OUT}$ + 1V, 0A < I_{OUT} < 1mA	–5	--	5	%
P-Channel On-Resistance		$R_{DS(ON)\_P}$	V_{IN} = 3.6V, I_{OUT} = 200mA	--	40	--	mΩ
N-Channel On-Resistance		$R_{DS(ON)\_N}$	V_{IN} = 3.6V, I_{OUT} = 200mA	--	20	--	mΩ
P-Channel Current Limit		I_{LIM_P}	0x16.IPEAK[1:0] = 2'b11	--	6.2	--	A
Under-Voltage Lockout Threshold (Falling)		UVLO_F	PVIN Falling	--	2.3	--	V
UVLO Hysteresis gap		UVLO_Hys		--	0.1	--	V
Oscillator Frequency		f_{OSC}	V_{IN} = 3.6V	--	3	--	MHz
Maximum Duty Cycle				100	--	--	%
Start-Up Time		t_{ST}	V_{OUT} = 1V, from EN going high to 90% of nominal VOUT	--	420	--	μs
VOUT Power Good Threshold (Rising)			Nominal VOUT Ratio	--	90	--	%
Power Conversion Efficiency			5V to 2.8V and Load = 1.5A	--	90	--	%
			5V to 1V and Load = 1.5A	--	82	--	
Line Regulation				--	0.25	--	%/V
Load Regulation				--	0.25	--	%/A
Load Transient Drop			5V to 2.8V and Load Current step 1.5A in 10μs Rising Time	--	50	--	mV
Output Discharge Resistor		R_{OD}	EN = GND, V_{OUT} = 2.8V	--	40	--	Ω
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C
EN, VSEL Pull Low Current				--	1	--	μA
EN, VSEL Input Voltage	Logic-High			1.05	--	--	V
	Logic-Low			--	--	0.4	

I²C for Fast Mode

(AVDD = 3.6V, T_A = 25°C, unless otherwise specification)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SDA, SCL Input Voltage	High-Level			1.2	--	--	V
	Low-Level			--	--	0.4	
Fast Mode							
SCL Clock Rate		f_{SCL}		--	--	400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated		$t_{HD;STA}$		0.6	--	--	μs
LOW Period of the SCL Clock		t_{LOW}		1.3	--	--	μs
HIGH Period of the SCL Clock		t_{HIGH}		0.6	--	--	μs
Set-Up Time for a Repeated START Condition		$t_{SU;STA}$		0.6	--	--	μs
Data Hold Time		$t_{HD;DAT}$		0	--	0.9	μs
Data Set-Up Time		$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition		$t_{SU;STO}$		0.6	--	--	μs
Bus Free Time between a STOP and START Condition		t_{BUF}		1.3	--	--	μs
Rising Time of both SDA and SCL Signals		t_r		20	--	300	ns
Falling Time of both SDA and SCL Signals		t_f		20	--	300	ns
SDA and SCL Output Low Sink Current		I_{OL}	SDA or SCL Voltage = 0.4V	2	--	--	mA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

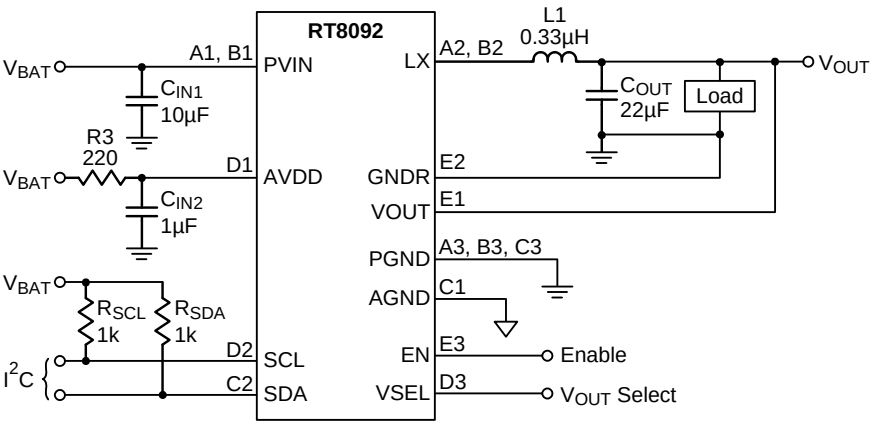


Figure 1. Typical Application Circuit for I²C Control for CSP Package

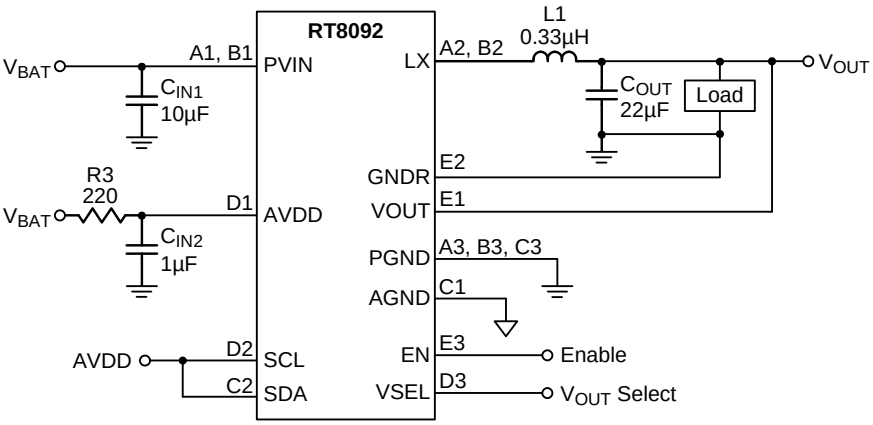


Figure 2. Typical Application Circuit for Internal Resistor Control without I²C for CSP Package

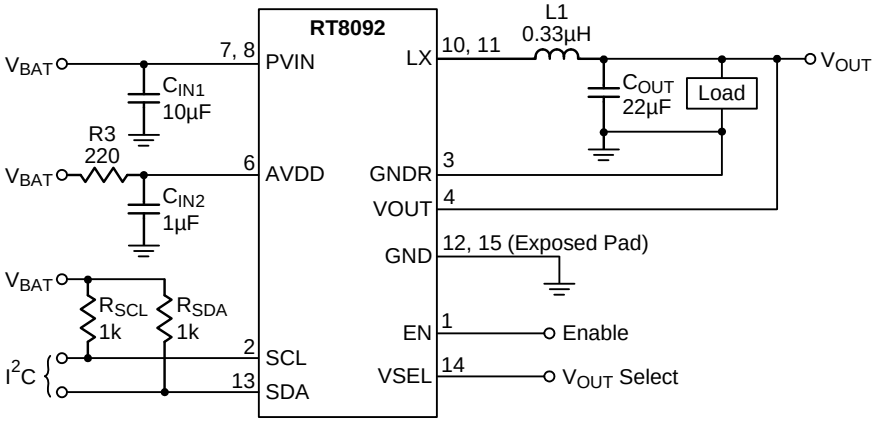


Figure 3. Typical Application Circuit for I²C Control for WQFN Package

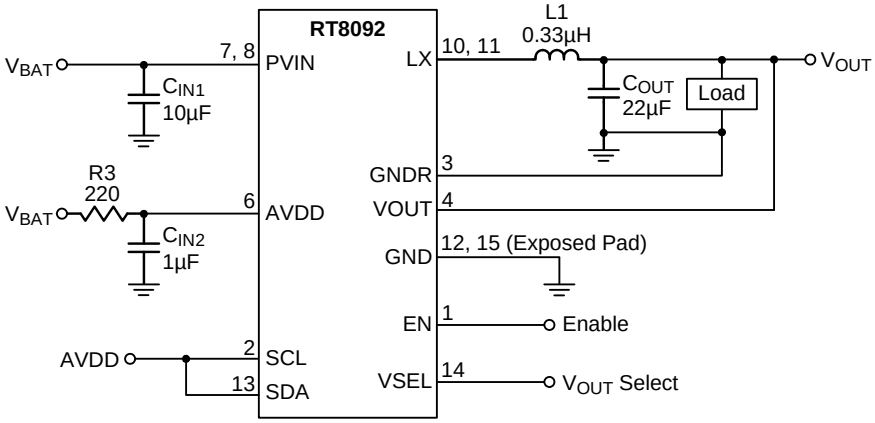
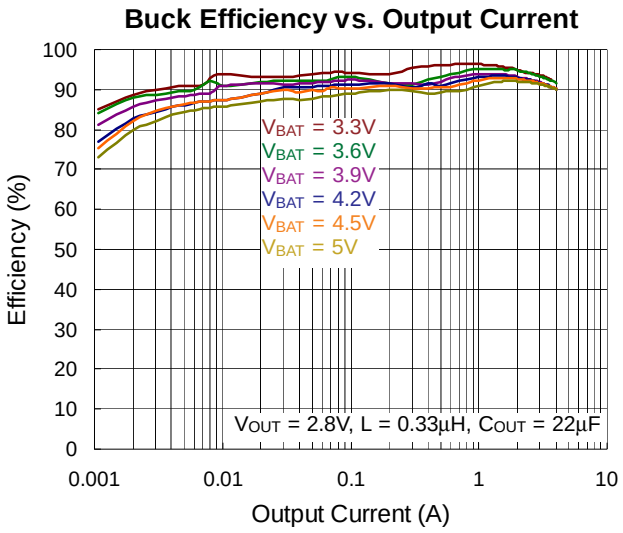
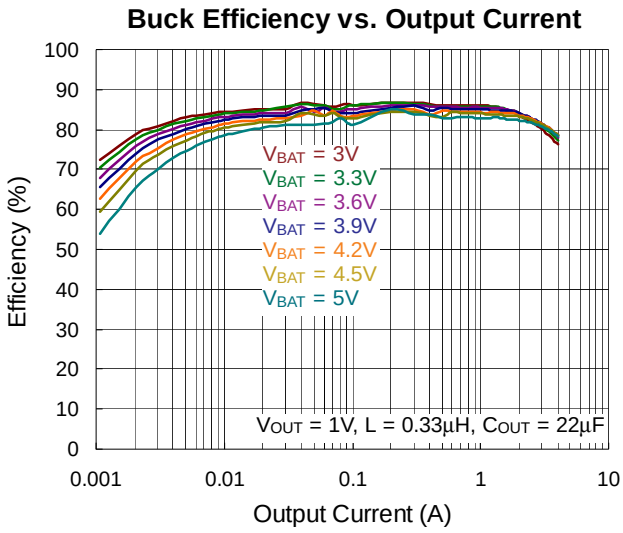
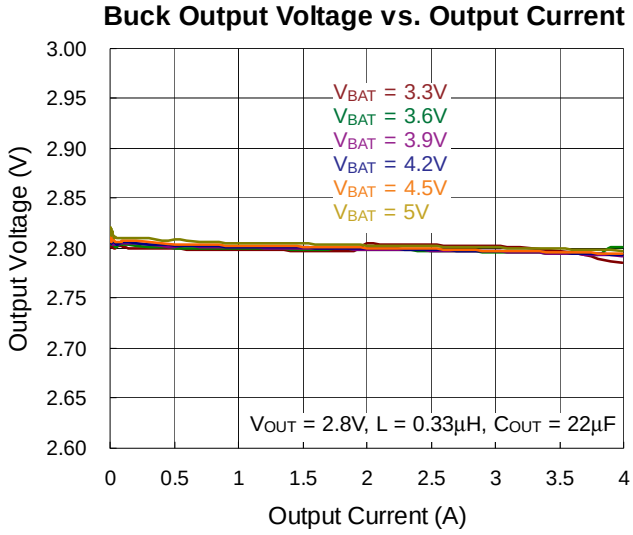


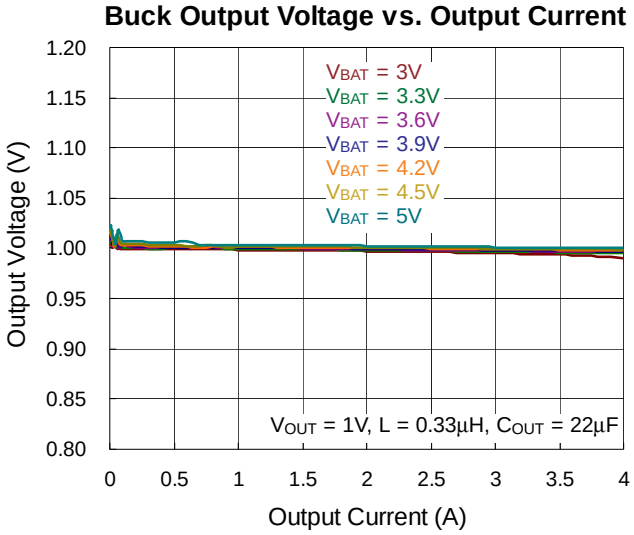
Figure 4. Typical Application Circuit for Internal Resistor Control without I²C for WQFN Package

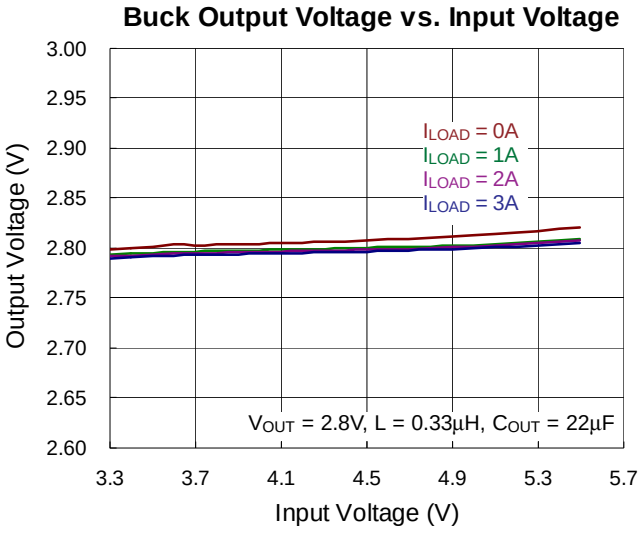
Typical Operating Characteristics

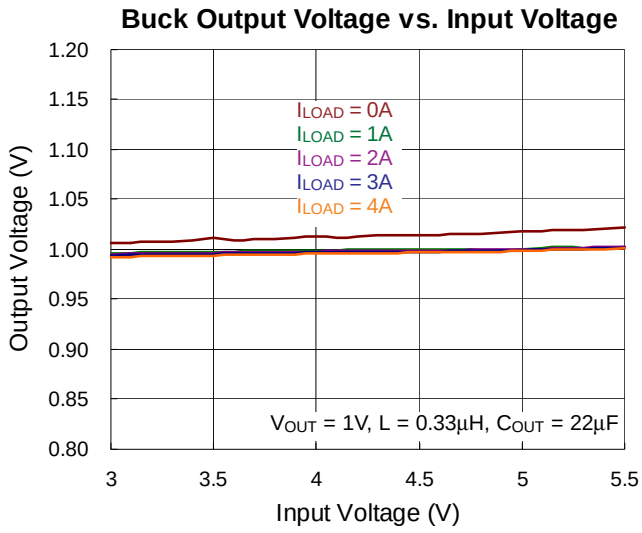




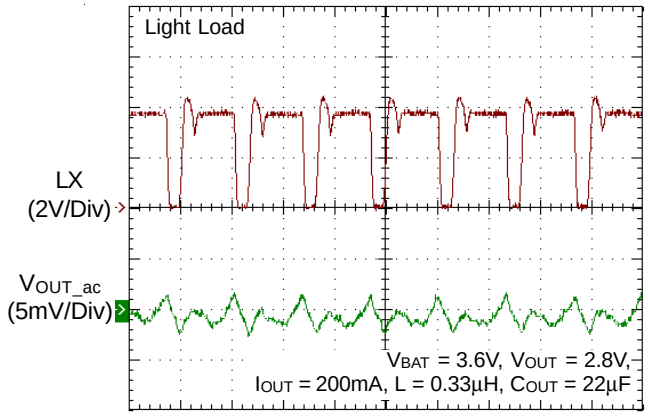




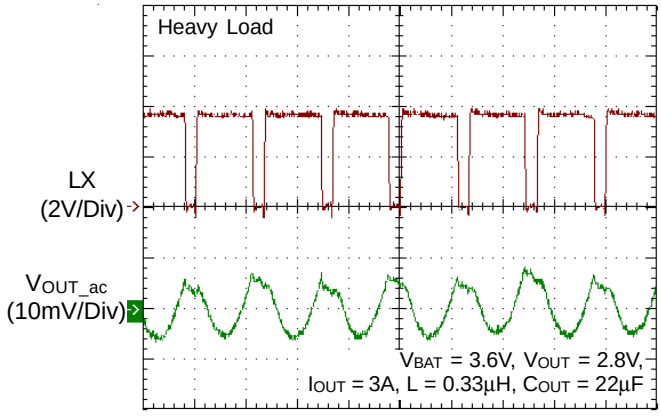




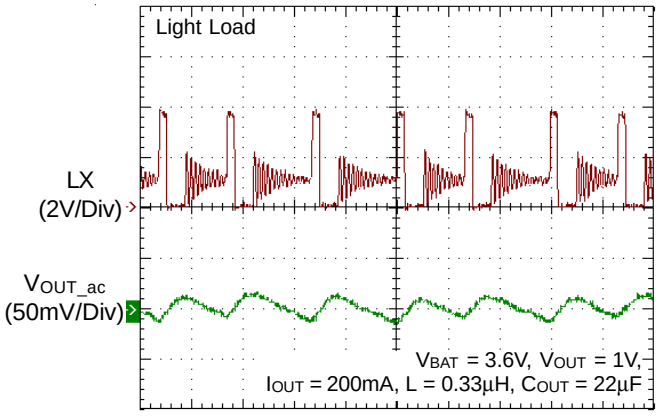
Buck Output Voltage Ripple



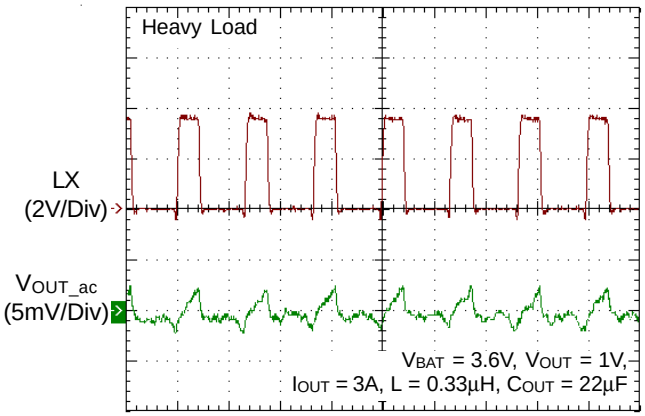
Buck Output Voltage Ripple



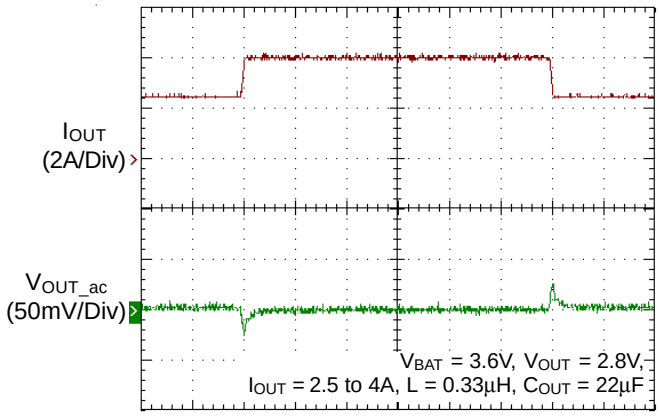
Buck Output Voltage Ripple



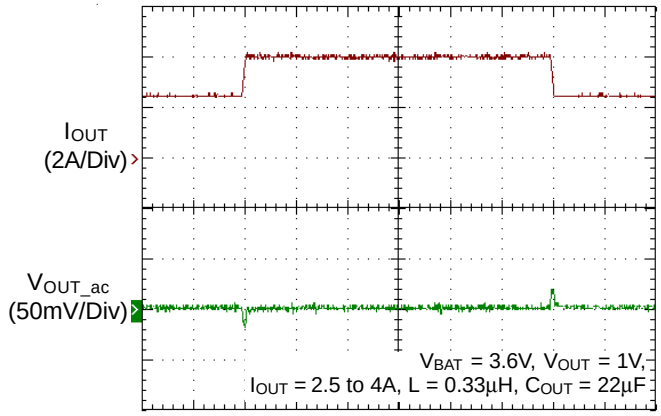
Buck Output Voltage Ripple



Buck Load Transient Response



Buck Load Transient Response



Application Information

The basic RT8092 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Inductor Selection

The inductor value and operating frequency determine the current ripple according to a specific input and output voltage. The ripple current, ΔI_L, increases with higher V_{IN} and decreases with higher inductance, as shown in equation below :

$$\Delta I_L = \frac{1}{f} \times \frac{V_{OUT}}{V_{IN}} \times \frac{V_{IN} - V_{OUT}}{L}$$

where f is the switch frequency and L is the inductance.

Having a lower ripple current reduces not only the ESR losses in the output capacitors, but also the output voltage ripple. Higher operating frequency combined with smaller ripple current is necessary to achieve high efficiency. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified $\Delta I_{L(MAX)}$, the inductor value should be chosen according to the following equation :

$$L = \frac{1}{f} \times \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{\Delta I_{L(MAX)}}$$

The inductor's current rating (defined by a temperature rise from 25°C ambient to 40°C) should be greater than the maximum load current and its saturation current should be greater than the short-circuit peak current limit. Refer to Table 1 for the suggested inductor selection.

Table 1. Suggested Inductors for Typical Application Circuit

Inductor Value	Component Supplier / Part Number	Dimensions (LxWxH mm)	I_{SAT}(L-30%) / DCR
0.33µH	Coilcraft / XFL4015-331	4.0x4.0x1.5	7A / 6.8mΩ
0.47µH	Coilcraft / XFL4015-471	4.0x4.0x1.5	5.4A / 7.6mΩ
0.47µH	SUMIDA / CDMCDS-R47MC	2.5x2.0x1.2	4.8A / 15.0 mΩ
0.47µH	TDK / TFM252010G	2.5x2.0x1.0	4.5A / 24.0mΩ

Input and Output Capacitor Selection

An input capacitor, C_{IN}, is needed to filter out the trapezoidal current at the source of the high-side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)} / 2$. This simple worst-case condition is commonly used for design. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.

The selection of C_{OUT} is determined by the required ESR to minimize output voltage ripple. Moreover, the amount

of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output voltage ripple, V_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right]$$

where f_{OSC} is the switching frequency and I_L is the inductor ripple current.

The output voltage ripple will be the highest at the maximum input voltage since I_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing. Nevertheless, high value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

VSEL Function Selection

Figure 5 shows the detailed logic of VSEL function. There are several parameters can be set its initial condition, such as output voltage, operation mode (Auto PSM/PWM or Forced-PWM) and output voltage bank. Users can set separately into VSEL high state and VSEL low state to design the required performance.

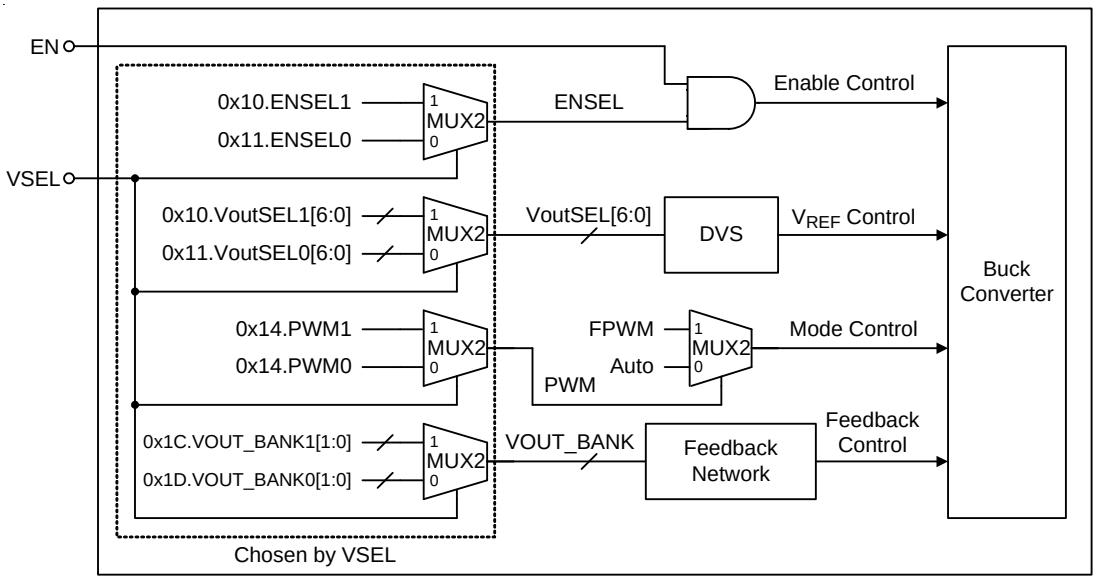


Figure 5. VSEL Logic

Setting the Output Voltage with Internal Feedback Network

Besides defined initial output voltages in VSEL high and VSEL low, the RT8092 can manually change voltage reference from 0.3V to 0.7V by I^2C programming. The difference among bank0 to bank3 is internal feedback configuration. Then the output voltage can be designed as following equation :

$$V_{OUT} = V_{REF} \times 2^{(BANK)}$$

where V_{REF} stand for reference voltage; BANK is 0 to 3, for bank0 to bank3 separately.

The Flow Chart from Power-ON to Soft-Start

To summarize the above functions and judgments such as VSEL function, internal feedback network selection at power-on state, following chart shows the actions and protections to clarify the time sequence and priority.

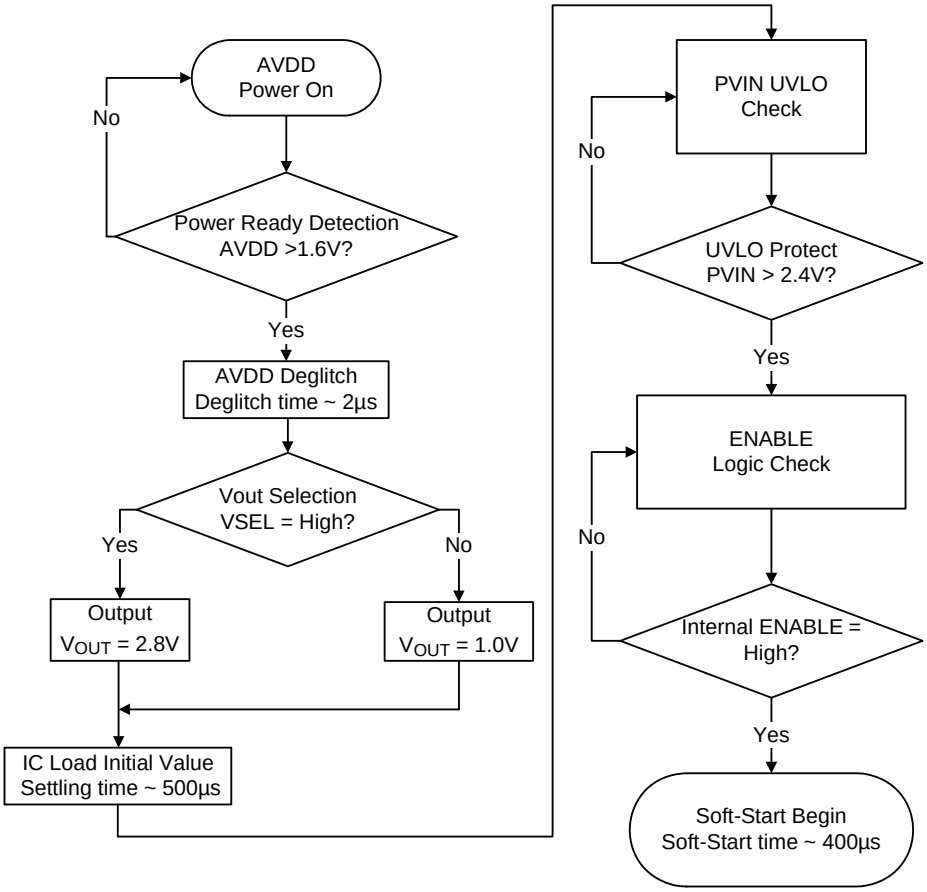
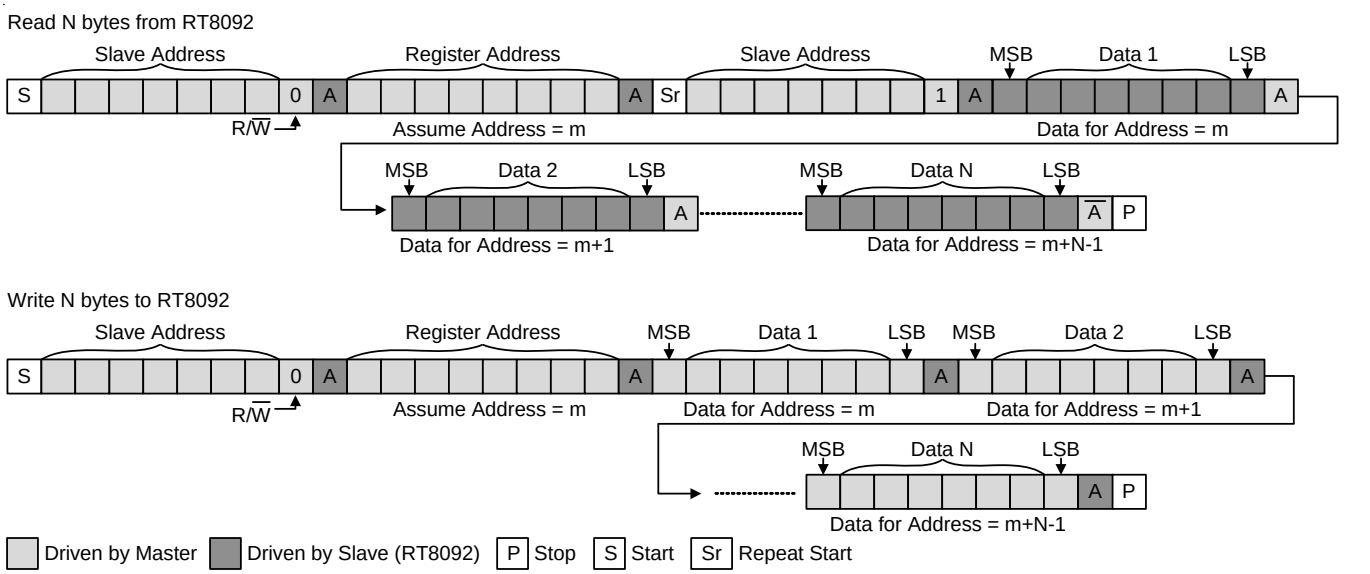


Figure 6. Flow chart of power-on state

I²C Interface

The RT8092 default I²C slave address = 7'b0011100. I²C interface support fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



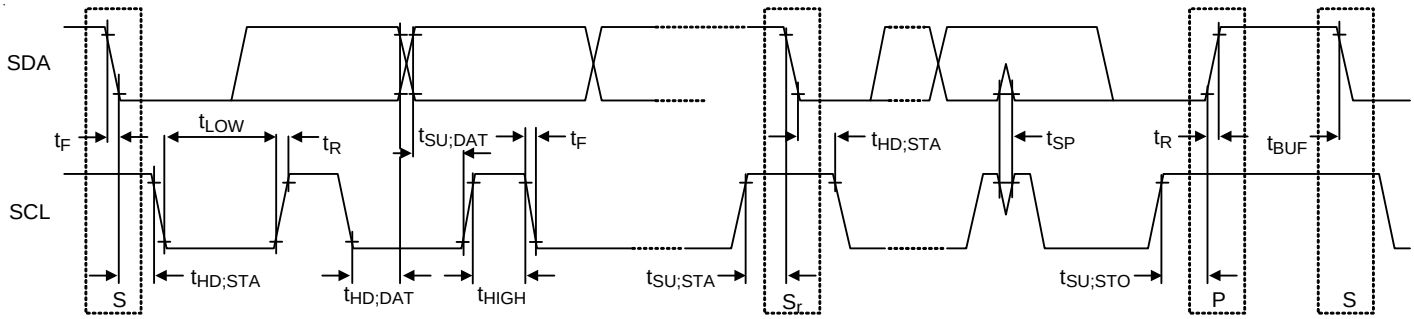


Figure 7. Definition of Timing for Hs-mode Devices on the I²C-bus

I²C Register Map

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x01	Meaning	SEN_TSD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SEN_PG
	Default	0	x	x	x	x	x	x	0
	Read/Write	R							R

SEN_TSD	Report junction temperature > thermal shutdown threshold.
	0 : T_J < 150°C
	1 : T_J > 150°C
SEN_PG	Report V_{OUT} Power GOOD or not.
	0 : V_{OUT} < 90% of target.
	1 : V_{OUT} is within nominal range.

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x10	Meaning	ENSEL1	VoutSEL1[6:0]						
	Default	1	1	1	1	1	1	1	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ENSEL1	When VSEL = High, it is used to gate the EN pin of the step-down converter. This makes the step-down converter can enable/disable by I²C and Software. When EN pin = High and this bit = 1, step-down converter can be enabled. Otherwise, step-down converter would be disabled.
	0 : Disable (even if EN=High, step-down converter still cannot be enabled.)
	1 : Enable
VoutSEL1[6:0]	When VSEL = High, it is used to set Vout voltage level. Vout voltage level = (303.125mV + 3.125mV x VoutSEL1[6:0]) x 2 ^ (0x1C.VOUT_BANK1 [1:0])

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x11	Meaning	ENSEL0	VoutSEL0[6:0]						
	Default	1	0	1	1	1	1	1	1
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ENSEL0	When VSEL = Low, it is used to gate the EN pin of the step-down converter. This makes the step-down converter can enable/disable by I²C and Software. When EN pin = High and this bit = 1, step-down converter can be enabled. Otherwise, step-down converter would be disabled.
	0 : Disable (even if EN=High, step-down converter still cannot be enabled.)
	1 : Enable
VoutSEL0[6:0]	When VSEL = Low, it is used to set Vout voltage level. Vout voltage level = (303.125mV + 3.125mV x VoutSEL0[6:0]) x 2 ^ (0x1D.VOUT_BANK0 [1:0])

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x12	Meaning	Reserved	Reserved	Reserved	Discharge	Reserved	Reserved	Reserved	Reserved
	Default	x	x	x	1	x	x	x	x
	Read/Write				R/W				
Discharge	Control the enabling of the LX discharge path when step-down converter is turned off.								
	0 : Disable discharge path.								
	1 : Enable discharge path.								
	Note. If there is a standby power at VOUT pin, it is suggest to disable this function.								

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x14	Meaning	PWM0	PWM1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Default	0	0	x	x	x	x	x	x
	Read/Write	R/W	R/W						
PWM0	When VSEL = Low, it is used to control PWM operation mode of step-down converter								
	0 : step-down converter would automatically switch the operation mode among CCM (forced PWM), DCM, and PSM.								
	1 : step-down converter works only at the forced PWM.								
PWM1	When VSEL = High, it is used to control PWM operation mode of step-down converter								
	0 : step-down converter would automatically switch the operation mode among CCM (forced PWM), DCM, and PSM.								
	1 : step-down converter works only at the forced PWM.								

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x16	Meaning	IPEAK[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Default	1	1	x	x	x	x	x	x
	Read/Write	R/W	R/W						
IPEAK[1:0]	Set inductor peak current limit.								
	00 : 4.7A								
	01 : 5.2A								
	10 : 5.7A								
	11 : 6.2A								

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x18	Meaning	OCP	Reserved	Reserved	SCP	Reserved	Reserved	PVIN_ UVLO	Reserved
	Default	0	x	x	0	x	x	0	x
	Read/Write	R/W			R/W			R/W	
OCP		Record the Over-current protection event.							
		0 : Over-current protection is not triggered							
		1 : Over-current protection is triggered							
SCP		Record the Vout short-circuit protection event.							
		0 : Vout short-circuit protection is not triggered							
		1 : Vout short-circuit protection is triggered							
PVIN_UVLO		Record the PVIN under voltage event after enabling.							
		0 : PVIN UVLO occurs is not triggered							
		1 : PVIN UVLO occurs is triggered							

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x19	Meaning	Reserved	Reserved	Reserved	Reserved	LPM	Reserved	Reserved	Reserved
	Default	x	x	x	x	0	x	x	x
	Read/Write					R/W			
LPM		Set step-down converter in normal switching mode or low power mode							
		0 : Normal switching mode. (I_Q is larger but transient response is better.)							
		1 : step-down converter works at low power mode (In PFM only.)							

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x1C	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VOUT_BANK1[1:0]	
	Default	x	x	x	x	x	x	1	0
	Read/Write							R/W	R/W
VOUT_BANK1[1:0]		When VSEL = High. It is used to select the Vout list. It should be set before enabling the step-down converter.							
		00 : 0.303125V to 0.7V							
		01 : 0.60625V to 1.4V							
		10 : 1.2125V to 2.8V							
		11 : 2.425V to 5.6V							

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x1D	Meaning	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VOUT_BANK0[1:0]	
	Default	x	x	x	x	x	x	0	1
	Read/Write							R/W	R/W
VOUT_BANK0[1:0]		When VSEL = Low. It is used to select the Vout list. It should be set before enabling the step-down converter.							
		00 : 0.303125V to 0.7V							
		01 : 0.60625V to 1.4V							
		10 : 1.2125V to 2.8V							
		11 : 2.425V to 5.6V							

Register Address	Register Address	b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
0x1E	Meaning	Vout_High[3:0]				Vout_Low(3:0]			
	Default	1	1	1	1	0	0	0	0
	Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Vout_High[3:0]		To avoid DVS change Vout out of reliable range, set the field to limit the effective upper bound of Vout voltage level. When VSEL = Low, if Register 0x11.VoutSEL0[6:0] > {Vout_High[3:0], 3'b111}, effective Vout would be limited to be the voltage corresponding to the code {Vout_High[3:0], 3'b111}. Else effective Vout would follow Register 0x11.VoutSEL0[6:0] setting. When VSEL = High, if Register 0x10.VoutSEL1[6:0] > {Vout_High[3:0], 3'b111}, effective Vout would be limited to be the voltage corresponding to the code {Vout_High[3:0], 3'b111}. Else effective Vout would follow Register 0x10.VoutSEL1[6:0] setting.							
Vout_Low[3:0]		To avoid DVS change Vout out of reliable range, set the field to limit the effective lower bound of Vout voltage level. When VSEL = Low, if Register 0x11.VoutSEL0[6:0] < {Vout_Low[3:0], 3'b000}, effective Vout would be limited to be the voltage corresponding to the code {Vout_Low[3:0], 3'b000}. Else effective Vout would follow Register 0x11.VoutSEL0[6:0] setting. When VSEL = High, if Register 0x10.VoutSEL1[6:0] < {Vout_Low[3:0], 3'b000}, effective Vout would be limited to be the voltage corresponding to the code {Vout_Low[3:0], 3'b000}. Else effective Vout would follow Register 0x10.VoutSEL1[6:0] setting.							

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-15B 1.2x2 (BSC) package, the thermal resistance, θ_{JA}, is 51.9°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WQFN-14L 3.5x3.5 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (51.9°C/W) = 1.92W for WL-CSP-15B 1.2x2 package

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-14L 3.5x3.5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

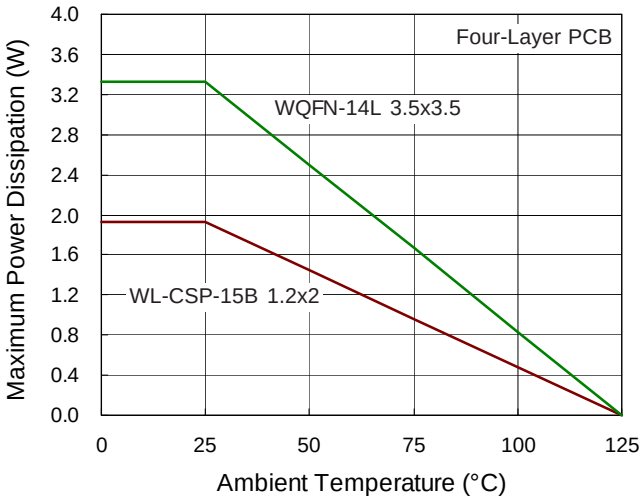


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT8092, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Place the feedback components as close as possible to the VOUT pin and keep these components away from the noisy devices.

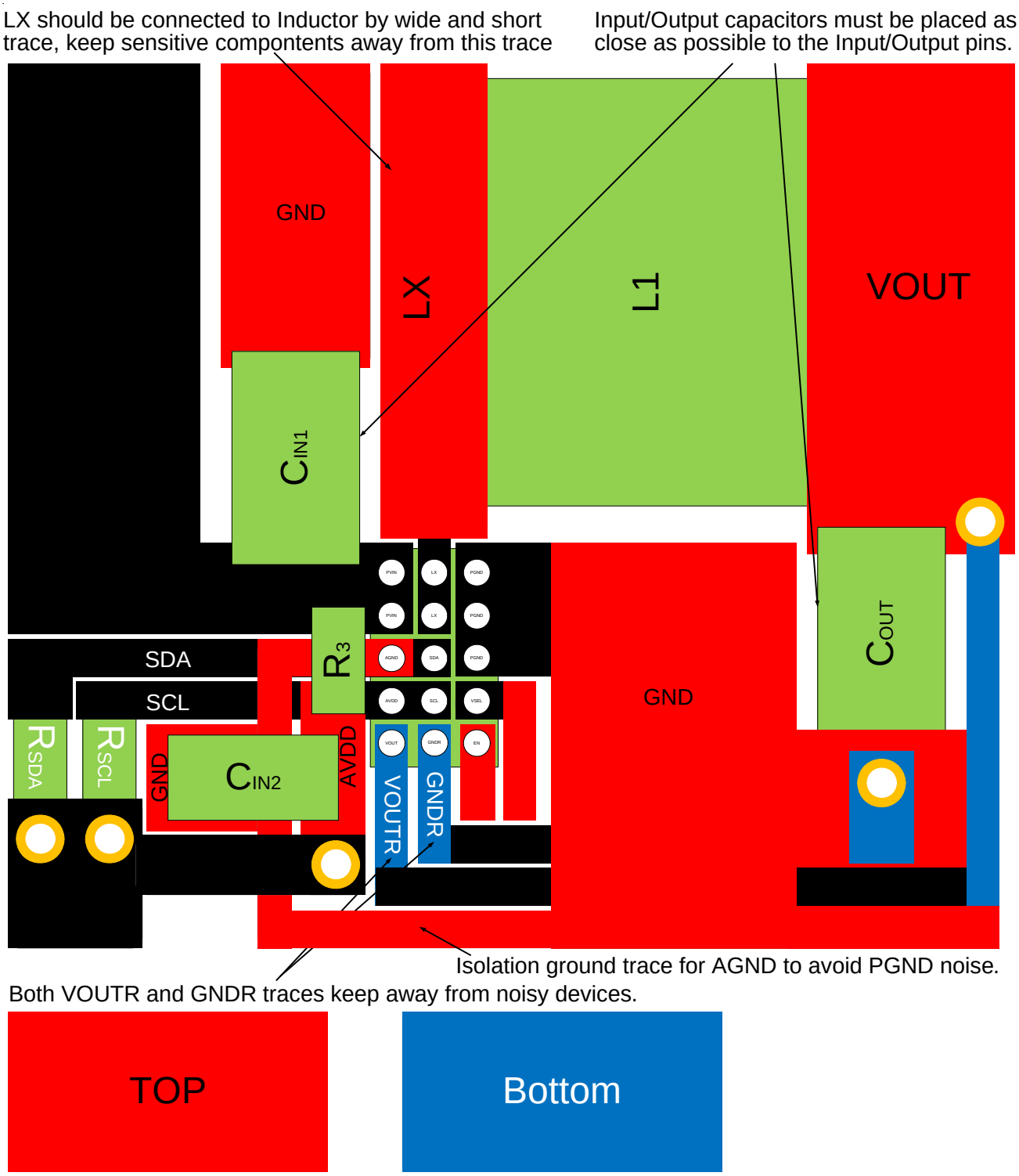


Figure 9. PCB Layout Guide

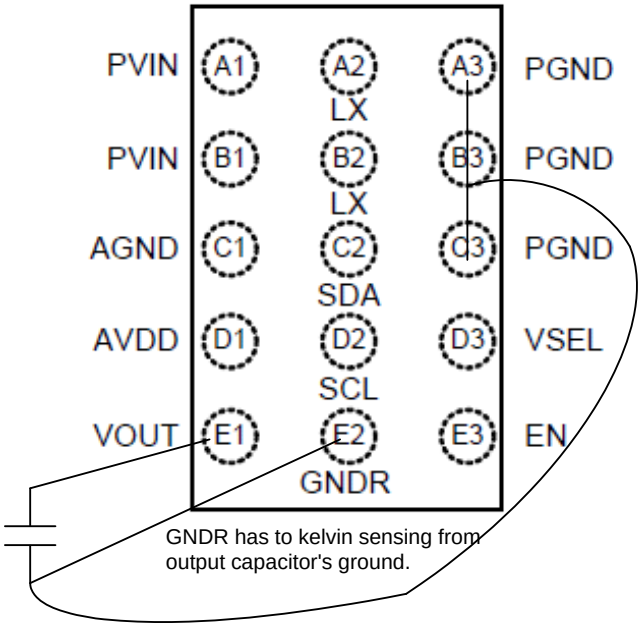
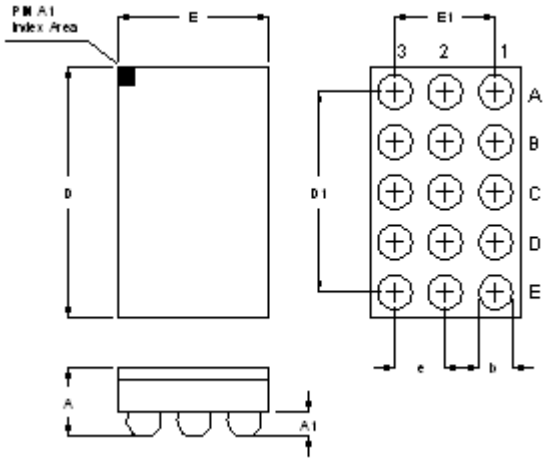


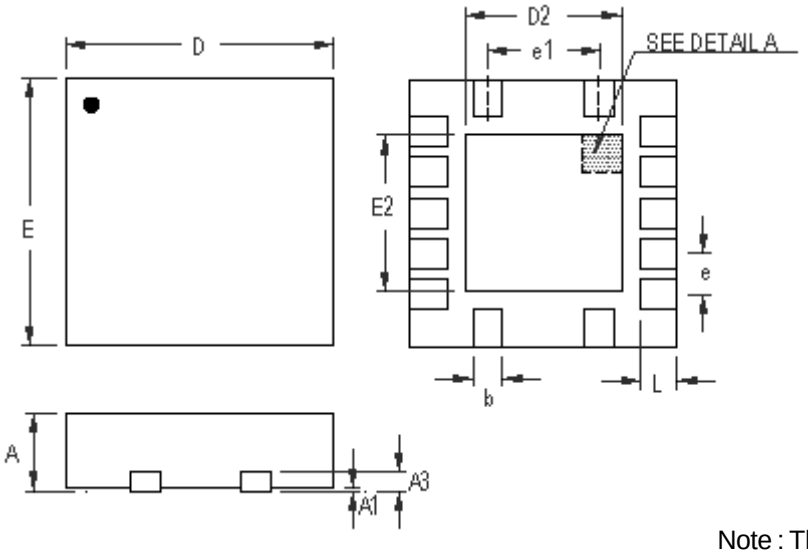
Figure 10. PCB Layout Guide for Critical Path

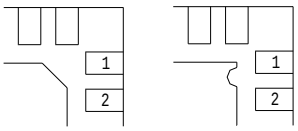
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.950	2.050	0.077	0.081
D1	1.600		0.063	
E	1.150	1.250	0.045	0.049
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.2x2 Package (BSC)





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.400	3.600	0.134	0.142
D2	1.950	2.150	0.077	0.085
E	3.400	3.600	0.134	0.142
E2	1.950	2.150	0.077	0.085
e	0.500		0.020	
e1	1.500		0.060	
L	0.300	0.500	0.012	0.020

W-Type 14L QFN 3.5x3.5 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789