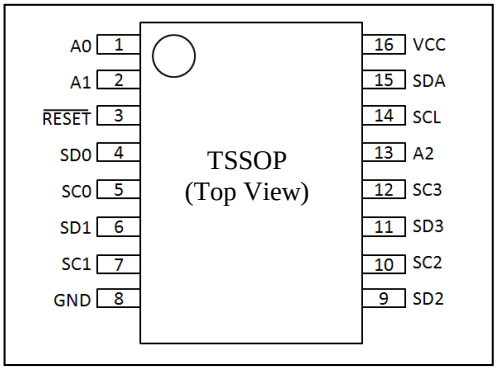
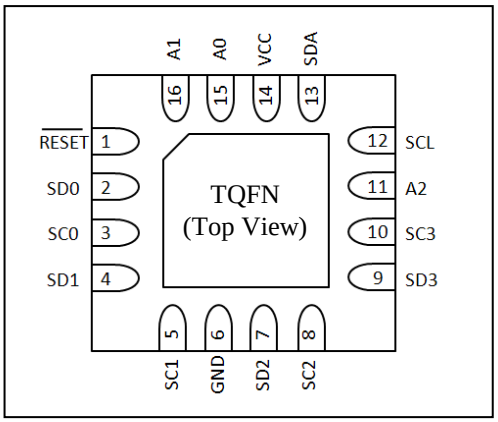
Buffered 4 Channel I2C bus Switch

Features

- 1-of-4 bidirectional translating switches
- Works with I2C-bus (Standard-mode, Fast-mode, and Fast-mode Plus), SMBus, and PMBus
- Operating power supply voltage range of 2.7 V to 5.5 V
- Allows voltage level translation between 3.3 V and 5 V buses
- Active LOW reset input
- 3 address pins allowing up to 8 devices on the I2C-bus
- Each I/O is impedance isolated from all others
- 30 mA static sink capability on all ports
- Allows driving of large loads
- Hysteresis on I/O increases noise immunity
- 5 V tolerant inputs
- 0 Hz to 1MHz clock frequency
- ESD protection exceeds 8000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered:
  TSSOP-16, TQFN4*4-16

Pin Configuration





Description

The PI4MSD5V9646 is designed for 2-wire bus buffering and switching in applications including I2C-bus, SMBus, PMBus, and other systems based on similar principles.

Each of the four outputs may be independently enabled in any combination as determined by the contents of the programmable control register. Each I/O is impedance isolated from all others, thus allowing a total of five branches of 2-wire bus with the maximum specified load (e.g., 5x400 pF for Fm+ I2C-bus at 1 MHz, or 5x4 nF at lower frequencies) .More than one PI4MSD5V9646 may be used in series, providing a substantial fan-out capability.

The PI4MSD5V9646 includes a unidirectional buffer for the clock signal, and a bidirectional buffer for the data signal. The direction of the clock signal may also be set by the contents of the programmable control register. Clock stretching and timing must always be under control of the master device.

The PI4MSD5V9646 has excellent application to 2-wire bus address expansion and increasing of maximum load capacitance. Very large LED displays are a perfect example.

Pin Description

Pin No. (TSSOP)	Pin No. (TQFN)	Pin Name	Type	Description
1	15	A0	I	address input 0
2	16	A1	I	address input 1
3	1	$\overline{\text{RESET}}$	I	active LOW reset input
4	2	SD0	I/O	serial data 0
5	3	SC0	I/O	serial clock 0
6	4	SD1	I/O	serial data 1
7	5	SC1	I/O	serial clock 1
8	6	GND	GND	supply ground
9	7	SD2	I/O	serial data 2
10	8	SC2	I/O	serial clock 2
11	9	SD3	I/O	serial data 3
12	10	SC3	I/O	serial clock 3
13	11	A2	I	address input 2
14	12	SCL	I/O	serial clock line
15	13	SDA	I/O	serial data line
16	14	VCC	VCC	supply voltage

Block Diagram

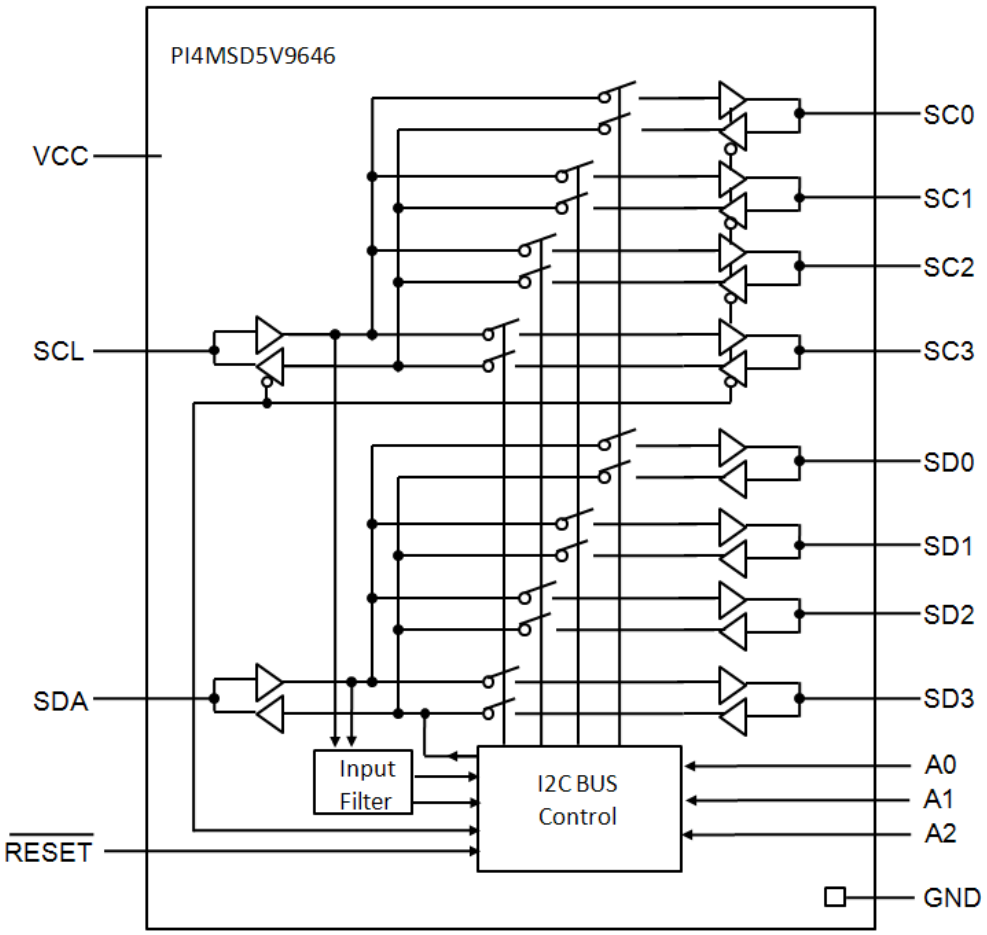


Figure 1: Block Diagram

Maximum Ratings

Storage Temperature .....–55 ℃ to +125 ℃
Supply Voltage port B .....–0.5V to +6.0V
Supply Voltage port A .....–0.5V to +6.0V
DC Input Voltage ..... –0.5V to +6.0V
Control Input Voltage (EN)… ..... –0.5V to +6.0V
Total power dissipation (1).....100mW
Input current(EN,VCCA,VCCB,GND).....50mA
ESD: HBM Mode 8000V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	V_{CCA} Positive DC Supply Voltage	2.7	-	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	-	5.5	V
V_{IO}	I/O Pin Voltage	GND	-	5.5	V
Δt /ΔV	Input transition rise or fall time	-	-	10	ns/V
T_A	Operating Temperature Range	−40	-	+85	℃

DC Electrical Characteristics

Unless otherwise specified, -40°C≤T_A≤85 ℃, 1.1V≤Vcc≤3.6V

Symbol	Parameter	Conditions	VCC	Min.	Typ.	Max.	Unit
Supply							
VCC	Supply Voltage			2.7		5.5	V
ICC	supply current	quiescent; VI (RESET pin) = 0 V	2.7V to 5.5V			1	uA
I2C-bus ports (SCL, SDA, SC[3:0], SD[3:0])							
$V_{I2C-bus}$	I2C-bus voltage	SDx, SCx				5.5	V
V_{IL}	LOW-level input voltage[1]		5.5V			0.5	V
			2.7V			0.4	
V_{IH}	HIGH-level input voltage[1]		5.5V	2.0			V
			2.7V	1.2			V
VI(hys)	hysteresis of input voltage[1]		5.5V	200			mV
			2.7V	80			mV
I_{LI}	input leakage current	pin at VCC or GND	2.7V to 5.5V	-1		+1	uA
$I_{O(sink)}$	output sink current	LOW-level; V_{Sxx} input < VIL	2.7V to 5.5V	30			mA
V_{OL}	LOW-level output voltage	IOL = 30 mA;	5.5V		140	275	mV
		IOL = 30 mA;	2.7V		260	450	mV
Pins SDA, SD0, SD1, SD2, SD3							
Vlock	direction lock voltage[1]		5.5V			3.0	V
			2.7V			1.3	V
Vunlock	direction unlock voltage[1]		5.5V	4.8			V
			2.7V	2.0			V
Reset							
V_{IL}	LOW-level input voltage		5.5V			0.9	V
			2.7V			0.65	V
V_{IH}	HIGH-level input voltage		5.5V	4.8			V
			2.7V	2.0			V
VI(hys)	hysteresis of input voltage		5.5V	200			mV
			2.7V	100			mV
I_{LI}	input leakage current	pin at VCC or GND	2.7V to 5.5V	-1		+1	uA
$t_{w(rst)L}$	LOW-level reset time[2]	VI < VIL			25		ns
trst	reset time	RESET pin; from VI > VIH			250	500	ns
tPOR	power-on reset pulse time	RESET pin; from VI > VIH			250	500	ns
Address inputs A0, A1, A2							
V_{IL}	LOW-level input voltage		2.7V to 5.5V	-0.5		+0.3Vdd	V
V_{IH}	HIGH-level input voltage		2.7V to 5.5V	0.7Vdd		6	V
I_{LI}	input leakage current	pin at VCC or GND	2.7V to 5.5V	-1		+1	uA
Timing characteristics							
td	delay time	RPU = 200 Ω	VCC=5.5V		70		ns
		RPU = 200 Ω	VCC=2.7V		100		ns
tf	fall time	RPU = 200 Ω			16		ns

Note:
[1] Supply voltage dependent; refer to graphs (Figure 7 through Figure 10) for typical trend.
[2] Guaranteed by design, not subject to test.

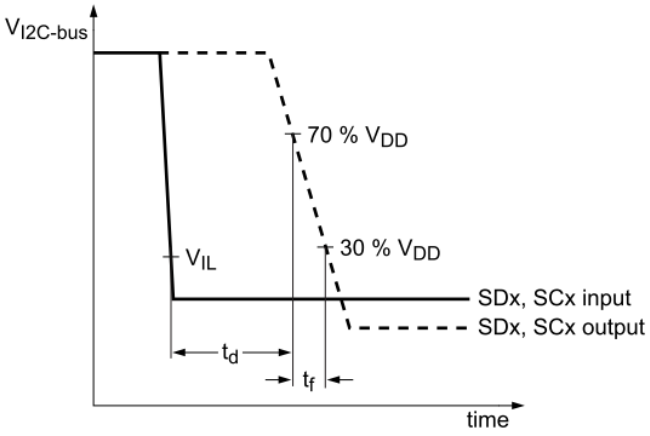


Fig 2 Timing diagram

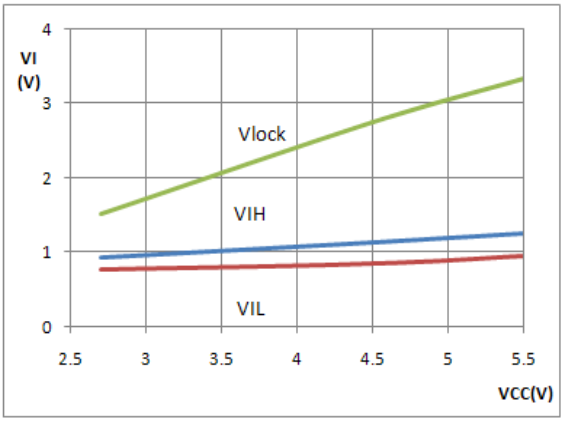


Fig 3 Typical input levels versus supply voltage

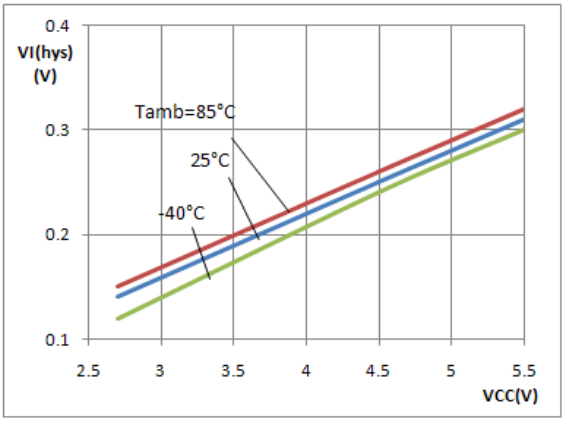


Fig 4 Typical hysteresis versus supply voltage

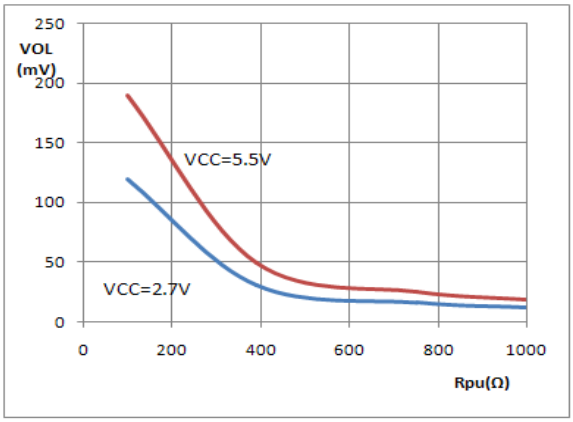


Fig 5 Typical LOW-level output voltage versus pull-up resistance

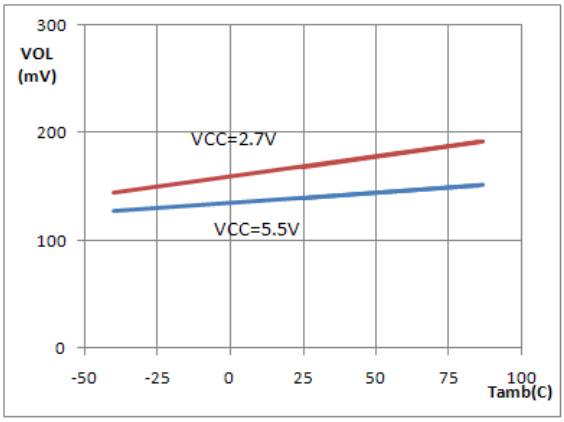


Fig 6 Typical LOW-level output voltage versus ambient temperature

I2C Interface Timing Requirements

Symbol	Parameter	STANDARD MODE I²C BUS		FAST MODE I²C BUS		FAST MODE PLUS I2C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
fscl	I2C clock frequency	0	100	0	400	0	1000	kHz
t_{Low}	I2C clock low time	4.7		1.3		0.5		µs
t_{High}	I2C clock high time	4		0.6		0.26		µs
t_{SP}	I2C spike time		50		50		50	ns
$t_{SU:DAT}$	I2C serial-data setup time	250		100		50		ns
$t_{HD:DAT}$	I2C serial-data hold time	0 (1)		0 (1)		0 (1)		µs
tr	I2C input rise time		1000		300		120	ns
tf	I2C input fall time		300		300		120	ns
t_{BUF}	I2C bus free time between stop and start	4.7		1.3		0.5		µs
$t_{SU:STA}$	I2C start or repeated start condition setup	4.7		0.6		0.26		µs
$t_{HD:STA}$	I2C start or repeated start condition hold	4		0.6		0.26		µs
$t_{SU:STO}$	I2C stop condition setup	4		0.6		0.26		µs
$t_{VD:DAT}$	Valid-data time (high to low) (2) SCL low to SDA output low valid		0.6		0.6		0.3	µs
	Valid-data time (low to high) (2) SCL low to SDA output high valid		1		1		0.45	µs
$t_{VD:ACK}$	Valid-data time of ACK condition ACK signal from SCL low to SDA output		1		1		0.45	µs
Cb	I2C bus capacitive load		400		400		550	pF

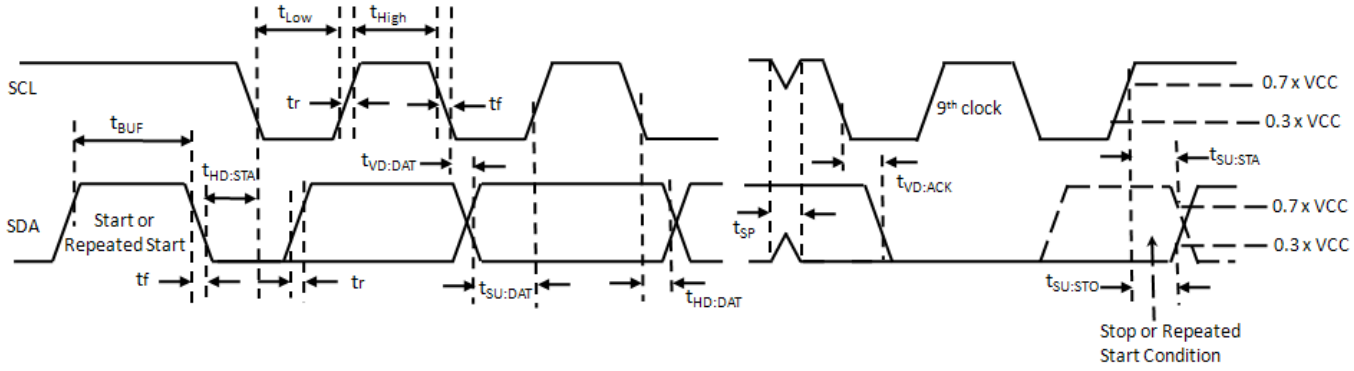


Figure 7. Definition of timing on the I2C-bus

Notes:
[1] A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the VIH min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
[2] Data taken using a 1-kΩ pull-up resistor and 50-pF load Notes

DC supply pins

The power supply voltage for the PI4MSD5V9646 may be any voltage in the range 2.7V to 5.5 V. The IC supply must be common with the supply for the bus. Hysteresis on the ports are a percentage of the IC's power supply, hence noise margin taken into account when selecting an operating voltage.

Clock signal input – SCL

The clock signal buffer is unidirectional, with this pin acting as the default input. However, the clock signal direction may be reversed by setting the MSB of the Control register HIGH. In normal I2C-bus operations the master device generates a unidirectional clock signal to the slave. For lowest cost the PI4MSD5V9646 combines unidirectional buffering of the clock signal with a bidirectional buffer for the data signal. Clock stretching is therefore not supported and slave devices that may require clock stretching must be accommodated by the master adopting an appropriate clocking when communicating with them.

The buffer includes hysteresis to ensure clean switching signals are output, especially with slow rise times on high capacitively loaded buses.

Clock signal outputs- SC0, SC1, SC2, SC3

The clock signal from SCL is buffered through four independent buffers, and the signal is presented at the four SC0 to SC3 ports. Ports are open-drain type and require external pull-up resistors.

When the MSB of the control register is set HIGH, the port direction is reversed. The ANDed result of the selected SC0 to SC3 lines is then used to drive the open-drain output of the SCL pin

Data signal inputs/outputs- SDA, SD0, SD1, SD2, SD3

The data signal buffers are bidirectional. The port (SDA, or any one of SD0 to SD3) which first falls LOW, will decide the direction of this buffer and 'lock out' signals coming from the opposite side. As the 'input' signal continues to fall, it will then drive the open-drain of the 'output' side LOW. Again, hysteresis is applied to the buffer to minimize the effects of noise. Ports are open-drain type and require external pull-up resistors.

At some points during the communication, the data direction will reverse—for example, when the slave transmits an acknowledge (ACK) or responds with its register contents.

During these times, the controlling 'input' side will have to rise to Vunlock before it releases the 'lock', which then allows the 'output' side to gain control, and pull (what was) the 'input' side LOW again. This will cause a 'pulse' on the 'input' side, which can be quite long duration in high capacitance buses. However, this pulse will not interfere with the actual data transmission, as it should not occur during times of clock line transition (during normal I2C-bus and SMBus protocols), and thus data signal set-up time requirements are still met.

Device Address

The slave address of the PI4MSD5V9646 is shown in Figure 8. The address pins (A2, A1, A0) must be driven to a HIGH or LOW level—they are not internally pulled to a default state. The read/write bit must be set LOW to enable a write to the Control register, or HIGH to read from the Control register.

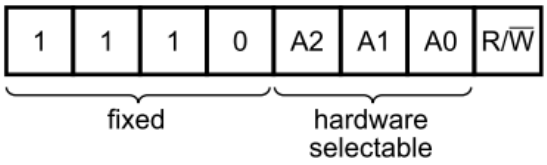


Figure 8:Device address

Control register

The Control register of the PI4MSD5V9646 is shown in Figure 9. Each of the four output channels (SCn/SDn pairs) can be enabled independently, and the direction of the clock signal can be reversed.

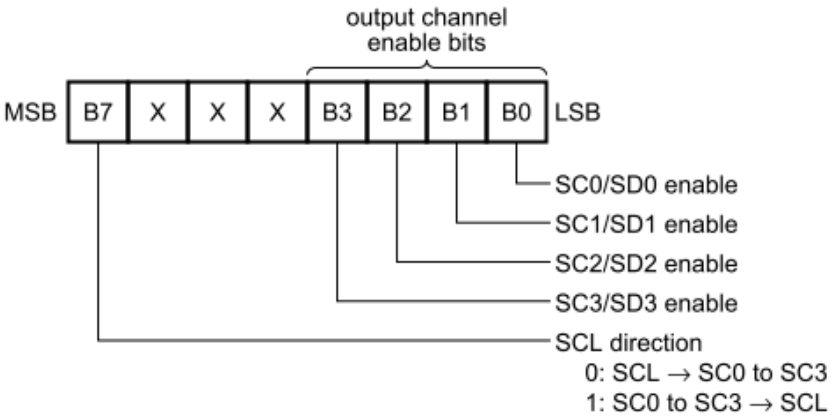


Figure 9: Control register

A LOW or 'zero' bit (B[3:0]) indicates that the respective channel (SC[3:0], SD[3:0]) is disabled. The default reset condition of the register is all zeros, all channels disabled, forward direction. A HIGH or 'one' bit indicates the respective channel is enabled.

Example: B3 = 1, B2 = 0, B1 = 1, B0 = 0 means channel 3 (SC3/SD3) and channel 1 (SC1/SD1) are enabled, and channel 2 (SC2/SD2) and channel 0 (SC0/SD0) are disabled.

As each channel is individually buffered, the loads on each are isolated, and therefore there is no special requirement to keep the sum of the collective capacitances below the maximum bus capacitance. Instead, each line may have up to the maximum bus capacitance and be enabled or disabled without affecting the performance of the other channels.

The Most Significant Bit (MSB) B7 is used to set the direction of the SCL (clock) signal. The default state is LOW (zero). In this state, the SCL port will act as the input, and the IC will supply a buffered signal to any of the four output channels (SC0 to SC3) which are enabled. When B7 is set HIGH (one), the clock signal direction is reversed. The ports SC0 to SC3 act as inputs, the ANDed combination of the selected signals is buffered and output on the SCL pin.

The PI4MSD5V9646 is always addressable from the SCL/SDA side, regardless of the state of B7. Any device which can communicate data to the SCL/SDA pins, either by being directly attached to those pins or by transmitting through the PI4MSD5V9646 (when B7 = 1), may address the device and change the control register's contents. The Control register is only updated upon receipt of the STOP condition

$\overline{\text{RESET}}$ input

The active LOW RESET input is used to disable the buffer, and reset it to its default state. The IC should only be disabled when the bus is idle to avoid truncation of commands which may confuse other devices on the bus.

The RESET signal will clear the contents of the Control register, which has the effect of disabling all output lines SC[0:3] and SD[0:3]. It is the nature of the I2C-bus protocol that devices may become 'stuck'. To help in the clearing of this condition, the PI4MSD5V9646 can be reset, and each port brought on-line successively to find the component holding the bus LOW.

Power-on reset

During power-on, the PI4MSD5V9646 is internally held in the reset condition for a maximum of trst = 500 ns. The default condition after reset is for the Control register to be erased (all zeros), resulting in all output channels being disabled.

Bus transaction

A typical I2C-bus write transaction to the PI4MSD5V9646 is shown in Fig 10. A read transaction is shown in Fig11.

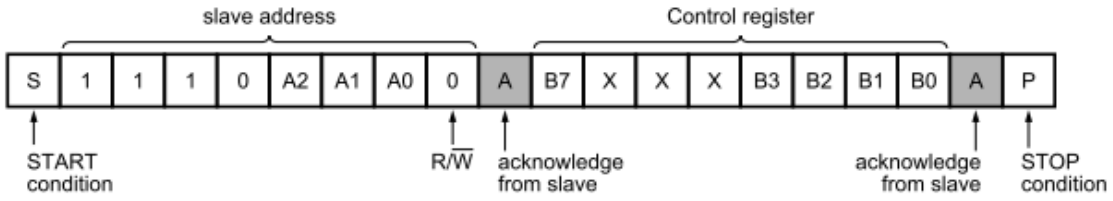


Figure 10: write transaction to Control register

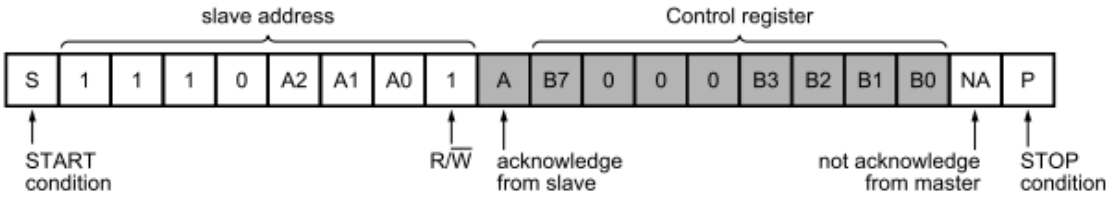


Figure 11: read transaction to Control register

Application

Figure 12 shows a typical application for the PI4MSD5V9646. Each channel can support up to the maximum permissible capacitance load, thus the maximum loading of the system can be 5 times that which could be achieved without buffering.

The channel enable function can be used to interface buses of different operating frequencies. When certain bus sections are enabled, the system frequency may be limited by a bus section having a slave device specified only to 100 kHz. When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow the PI4MSD5V9646 to run in excess of the 1 MHz maximum limit of the I2C-bus Fast-mode Plus (Fm+), or to run a huge 4 nF load at 100 kHz.

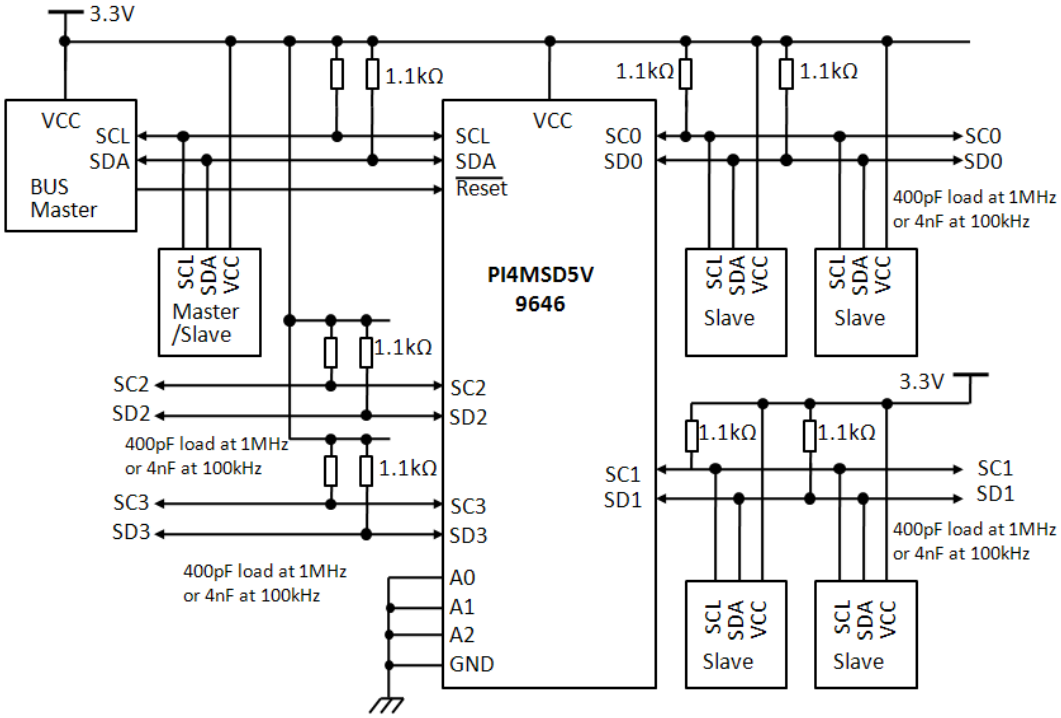


Figure 12. Typical Application of PI4MSD5V9646

Figure 13 shows a level translating application for the PI4MSD5V9646. Per there's VIH limitation of the SCL,SDA and SDX,SCX channel, it's very important to choose the VCC. If VDP1 is lower than VCC, it's better to add a pull-up resistor on the RESET pin , because the VIH of reset pin is close to VCC.

VCC	VDP1	VDP2
3.3V	3.0V-5.5V	3.0V-5.5V
5V	4.5V-5.5V	4.5V-5.5V

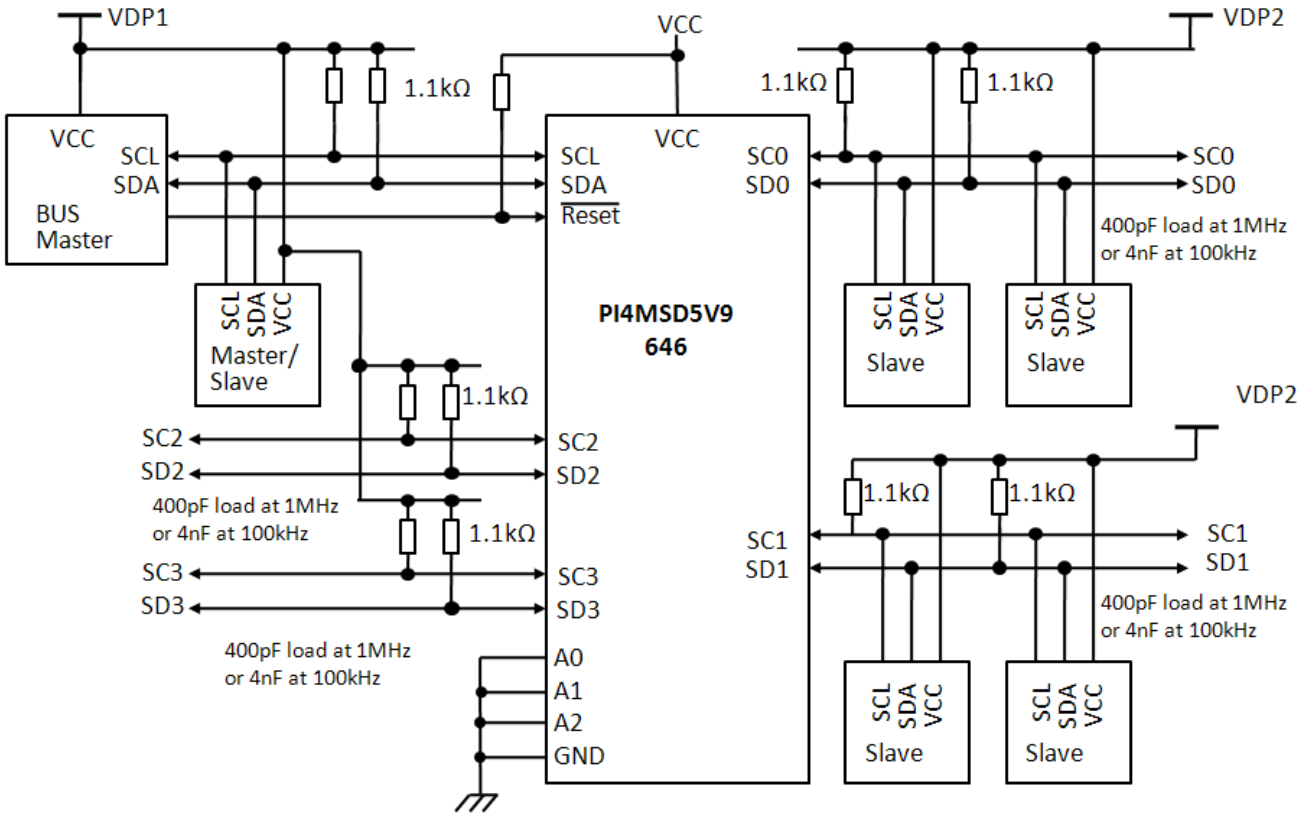


Figure 13. Typical Application of PI4MSD5V9646

Figure 14 shows the PI4MSD5V9646 used as a line driver. Four such lines (only one shown) can be run from the same device. The receiving end may then again be used as a 4-way bus switch, radiating out into another four lines.

Using the address pins, this entire structure may be repeated. Thus a total of eight PI4MSD5V9646 'line drivers' may be connected to a single bus master (U1), allowing for 2 (8 x4) long distance bus pairs to be driven from the one I2C-bus port.

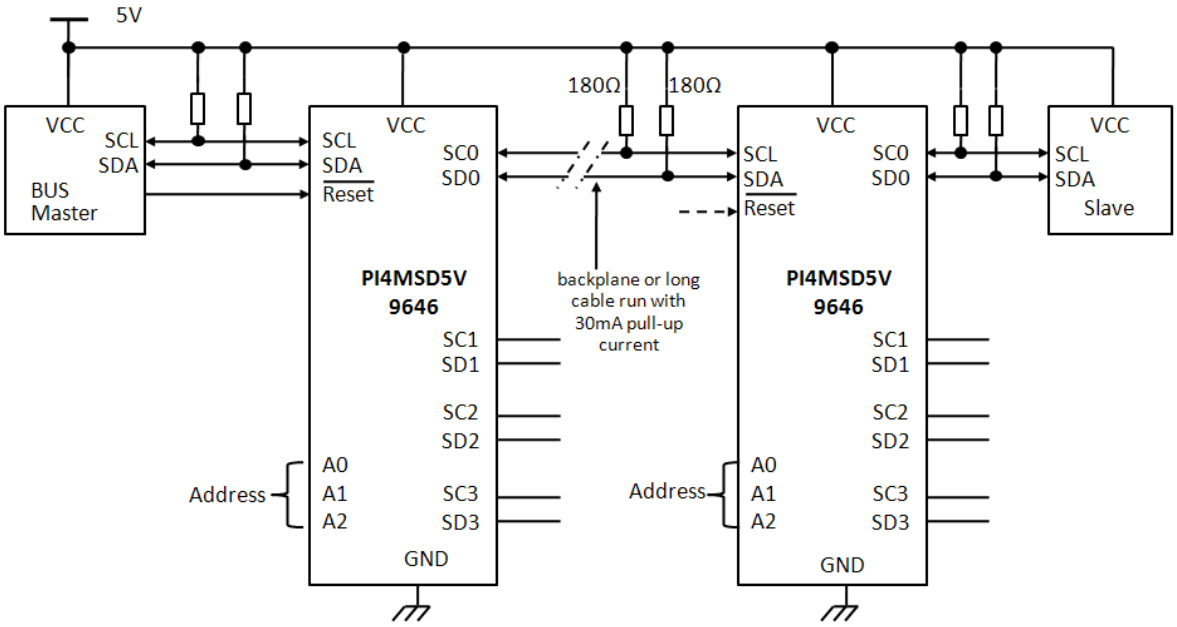
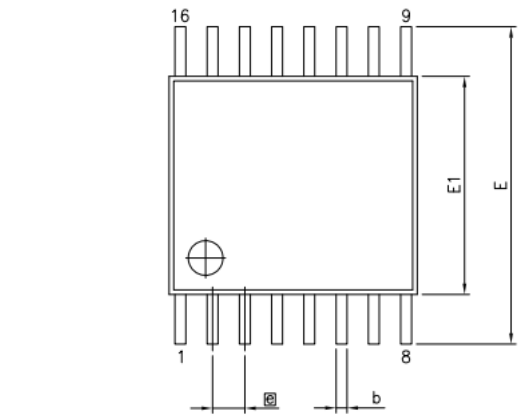
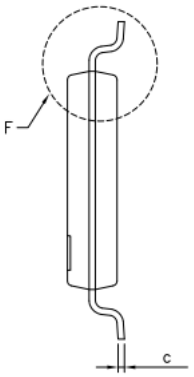


Figure 14. Typical Application of PI4MSD5V9646

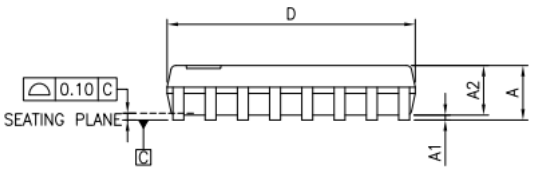
Mechanical Information

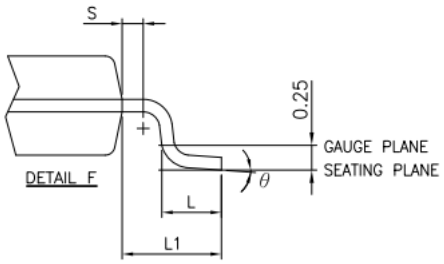
TSSOP-16(L)





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

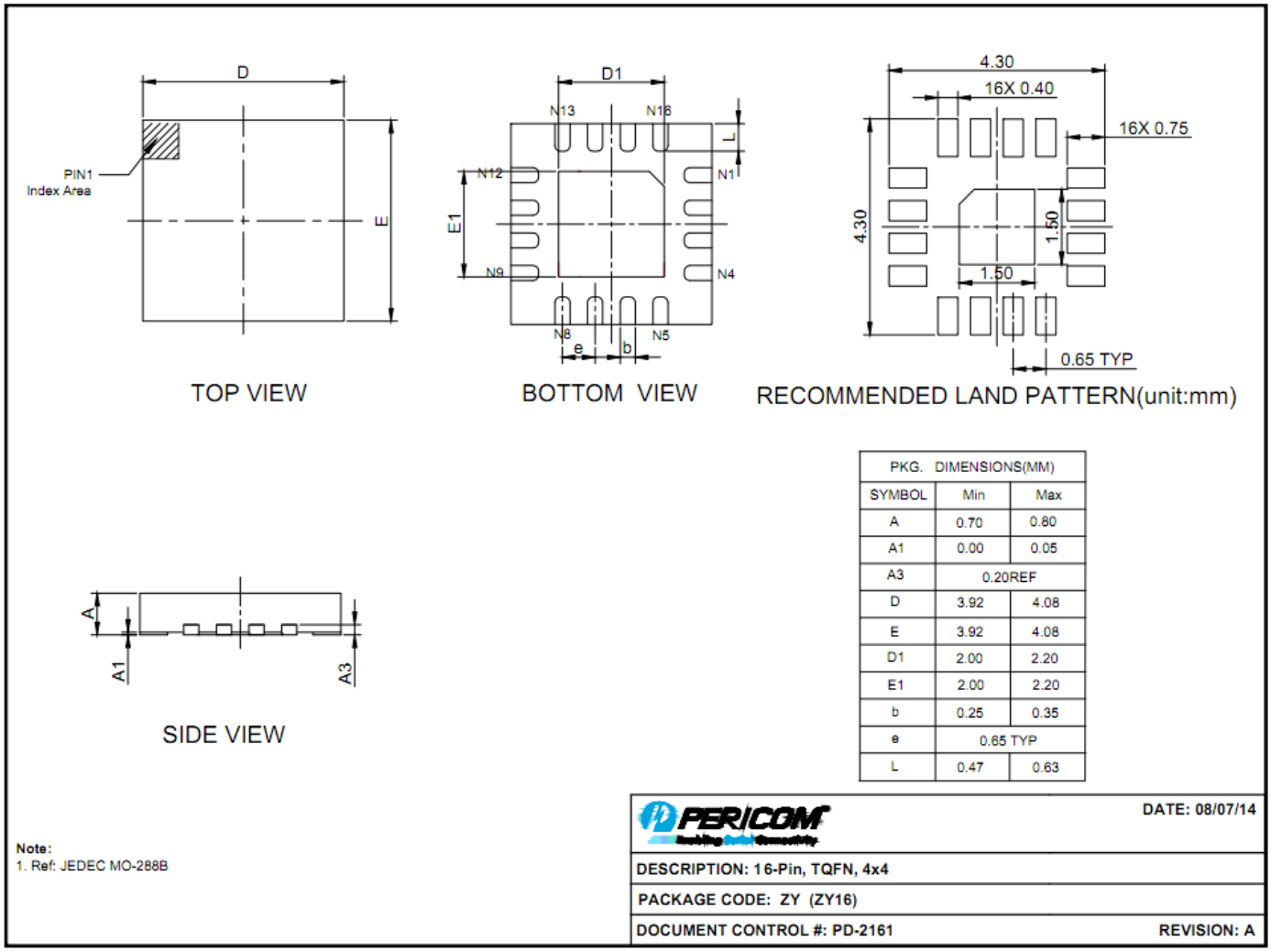
PERICOM Enabling Serial Connectivity — DATE: 03/24/16

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310 — REVISION: G

TQFN4*4-16(ZY)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20REF	
D	3.92	4.08
E	3.92	4.08
D1	2.00	2.20
E1	2.00	2.20
b	0.25	0.35
e	0.65 TYP	
L	0.47	0.63

Note:
1. Ref: JEDEC MO-288B

DATE: 08/07/14

DESCRIPTION: 16-Pin, TQFN, 4x4

PACKAGE CODE: ZY (ZY16)

DOCUMENT CONTROL #: PD-2161 REVISION: A

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Number	Package Code	Package
PI4MSD5V9646LE	L	16-Pin,173 mil Wide (TSSOP)
PI4MSD5V9646LEX	L	16-Pin,173 mil Wide (TSSOP), Tape & Reel
PI4MSD5V9646ZYEX	ZY	16-Pin, 4x4 (TQFN), Tape & Reel

Note:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding X Suffix= Tape/Reel