

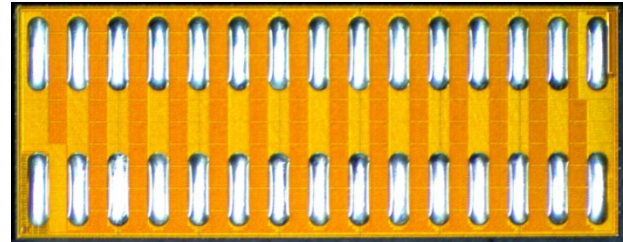
# EPC2023 – Enhancement Mode Power Transistor

## Preliminary Specification Sheet

Status: Engineering

Features:

- $V_{DS}$ , 30 V
- Maximum  $R_{DS(ON)}$ , 1.3 m $\Omega$
- $I_D$ , 60 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2023 eGaN<sup>®</sup> FETs are supplied only in passivated die form with solder bars

Die Size: 6.05 mm x 2.3 mm

Applications:

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- Synchronous Rectification
- Inrush Protection
- Point-of-Load (POL) Converters

### MAXIMUM RATINGS

Parameter	Value
$V_{DS}$ (Maximum Drain – Source Voltage)	30 V
$V_{GS}$ (Gate – Source Maximum Voltage Range)	-4 V < $V_{GS}$ < 6 V
$I_D$ Continuous Drain Current, 25 °C, $\theta_{JA} = 13.5$ )	60 A
$I_D$ (Maximum Pulsed Drain Current, 25 °C, $T_{pulse} = 300 \mu s$ )	590 A
$T_J$ (Optimum Temperature Range)	-40 °C < $T_J$ < 150 °C

### STATIC CHARACTERISTICS

Parameter	Conditions	Value
$I_{DSS}$ (Maximum Drain – Source Leakage)	$V_{DS} = 24 V, V_{GS} = 0 V$	1.0 mA
$R_{DS(ON)}$ (Maximum $R_{DS(ON)}$ )	$V_{GS} = 5 V, I_D = 40 A$	1.3 m $\Omega$
$R_{DS(ON)}$ (Typical $R_{DS(ON)}$ )	$V_{GS} = 5 V, I_D = 40 A$	1 m $\Omega$
$V_{GS(TH)}$ (Gate – Source Threshold Voltage)	$V_{DS} = V_{GS}, I_D = 20 mA$	0.7 V < $V_{GS(TH)}$ < 2.5 V
$I_{GSS}$ (Gate – Source Maximum Positive Leakage)	$V_{GS} = 5 V$	9 mA
$I_{GSS}$ (Gate – Source Maximum Negative Leakage)	$V_{GS} = -4 V$	-1 mA

$T_J = 25 \text{ }^\circ\text{C}$  unless otherwise stated

Specifications are with Substrate shorted to Source where applicable

# EPC2023 – Enhancement Mode Power Transistor Preliminary Specification Sheet



## DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
$C_{ISS}$ (Input Capacitance)	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	2.3 nF
$C_{OSS}$ (Output Capacitance)		1.3 nF
$C_{RSS}$ (Reverse Transfer Capacitance)		56 pF
$R_G$ (Gate Resistance)		0.3 $\Omega$
$Q_G$ (Total Gate Charge)	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$	20 nC
$Q_{GS}$ (Gate to Source Charge)		5.8 nC
$Q_{GD}$ (Gate to Drain Charge)		1.9 nC
$Q_{G(TH)}$ (Gate Charge at Threshold)		3.6 nC
$Q_{OSS}$ (Output Charge)	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	28 nC
$Q_{RR}$ (Source-Drain Recovery Charge)		0

$T_J = 25\text{ }^\circ\text{C}$  unless otherwise stated

Specifications are with Substrate shorted to Source where applicable

## THERMAL CHARACTERISTICS

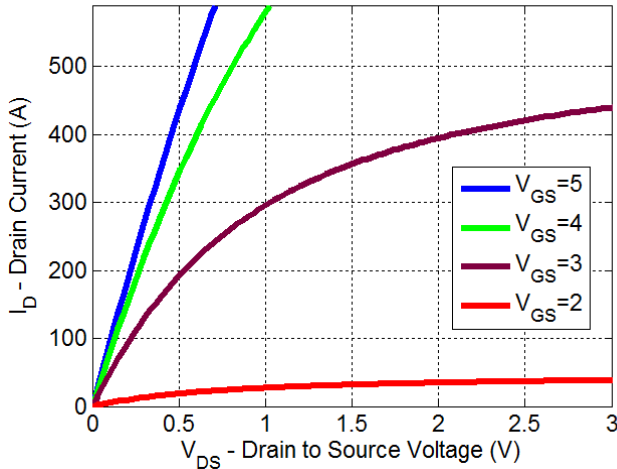
		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	42	$^\circ\text{C/W}$

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

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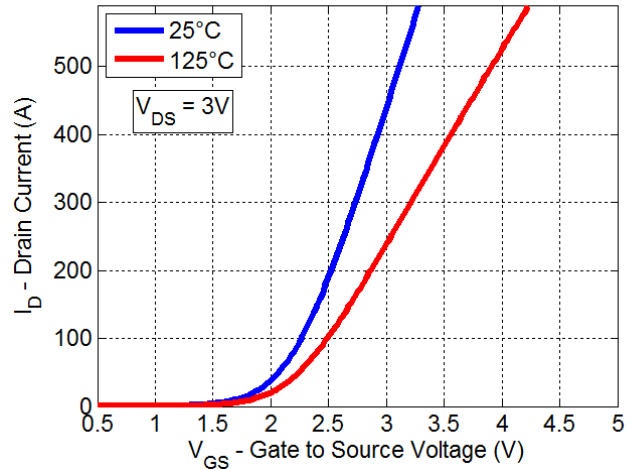
**Figure 1:**

EPC2023: Typical Output Characteristics at 25°C



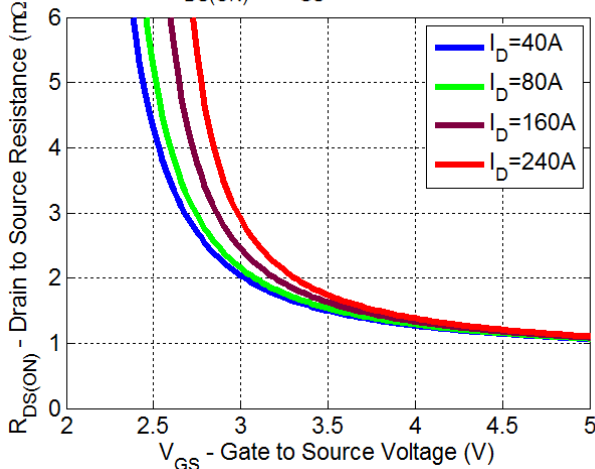
**Figure 2:**

EPC2023: Transfer Characteristics



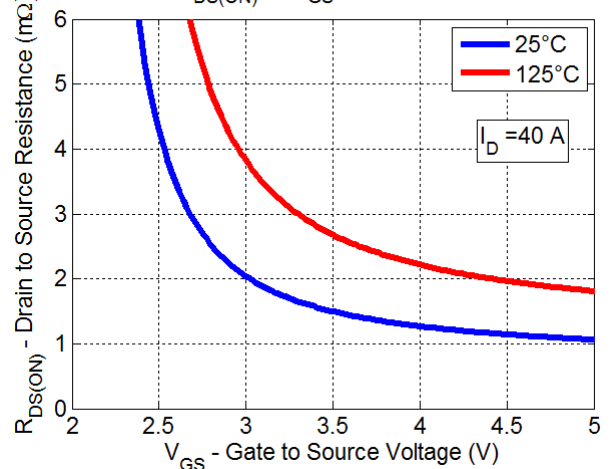
**Figure 3:**

EPC2023:  $R_{DS(ON)}$  vs  $V_{GS}$  for Various Drain Currents



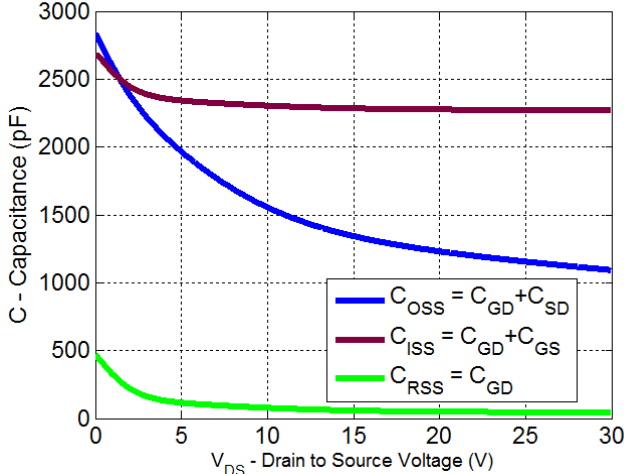
**Figure 4:**

EPC2023:  $R_{DS(ON)}$  vs  $V_{GS}$  for Various Temperatures



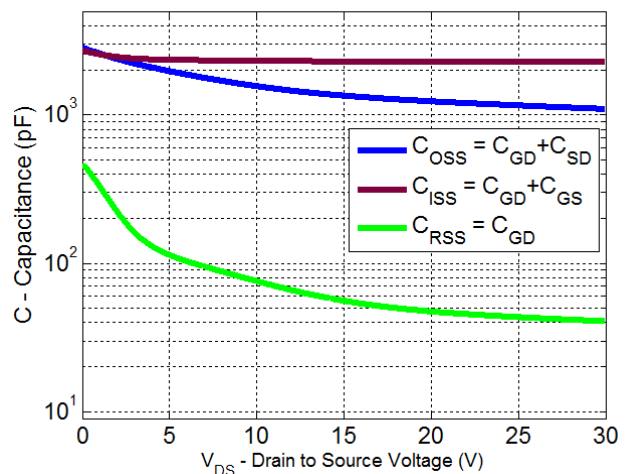
**Figure 5a:**

EPC2023: Capacitance (Linear Scale)



**Figure 5b:**

EPC2023: Capacitance (Log Scale)

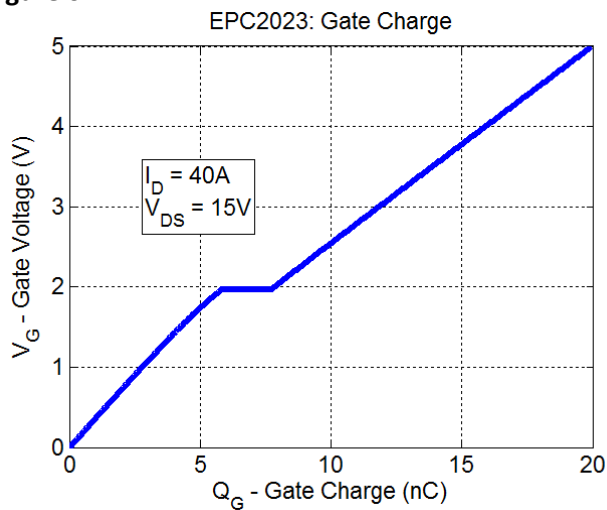


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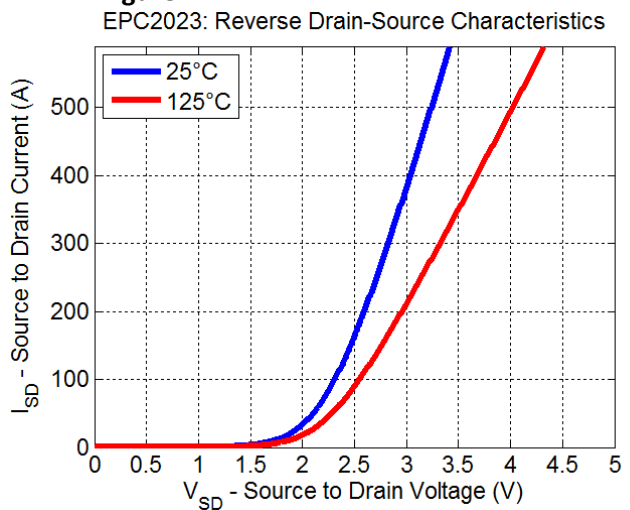
## Preliminary Specification Sheet



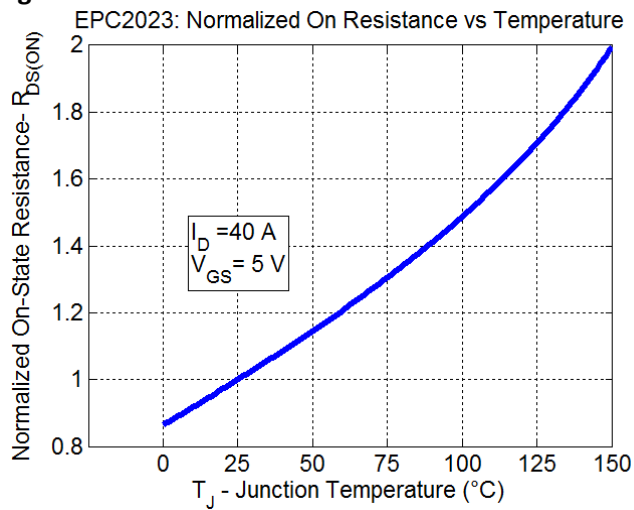
**Figure 6:**



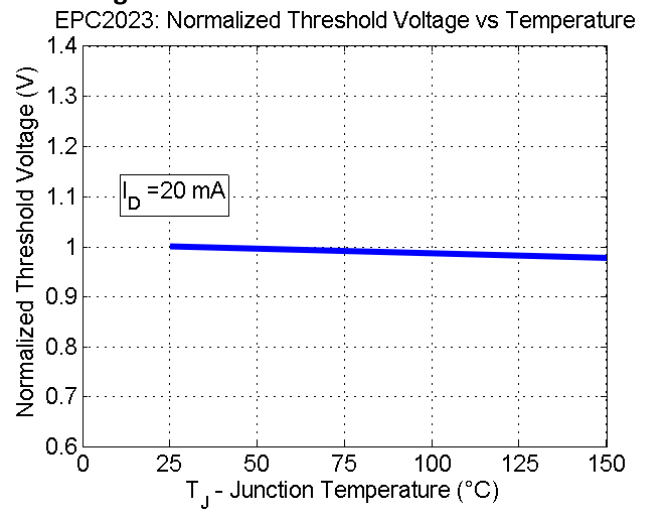
**Figure 7:**



**Figure 8:**



**Figure 9:**

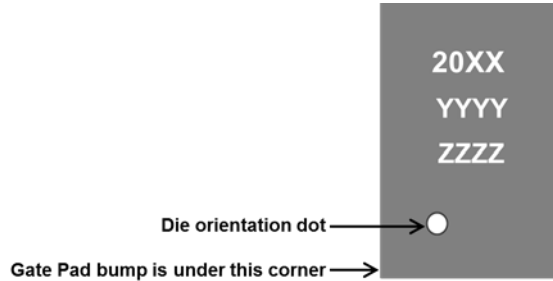


All measurements were done with substrate shorted to source

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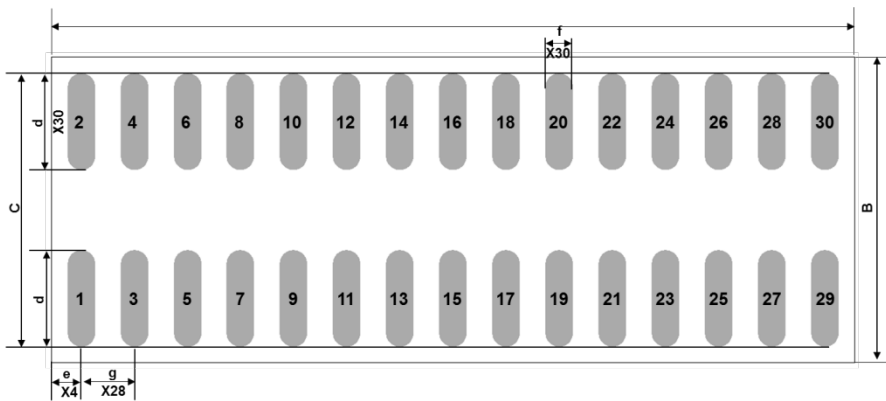
## DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2023ENGR	20XX	YYYY	ZZZZ

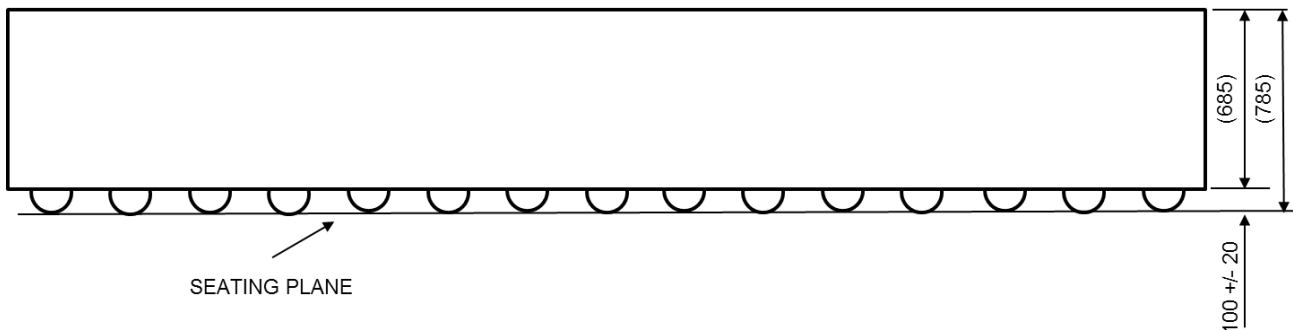
## DIE OUTLINE

### Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

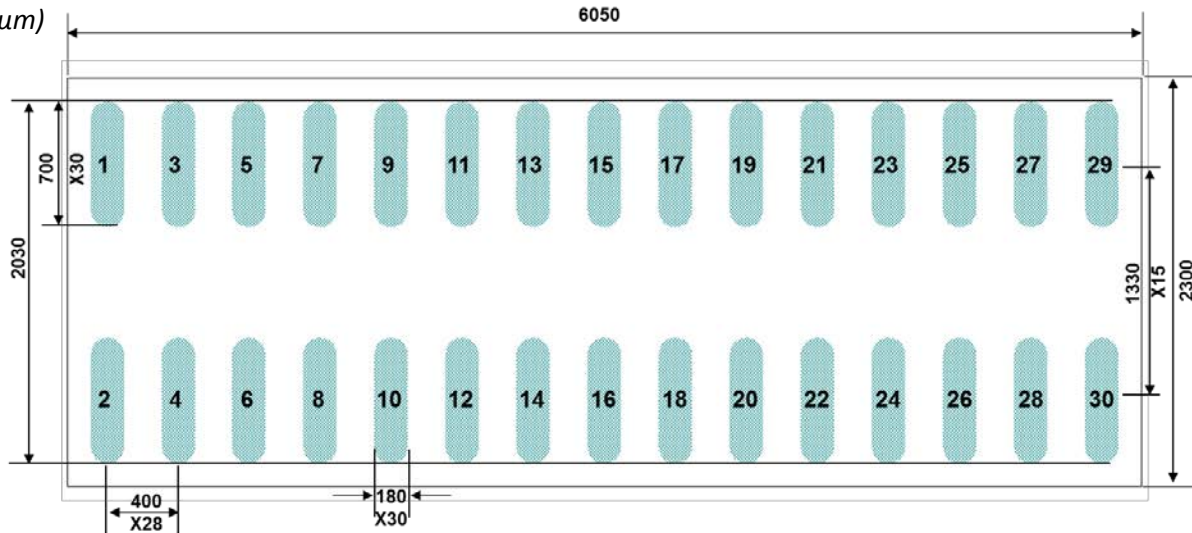
### Side View



# EPC2023 – Enhancement Mode Power Transistor Preliminary Specification Sheet

## RECOMMENDED LAND PATTERN

(Units in  $\mu\text{m}$ )

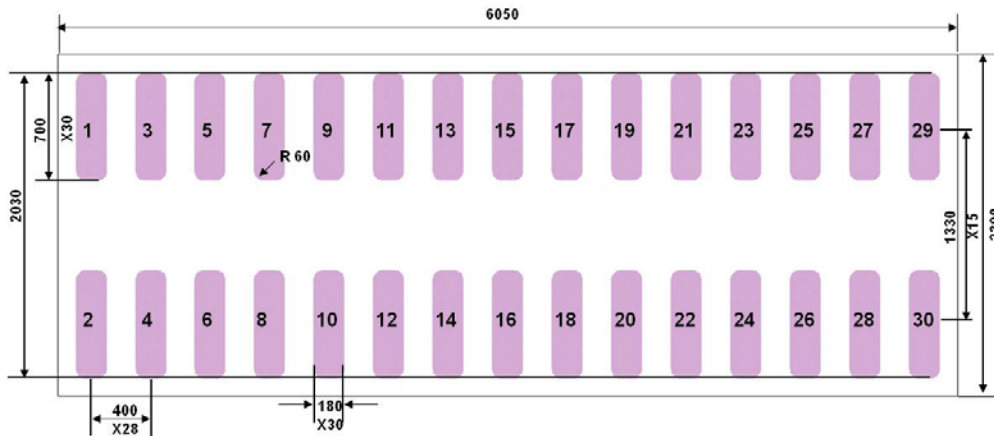


Pad 1 is Gate  
 Pads 2,5,6,9,10,13,14,17,18,21,22,25,26,29 are Source  
 Pads 3,4,7,8,11,12,15,16,19,20,23,24,27,28 are Drain  
 Pad 30 is Substrate

Land pattern is solder mask defined  
 Solder mask opening is 10  $\mu\text{m}$  smaller per side than bump

## RECOMMENDED STENCIL

(Units in  $\mu\text{m}$ )



Pad 1 is Gate  
 Pads 2,5,6,9,10,13,14,17,18, 21,22,25,26,29 are Source  
 Pads 3,4,7,8,11,12,15,16,19, 20,23,24,27,28 are Drain  
 Pad 30 is Substrate

Recommended stencil should be 4mil (100 $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

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