

## Product Summary

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C
-20V	5.5mΩ @ V <sub>GS</sub> = -4.5V	-40A
	7.5mΩ @ V <sub>GS</sub> = -2.5V	-40A

## Description and Applications

This MOSFET is designed to meet the stringent requirements of Automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

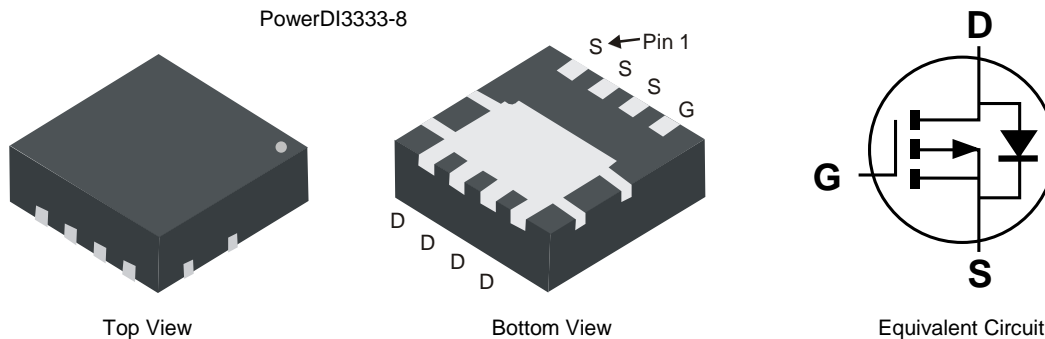
- Load Switch
- Power Management Functions

## Features

- Low R<sub>DS(ON)</sub> – Ensures On State Losses are Minimized
- Small Form Factor, Thermally Efficient Package Enables Higher Density End Products
- Occupies just 33% of the Board Area Occupied by SO-8 Enabling Smaller End Product
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Capable (Note 4)**

## Mechanical Data

- Case: PowerDI<sup>®</sup>3333-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.030 grams (Approximate)

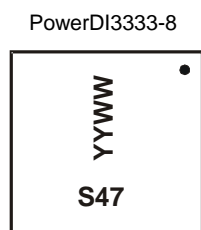


## Ordering Information (Note 5)

Part Number	Case	Packaging
DMP2006UFGQ-7	PowerDI3333-8	2,000/Tape & Reel
DMP2006UFGQ-13	PowerDI3333-8	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to [http://www.diodes.com/product\\_compliance\\_definitions.html](http://www.diodes.com/product_compliance_definitions.html).
  5. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



S47 = Product Type Marking Code  
YYWW = Date Code Marking  
YY = Last Two Digits of Year (ex: 17 = 2017)  
WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate-Source Voltage	V <sub>GSS</sub>	±10	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	I <sub>D</sub>	T <sub>A</sub> = +25°C	-17.5
Steady State		T <sub>A</sub> = +70°C	-14.0
		T <sub>C</sub> = +25°C	-40
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-80	A
Maximum Continuous Body Diode Forward Current (Note 6)	I <sub>S</sub>	-2.2	A
Avalanche Current (Note 8) L = 0.1mH	I <sub>AS</sub>	-23	A
Avalanche Energy (Note 8) L = 0.1mH	E <sub>AS</sub>	28	mJ

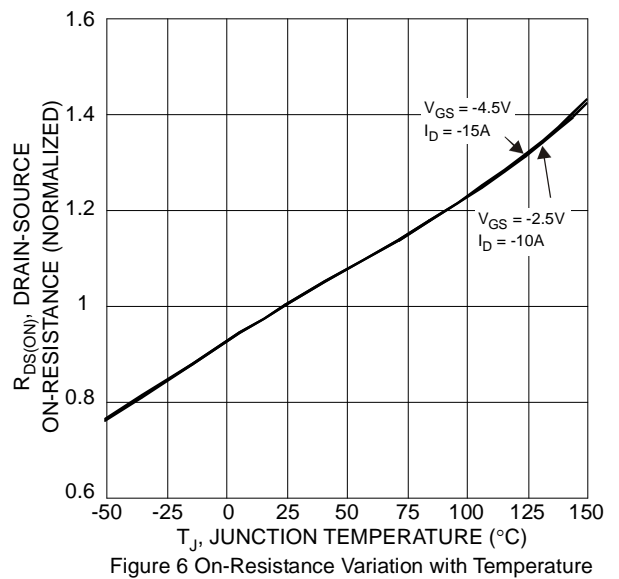
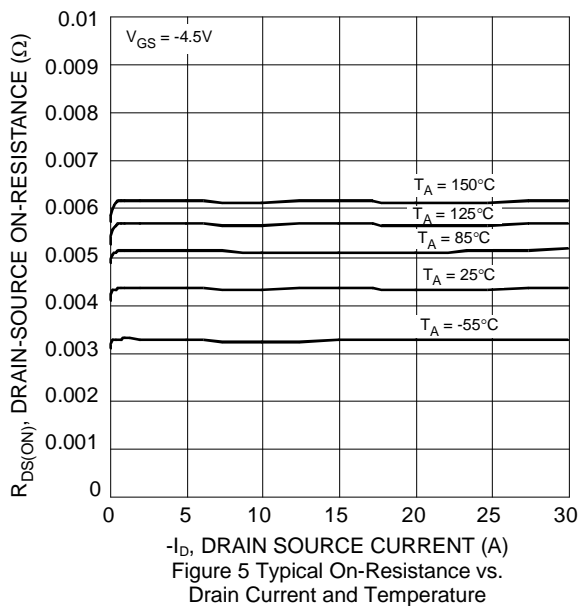
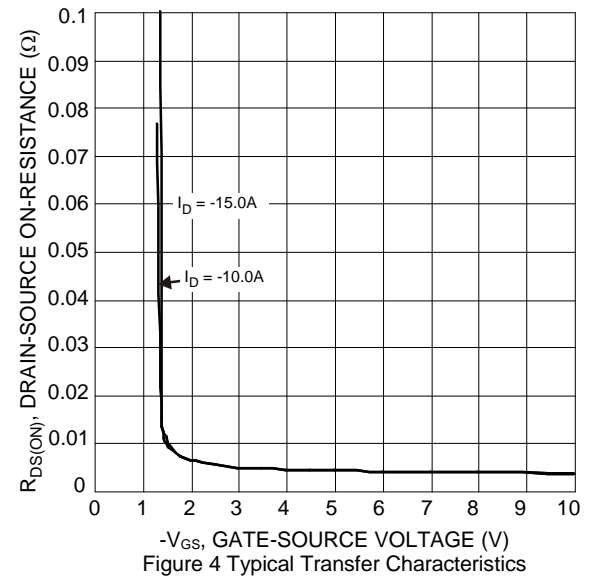
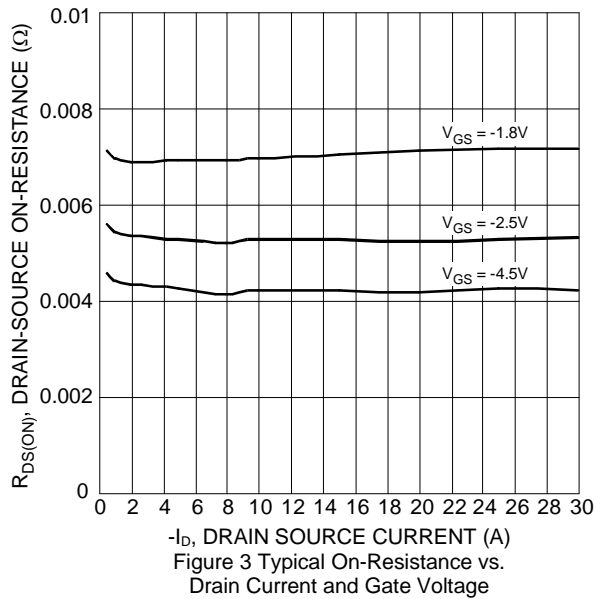
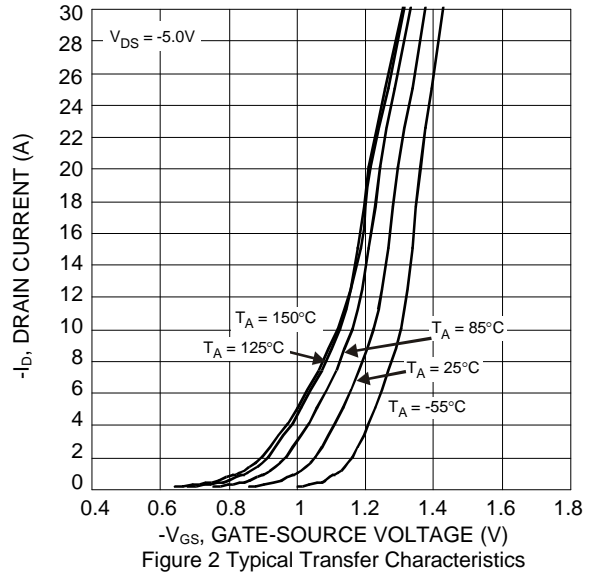
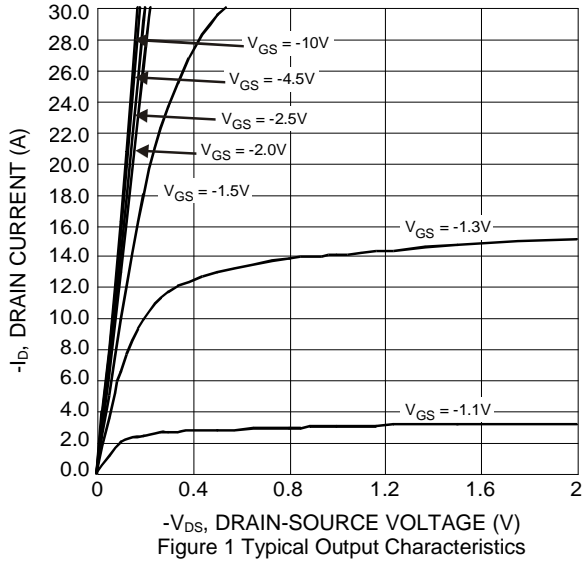
**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 6)	P <sub>D</sub>	T <sub>A</sub> = +25°C	2.3
		T <sub>C</sub> = +25°C	41
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	(Note 5)	54
		(Note 6)	136
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	3.0	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 9)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-1	µA	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 9)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-0.4	—	-1.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250µA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	4.2	5.5	mΩ	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -15A
		—	5.4	7.5		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -10A
		—	8	12		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -1A
		—	12	17		V <sub>GS</sub> = -1.5V, I <sub>D</sub> = -1A
Diode Forward Voltage	V <sub>SD</sub>	—	-0.7	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -10A
<b>DYNAMIC CHARACTERISTICS (Note 10)</b>						
Input Capacitance	C <sub>ISS</sub>	—	5404	7500	pF	V <sub>DS</sub> = -10V, V <sub>GS</sub> = 0V f = 1.0MHz
Output Capacitance	C <sub>OSS</sub>	—	728	1000		
Reverse Transfer Capacitance	C <sub>RSS</sub>	—	612	900		
Gate Resistance	R <sub>g</sub>	—	3.8	8	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = -4.5V)	Q <sub>g</sub>	—	64	100	nC	V <sub>DD</sub> = -10V, I <sub>D</sub> = -20A
Total Gate Charge (V <sub>GS</sub> = -10V)	Q <sub>g</sub>	—	140	200		
Gate-Source Charge	Q <sub>gs</sub>	—	8.5	15		
Gate-Drain Charge	Q <sub>gd</sub>	—	17	30		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	9.1	20	ns	V <sub>GS</sub> = -4.5V, V <sub>DD</sub> = -10V, R <sub>g</sub> = 1Ω, I <sub>D</sub> = -10A
Turn-On Rise Time	t <sub>r</sub>	—	19	35		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	146	220		
Turn-Off Fall Time	t <sub>f</sub>	—	104	150		
Reverse Recovery Time (Note 9)	t <sub>RR</sub>	—	61	100	ns	I <sub>F</sub> = -10A, di/dt = 100A/µs
Reverse Recovery Charge (Note 9)	Q <sub>RR</sub>	—	44	70	nC	I <sub>F</sub> = -10A, di/dt = 100A/µs

- Notes:
6. R<sub>θJA</sub> is determined with the device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.
  7. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  8. UIS in production with L = 0.1mH, T<sub>J</sub> = +25°C.
  9. Short duration pulse test used to minimize self-heating effect.
  10. Guaranteed by design. Not subject to product testing.



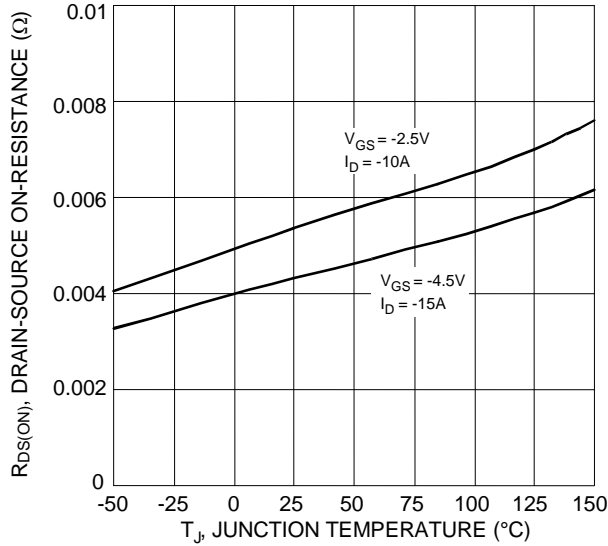


Figure 7 On-Resistance Variation with Temperature

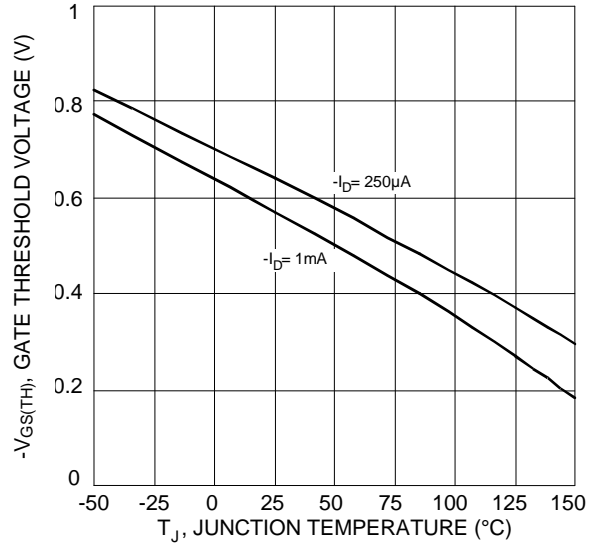


Figure 8 Gate Threshold Variation vs. Junction Temperature

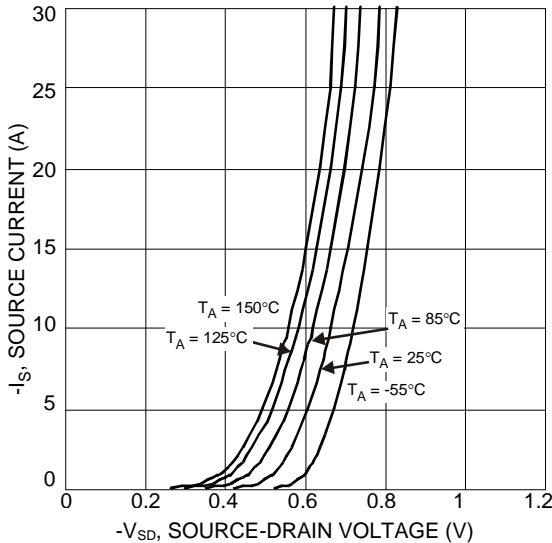


Figure 9 Diode Forward Voltage vs. Current

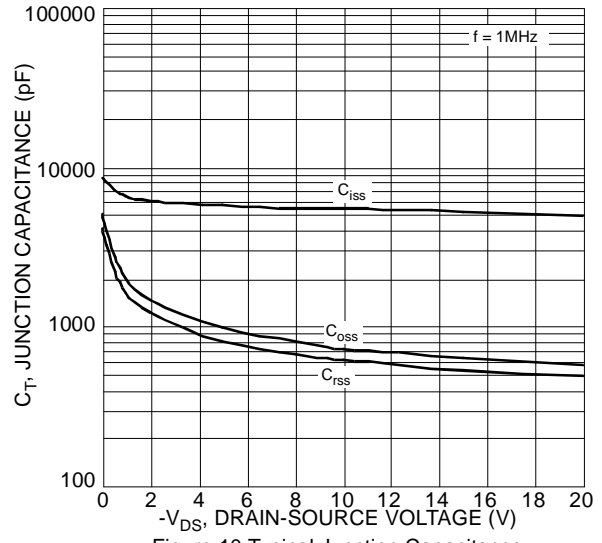


Figure 10 Typical Junction Capacitance

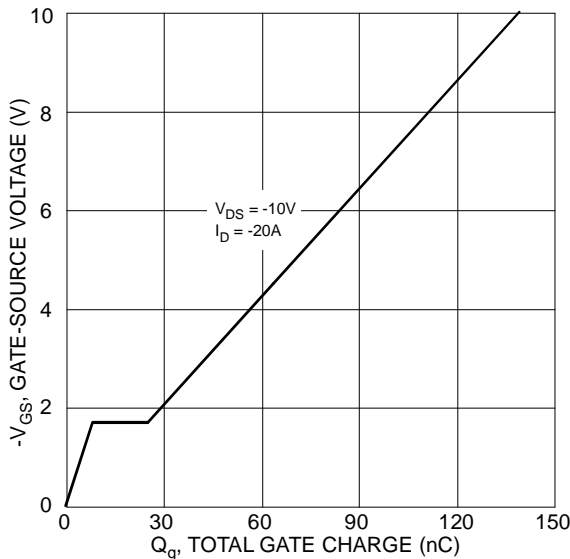


Figure 11 Gate-Charge Characteristics

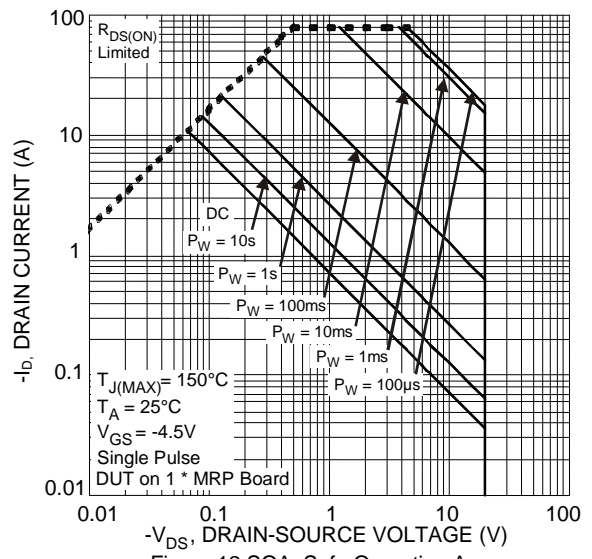
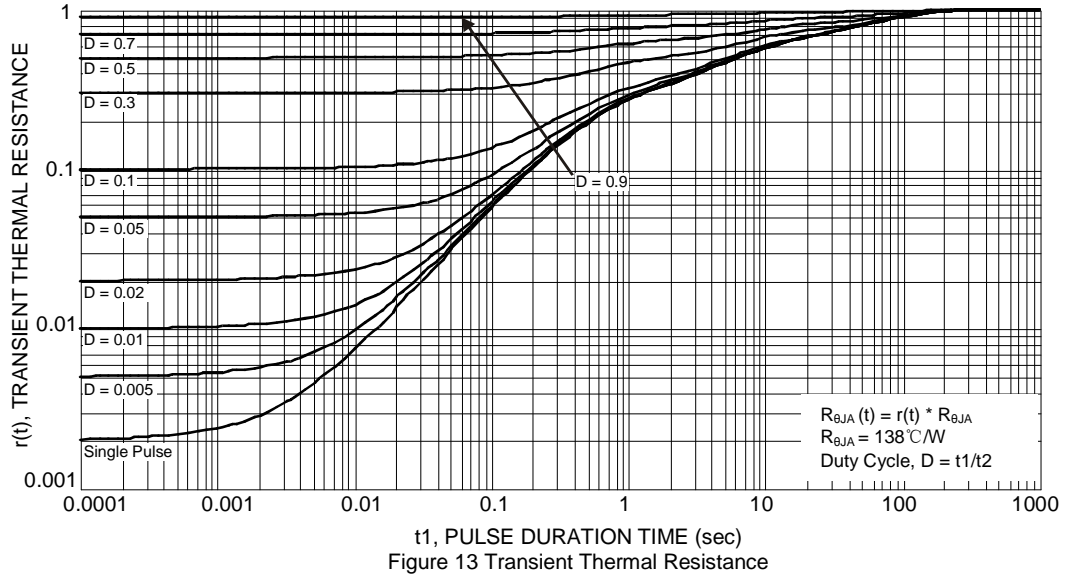


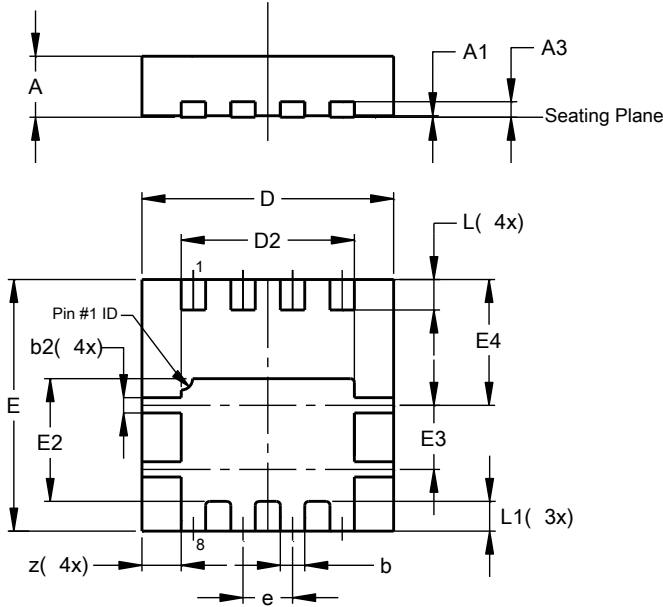
Figure 12 SOA, Safe Operation Area



**Package Outline Dimensions**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8**

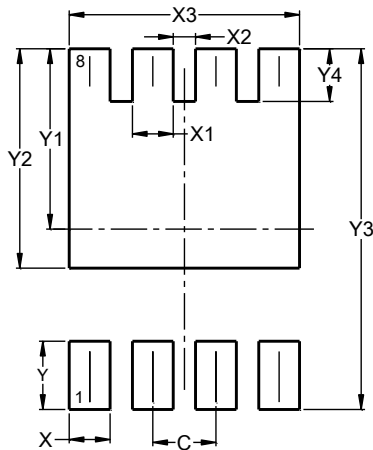


PowerDI3333-8			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.27	0.37	0.32
b2	0.15	0.25	0.20
D	3.25	3.35	3.30
D2	2.22	2.32	2.27
E	3.25	3.35	3.30
E2	1.56	1.66	1.61
E3	0.79	0.89	0.84
E4	1.60	1.70	1.65
e	-	-	0.65
L	0.35	0.45	0.40
L1	-	-	0.39
z	-	-	0.515
All Dimensions in mm			

**Suggested Pad Layout**

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**PowerDI3333-8**



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	0.420
X2	0.230
X3	2.370
Y	0.700
Y1	1.850
Y2	2.250
Y3	3.700
Y4	0.540

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