64 Bit PCI Master/Target

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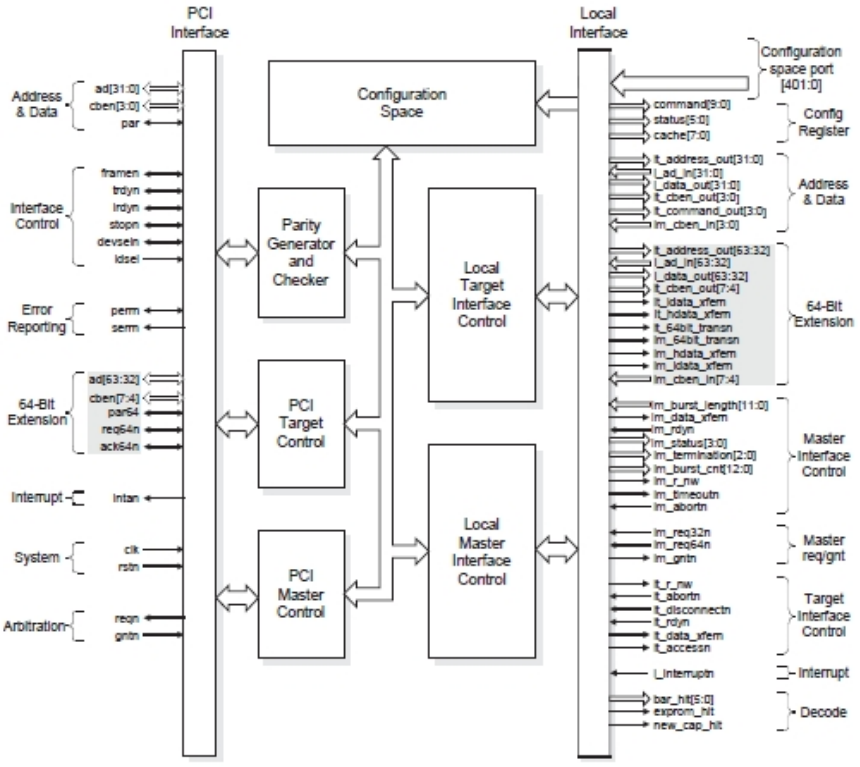
Overview

Peripheral Component Interconnect (PCI) is a widely accepted bus standard that is used in many applications including telecommunications, embedded systems, high performance peripheral cards, and networking.

Lattice's PCI IP core provides an ideal solution that meets the needs of today's high performance PCI applications. It is fully compliant with the PCI Local Bus Specification, revision 2.2 for speeds up to 66MHz. The PCI core provides a **customizable 32/64-bit master/target** or target solution. The core bridges the gap between the PCI interface and a specific design application, providing an integrated PCI solution. The PCI solution allows designers to focus on the application rather than on the PCI specification, resulting in a faster time-to-market.

The Lattice PCI offering is available in a number of configurations covering 32-bit PCI, 64-bit PCI, 32-bit local bus, 64-bit local bus, master/target and target applications. In this document, details of 64-bit operation and master operation only apply when relevant. The appendix to the user's guide shows what cores are available on which devices.



Note: Signals in shaded boxes are used for 64-bit PCI Cores.

Features

- Available as 32/64-Bit PCI Bus and 32/64-Bit Local Bus
- PCI SIG Local Bus Specification, Revision 3.0 Compliant
- 64-Bit Addressing Support (Dual Address Cycle)
- Capabilities List Pointer Support
- Parity Error Detection
- Up to Six Base Address Registers (BARs)
- Fast Back-to-Back Transaction Support
- Supports Zero Wait State Transactions
- Special Cycle Transaction Support
- Customizable Configuration Space
- Up to 66MHz PCI
- Fully Synchronous Design

Performance and Resource Utilization

LatticeECP3[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	1005	1552	847	-	89	33
64-bit	Master/Target 66 MHz	1550	2570	867	-	89	66

1. Performance and utilization data are generated using an LFE3-95EA-7FN1156CES device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	1168	1561	849	-	89	33
64-bit	Master/Target 66 MHz	1598	2580	869	-	89	66

1. Performance and utilization data are generated using an LFE2M-35E-6F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.

LatticeECP2[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	1168	1561	849	-	89	33
64-bit	Master/Target 66 MHz	1598	2580	869	-	89	66

1. Performance and utilization data are generated using an LFE2-20E-6F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeEC/P[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	1153	1549	849	-	89	33
64-bit	Master/Target 66 MHz	1599	2569	869	-	89	66

1. Performance and utilization data are generated using an LFEC33E-5F672C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP/EC family.

LatticeSC[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	986	1529	850	-	89	33
64-bit	Master/Target 66 MHz	1513	2631	871	-	89	66

1. Performance and utilization data are generated using an LFSC3GA25E-6F900C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC family.

LatticeXP2[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)
64-bit	Master/Target 33 MHz	1100	1553	847	-	89	33
64-bit	Master/Target 66 MHz	1530	2572	867	-	89	66

1. Performance and utilization data are generated using an LFXP2-17E-6F484C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

LatticeXP[1]

Bus Width	IPexpress Mode	Slices	LUTs	Registers	sysMEM EBRs	External Pins	f_{MAX} (MHz)

64-bit	Master/Target 33 MHz	1090	1549	849	-	89	33

1. Performance and utilization data are generated using an LFXP20C-5F484C device with Lattice Diamond 1.0 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP family.

Ordering Information

Family	Bus Width	Bus Speed	Master/Target Part Number
LatticeECP3	64-bit	33MHz, 66MHz	PCI-MT64-E3-U6
LatticeECP2M	64-bit	33MHz, 66MHz	PCI-MT64-PM-U6
LatticeECP2	64-bit	33MHz, 66MHz	PCI-MT64-P2-U6
LatticeECP/EC	64-bit	33MHz, 66MHz	PCI-MT64-E2-U6
LatticeSC	64-bit	33MHz, 66MHz	PCI-MT64-SC-U6
LatticeXP2	64-bit	33MHz, 66MHz	PCI-MT64-X2-U6
LatticeXP	64-bit	33MHz, 66MHz	PCI-MT64-XM-U6

IP Version: PCI Master/Target 33MHz = 6.6, PCI Master/Target 66MHz = 6.4
Evaluate: To download a full evaluation version of this IP, go to the Lattice IP Server tab in the IPexpress Main Window. All ispLeverCORE IP cores and modules available for download are visible on this tab. *PCI cores for ORCA and ispXPGA,devices are supported by the Lattice factory-configurable design flow.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.

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