DATA SHEET

AU5783

J1850/VPW transceiver with supply control function

Preliminary specification
Supersedes data of 2000 Nov 29

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Philips
Semiconductors

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J1850/VPW transceiver with supply control function AU5783

FEATURES

- Supports SAE/J1850 VPW standard for in-vehicle class B multiplexing
- Bus speed 10.4 kbit/s nominal
- 4X transmission mode (41.6 kbit/s)
- Drive capability 32 bus nodes
- Low RFI due to output waveshape function
- Direct battery operation with protection against +40 V load dump and 8 kV ESD
- Bus terminals proof against automotive transients up to +100 V/–150 V and 8 kV ESD
- Power supply enable function
- Very low sleep mode power consumption
- Diagnostic loop-back mode
- Thermal overload protection
- 14-pin SOIC

DESCRIPTION

The AU5783 is a line transceiver being primarily intended for in-vehicle multiplex applications. It provides interfacing between a J1850 link controller and the physical bus wire. The device supports the SAE/J1850 VPWM standard with a nominal bus speed of 10.4 kbit/s. For data upload and download purposes the 4X transmission mode is supported with a nominal bus speed of 41.6 kbit/s. The AU5783 provides protection against loss of ground conditions, thus ensuring the network will be operational in case of an electronic control unit loosing connection to ground potential. Low power operation is supported through provision of a sleep mode with very low power consumption. In addition an external voltage regulator can be turned off via the AU5783 transceiver to further reduce the overall power consumption. The voltage regulator will be activated again upon detection of bus activity or upon a local wake-up event.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE
	NAME	DESCRIPTION	VERSION	
AU5783D	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	–40 to +125°C

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{BAT.op}$	Operating supply voltage, including low battery operation		5.5	12	16	V
T_{amb}	Operating ambient temperature range		–40		+125	°C
$V_{BAT.ld}$	Battery voltage	load dump, 1s			+40	V
V_{BOH}	Bus output voltage	250 Ω < R_L < 1.6 kΩ	6.7		8.0	V
V_{BI}	Bus input threshold		3.4		4.2	V
$I_{BAT.lp}$	Sleep mode supply current				90	µA
t_P	Propagation delay	Tx to Rx			25	µs
t_r	Bus output rise time			14		µs

BLOCK DIAGRAM

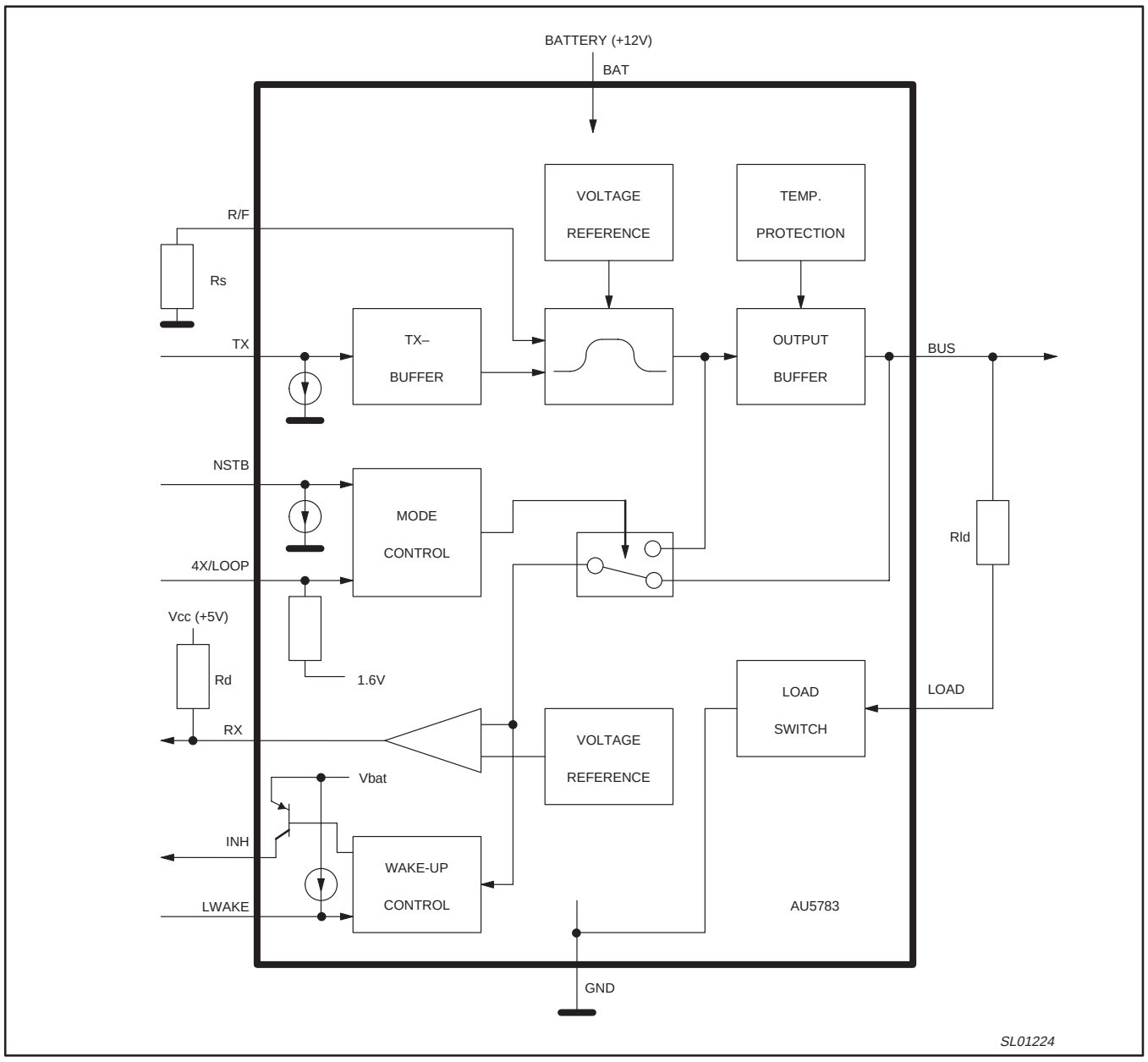


Figure 1. Block diagram

PINNING

Pin configuration

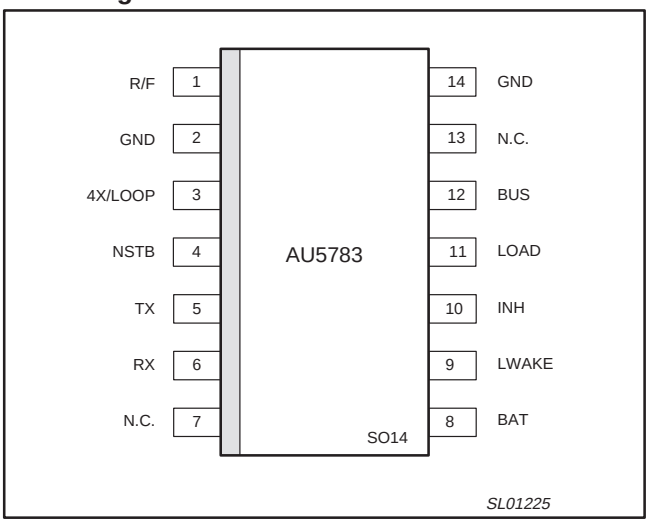


Figure 2. Pin configuration

Pin description

SYMBOL	PIN	DESCRIPTION
R/F	1	Rise/fall time control input; connect to ground potential via a resistor
GND	2	Ground
4X/LOOP	3	Tx mode control input; low: normal mode; high: 4X mode; float: loopback
NSTB	4	Network STandBy power control input; low: transmit function disabled (low power modes); high: transmit function enabled
TX	5	Transmit data input; low: transmitter passive; high: transmitter active
RX	6	Receive data output; low: active bus condition detected; high: otherwise
N.C.	7	Not connected
BAT	8	Battery supply input, 12V nominal
LWAKE	9	Local wake-up input, edge sensitive
INH	10	Activity indication flag (inhibit) output high side driver; e.g., to control a voltage regulator. Active high enables the regulator
LOAD	11	Bus load in/output
BUS	12	Bus line transmit/receive input/output, active high side driver
N.C.	13	Not connected
GND	14	Ground

FUNCTIONAL DESCRIPTION

The AU5783 is an integrated line transceiver IC that interfaces an SAE/J1850 protocol controller IC to the vehicle's multiplex bus line. It is primarily intended for automotive "Class B" multiplexing applications in passenger cars using VPW (Variable Pulse Width) modulated signals with a nominal transmission speed of 10.4 kbit/s. The device provides transmit and receive capability as well as protection to a J1850 electronic module.

A J1850 link controller feeds the transmit data stream to the transceiver's TX input. The AU5783 transceiver waveshapes the TX data input signal so as to minimize electromagnetic emission. The bus output signal features controlled rise & fall characteristic including rounded shape. A resistance being connected to the R/F control input sets the bus output slew rate.

The LOAD output is connected to the physical bus line via an external load resistor R_{ld}. The load resistor pulls the bus line to ground potential being the default state, e.g., when no transmitter outputs an active state. This output ensures the J1850 network will not be affected by a potential loss of ground condition at an individual electronic control unit.

The AU5783 includes a bus receiver with filter function to minimize susceptibility against interference. The logic state of the J1850 bus signal is indicated at the RX output being connected to the J1850 link controller.

The AU5783 also provides advanced low-power modes to help minimize ignition-off power consumption of an electronic control unit. The bus receiver function is kept alive in the low-power modes. If an active state is being detected on the bus line this will be indicated via the RX output. By default the AU5783 enters the low-power standby mode when the mode control inputs NSTB and 4X/LOOP are not driven. A 100 kΩ pull down resistor is required on NSTB.

Ignition-off current draw can be reduced further by turning off the voltage regulator being typically provided in an electronic control unit. This is supported by the activity indication function of the AU5783. In this application the activity indication flag INH will control external devices such as a voltage regulator. To turn-off the INH flag and thus the voltage regulator, the go to sleep command needs to be applied to the Network Standby power control input, e.g., NSTB = 0. The INH output is turned off after the sleep time-out period thereby, reducing the power consumption of an electronic control unit to an extremely low level.

The activity indication flag INH will be turned on again upon detection of a remote wake-up condition (i.e. bus activity) or upon detection of a local wake-up condition or a respective command from the microcontroller. A local wake-up condition is detected when an edge occurs at the wake-up input LWAKE. The INH flag will also be turned on upon detection of a high input level at the mode control input NSTB. Activation of the INH output enables external devices, e.g., a voltage regulator. This condition will power-up logic devices, e.g., a microcontroller in order to perform appropriate action, e.g., activation of the AU5783 and the J1850 network.

The AU5783 contain a power on reset (POR) circuit, which is active at low voltages. This circuit insures that if the control input NSTB is at 0 V or floating during power up, the device will be forced into the standby mode by the time the battery voltage rises to 4.4 V. This will also insure that the INH pin is in the high state to turn on the local voltage regulator. If there is a dip going below 4.4 V in battery voltage while in the sleep mode, the device may return to the

standby mode if the POR is tripped. Even if the device is not in sleep mode the INH output will turn off at some battery voltages below 4.4 V when the internal POR circuit is active. At still lower voltages where the POR circuit does not operate, the INH may again pull up toward the battery level, typically with battery voltages below approximately 3.6 V. The operation of the POR circuit can be verified by placing the device in the sleep mode while the battery voltage is above 4.4 V. The INH output, which is a high side driver, should turn off when the sleep mode is entered. Next ramp the battery voltage down to 2.0V and finally return the battery voltage to 4.4 V. When the battery supply is returned to 4.4V, the INH output will pull high since the device enters standby mode. The actual voltages at which the POR engages and releases will vary from part to part. The lowest voltage at which the POR will be active is 2.6 V and it will always release below 4.4 V.

The AU5783 provides a high-speed data transmission mode where the bus output waveshape function is disabled. In this mode transmit signals are output as fast as possible thus allowing higher data rates, e.g., the so-called 4X mode with 41.6 kbit/s nominal speed.

The AU5783 also provides a loop-back mode for diagnostic purpose, e.g., self-test of an electronic control unit. In loop-back mode the bus transmit and receive functions are disabled thus essentially disconnecting an electronic control unit from the J1850 bus line. The TX signal is internally looped back to the RX output.

The AU5783 only requires one power supply V_{BAT}. Bus transmissions can continue with battery voltage down to 5.5 V. The bus output voltage will track 1.3V bellow the battery voltage. The bus input voltage threshold will also follow the battery voltage going down as shown in Figure 3. This ratio metric behavior of the input threshold partially compensates for the reduced dominant level transmitted during low battery operation.

The AU5783 features special robustness at its BAT and BUS pins hence the device is well protected for applications in the automotive environment. Specifically the BAT input is protected against 40 V load dump and jump start condition. The BUS output is protected against wiring fault conditions, e.g., short circuit to ground and battery voltage as well as typical automotive transients and electrostatic discharge. In addition, an over-temperature shutdown function with hysteresis is incorporated which protects the device under network fault conditions. In case of the die temperature reaching the trip point, the AU5783 will latch-off the transceiver function. The device is reset on the first rising edge on the TX input after a decrease in the junction temperature.

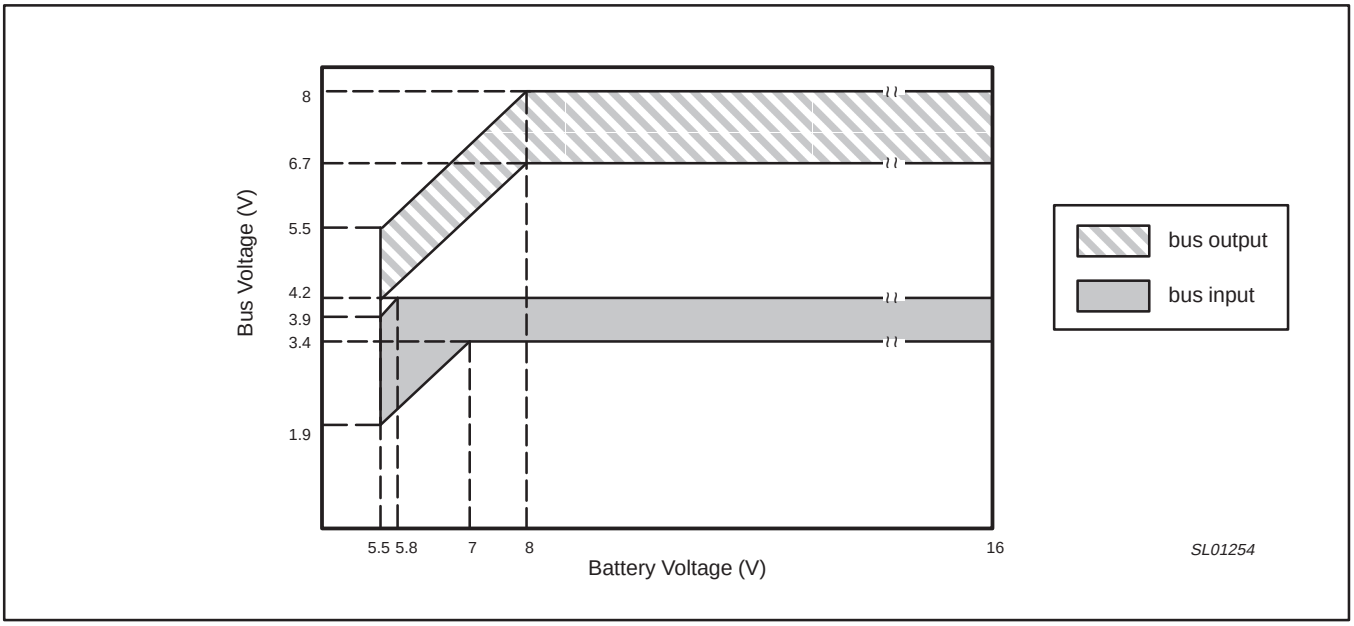


Figure 3. Bus voltage vs battery voltage

Table 1. Control input summary

Z = Input connected to high impedance permitting it to float. Typically accomplished by turning off the output of a microcontroller.
X = Don't care; The input may be at either logic level.

NSTB	4X/LOOP	TX	Mode	Bus transmitter	BUS	RX (out)	INH
1	0	1	normal operation	active	high	low	high
1	0	0	normal operation	passive	float	bus state, Note 2	high
1	1	1	4X transmit	active	high	low	high
1	1	0	4X transmit	passive	float	bus state, Note 2	high
1	Z	1	loop-back	passive	float	low	high
1	Z	0	loop-back	passive	float	high	high
0 or Z	X	X	standby (default state after power on), Note 1, Note 6	off	float	bus state, Note 5	high
1 –> 0	X	0	go to sleep command, Note 4, Note 6	off	float	bus state, Note 5	float, Note 3
0 or Z	X	X	sleep, Note 4, Note 6	off	float	bus state, Note 5	float

NOTES:

1. After power-on, the AU5783 enters standby mode since the input pins NSTB and 4X/LOOP are assumed to be floating. In standby mode the voltage regulator is enabled via the INH output, and therefore power is supplied to the microcontroller. When the microcontroller begins operation it will normally set the control inputs NSTB high and 4X/LOOP to low state in order to start normal operation of the AU5783.
2. RX outputs the bus state. If the bus level is below the receiver threshold (i.e., all transmitters passive), then RX will be high. Otherwise, if the bus level is above the receiver threshold (i.e., at least one transmitter is active), then RX will be low.
3. INH is turned off after a time-out period.
4. For entering the sleep mode (e.g., to deactivate INH), the "Go To Sleep" command needs to be applied. The "Go To Sleep" command is a high-to-low transition on the NSTB input. When the "Go To Sleep" command is present, the INH flag is deactivated. This signal can be used to turn-off the voltage regulator of an electronic module. After the voltage regulator is turned off the microcontroller is no longer supplied and the NSTB input will be floating. The INH output will be set again upon detection of bus activity or occurrence of a local wake-up event.
5. In standby and sleep mode, the detection of a wake-up condition (e.g., high level on BUS) will be signalled on the output RX.
6. The NSTB pin contains a weak pull down which is active in the normal, loop-back and high-speed modes but is disabled in the sleep mode. To insure a logic 0 input if the microcontroller's outputs are tri-stated or the microcontroller is not powered, a 100 kΩ resistor between NSTB and ground is suggested.

ABSOLUTE MAXIMUM RATINGS

According to the IEC 134 Absolute Maximum System.
Unless otherwise specified, operation is not guaranteed under these conditions: all voltages are referenced to pin GND; positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT}	Voltage on pin BAT		–0.3	+34	V
$V_{BAT.ld}$	Short-term supply voltage	load dump, t < 1s		+40	V
$V_{BAT.tr}$	Transient voltage on pin BAT and pin LWAKE	SAE J1113 test pulses 3A and 3B, Rwake > 9 kΩ	–150	+100	V
V_{B0}	Bus voltage	V_{BAT} < 2 V, R_{ld} > 1.4 kΩ	–16	+18	V
V_{B1}	Bus voltage	V_{BAT} > 2 V, R_{ld} > 1.4 kΩ	–10	+18	V
$V_{B.tr}$	Transient bus voltage	SAE J1113, test pulses 3A and 3B, coupled via C = 1 nF; R_{ld} > 1.4 kΩ	–150	+100	V
V_{WKE}	Voltage on pin LWAKE		–0.3	≤ V_{BAT}	V
V_{WKR}	Voltage on pin LWAKE	via series resistor of Rwake > 9 kΩ	–16	+34	V
V_{INH}	DC voltage on pin INH		–0.3	≤ V_{BAT}	V
V_I	DC voltage on pins TX, RX, NSTB and 4X/LOOP		–0.3	7.0	V
$V_{I,RF}$	DC voltage on pin R/F		–0.3	5.0	V
ESD_{HBM1}	ESD capability of pins BAT, BUS, LOAD and LWAKE	Human body model, direct contact discharge, R = 1.5 kΩ, C = 100 pF, R_{ld} > 1.4 kΩ; Rwake > 9 kΩ	–8	+8	kV
ESD_{HBM2}	ESD capability of all pins	Human body model, direct contact discharge, R = 1.5 kΩ, C = 100 pF	–2	+2	kV
P_{tot}	Maximum power dissipation	@ T_{amb} = +125°C		205	mW
Θ_{JA}	Thermal impedance	with standard test PCB		120	°C/W
T_{amb}	Operating ambient temperature		–40	+125	°C
T_{vj}	Operating junction temperature		–40	+150	°C
T_{stg}	Storage temperature		–40	+150	°C

DC ELECTRICAL CHARACTERISTICS

$7V < V_{BAT} < 16$ V; -40 °C $< T_{amb} < +125$ °C; 250 Ω $< R_L < 1.6$ kΩ; 1.4 kΩ $< R_{ld} < 12$ kΩ;
$-2V < V_{bus} < +9$ V; NSTB = 5 V; 4X/LOOP = 5 V; $R_s = 56$ kΩ ± 1%; RX connected to +5 V via $R_d = 3.9$ kΩ; INH loaded with 100 kΩ to GND; LWAKE connected to BAT via 10 kΩ resistor; all voltages are referenced to pin 14 (GND); positive currents flow into the IC; typical values reflect the approximate average value at $V_{BAT} = 13$ V and $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin BAT & thermal shutdown						
$I_{BAT.sl}$	Sleep mode supply current	Note 1			90	µA
$I_{BAT.sb}$	Standby mode supply current	Note 1			500	µA
$I_{BAT.p.nl}$	Supply current; passive state, in normal or loopback modes	TX = 5 V; LWAKE = 0 V, 4X/LOOP = 0 or Z			3	mA
$I_{BAT.p.h}$	Supply current; passive state, in high speed mode	TX = 5 V; LWAKE = 0 V, 4X/LOOP = 5 V			10	mA
$I_{BAT.wl}$	Supply current; weak load	TX = 5 V, R_L = 1.38 kΩ, Note 2			25	mA
$I_{BAT.fl}$	Supply current; full load	TX = 5 V, R_L = 250 Ω			45	mA
T_{sd}	Thermal shutdown temperature	Note 2	155		190	°C
T_{hys}	Thermal shutdown hysteresis	Note 2	5		15	°C
Pins TX, NSTB						
V_{ih}	High level input voltage		2.7			V
V_{il}	Low level input voltage				0.9	V
I_{ihtx}	TX high level input current	V_{TX} = 5 V	50		200	µA
$I_{ih.nstb,nlh}$	NSTB high level input current in normal, loop back and high speed modes	V_{NSTB} = 5 V	10		50	µA
I_{il}	Low level input current	V_i = 0 V	–2		+2	µA
Pin 4X/LOOP						
V_{ih}	High level input voltage (High Speed Mode)	NSTB = 5 V	2.7			V
		NSTB = 5 V, Bare Die	2.9			V
I_{ih-5}	High level input current with 5 V logic	4X/LOOP = 5 V, NSTB = 5 V	50		300	µA
I_{ih-3}	High level input current with 3 V logic	4X/LOOP = 3 V, NSTB = 3 V	30		250	µA
V_{ilb}	Mid level input voltage (Loop back operation)	NSTB = 5 V	1.25		1.65	V
I_{ilb}	Loopback mode input current	NSTB = 5 V; Note 4	–2		2	µA
V_{il}	Low level input voltage (Normal Mode)	NSTB = 5 V			+0.7	V
$-I_{il}$	Low level input current	V_{4X} = 0 V, NSTB = 5 V	50		200	µA
$-I_{ils}$	Low level input current in standby and sleep mode	V_{4X} = 0 V, NSTB = 0 V	–5		+5	µA
Pin LWAKE						
V_{i_wh}	Local wake-up high	NSTB = 0 V	3.9			V
V_{i_Wl}	Local wake-up low	NSTB = 0 V			2.5	V
$-I_{I\_w}$	Low level input current	V_{LWAKE} = 0 V	2		25	µA
Pin INH						
$-I_{oh\_inh}$	INH high level output current	$V_{INH} = V_{BAT} - 1$ V; 4.9 V $< V_{BAT} <$ 16 V	120		500	µA
$-I_{ol\_inh}$	INH off-state output leakage	V_{INH} = 0 V; NSTB = 0 V	–5		+5	µA
V_{bat_POR}	Power-on reset release voltage; Battery voltage threshold for setting INH output high	NSTB = 0 V, BUS = 0 V, V_{BAT} = 4.4 V, verify INH = 1			4.4	V
Pin RX						
V_{ol_rx}	Low level output voltage	I_{RX} = 1.6 mA, BUS = 7 V, all modes	0		0.45	V
I_{ol_rx}	Low level output current	V_{RX} = 5 V, BUS = 7 V	2		20	mA
I_{oh_rx}	High level output leakage	V_{RX} = 5 V, BUS = 0 V, all modes	–10		+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin BUS						
V_{BOh_n}	BUS output high voltage in normal mode	TX = 5 V, 4X/LOOP = 0 V; 8 V < V_{BAT} < 16 V 250 Ω < R_L < 1.6 kΩ; Note 3	6.7		8.0	V
V_{BOh_h}	BUS output high voltage in high speed mode	TX = 5 V, 4X/LOOP = 5 V; 8 V < V_{BAT} < 16 V 250 Ω < R_L < 1.6 kΩ; Note 3	6.7		9.0	V
V_{BOhl}	BUS voltage; low battery	TX = 5 V; Note 3 5.5 V<V_{BAT} < 8 V; 250 Ω < R_L < 1.6 kΩ	V_{BAT}–1.3		V_{BAT}	V
$-I_{BO.LIM}$	BUS short circuit current	TX = 5 V; V_{BUS} = –2 V	30		100	mA
$-I_{BO.LK1}$	BUS leakage current; passive state	TX = 0 V; 0 V < V_{BAT} < 16 V; –2 V < V_{BUS} < +9 V	–100		+100	µA
$-I_{BO.LK0}$, $-I_{BO.LK5}$	BUS current with loss of battery	V_{BAT} < 2 V; –2 V < V_{BUS} < +9 V	–100		+100	µA
$-I_{BO.LKLB0}$, $-I_{BO.LKLB5}$	BUS leakage current; loop back mode	TX = 0 V or 5 V; 0 V<V_{BAT}<16 V; –2 V < V_{BUS} < +9 V	–100		+100	µA
$-I_{LOG}$	BUS leakage current at loss of ground	0 V < V_{BAT} < 16 V; see test circuit	–20		+100	µA
V_{Bih}	BUS input high voltage	5.8 V < V_{BAT} < 16 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V	4.2			V
V_{Bil}	BUS input low voltage	4X/LOOP = 5 V or 4X/LOOP = 0 V			3.4	V
V_{Bhy}	BUS input hysteresis	4X/LOOP = 5 V and 4X/LOOP = 0 V	0.1		0.5	V
V_{Bih_l}	BUS input high voltage at low battery	5.5 V < V_{BAT} < 5.8 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V	V_{BAT} – 1.6 V			V
V_{BiL_L}	BUS input low voltage at low battery	5.5 V < V_{BAT} < 7 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V			V_{BAT} – 3.6 V	V
V_{Bih_s}	BUS input high voltage in standby and sleep mode	NSTB = 0 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V, 6 V < V_{BAT} < 16 V	4.2			V
V_{Bil_s}	BUS input low voltage in standby and sleep mode	NSTB = 0 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V, 6 V < V_{BAT} < 16 V			2.2	V
V_{Bih_sl}	BUS input high voltage in standby and sleep mode at low battery	NSTB = 0 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V , 4.5 V < V_{BAT} < 6 V	$^1/_2$ (V_{BAT} + 2.4)			V
V_{Bil_sl}	BUS input low voltage in standby and sleep mode at low battery	NSTB = 0 V, 4X/LOOP = 5 V and 4X/LOOP = 0 V , 4.5 V < V_{BAT} < 6 V			$^1/_2$ (V_{BAT} – 1.6)	V
Pin LOAD						
V_{ld}	Load output voltage	I_{ld} = 2 mA			0.2	V
V_{ldoff}	Load output voltage unpowered	I_{ld} = 6 mA, V_{BAT} = 0 V			1	V

NOTES:

1. TX = 0 V; NSTB = 0 V; 7 V < V_{BAT} < 13 V; T_j < 125°C; –1 V < V_{BUS} < 1 V; LWAKE connected to BAT via 10 kΩ; INH not connected.
2. This parameter is characterized but not subject to production test.
3. For V_{BAT} < 8.3 V the bus output voltage is limited by the supply voltage. For 16 V < V_{BAT} < 27 V the load is limited by the package power dissipation ratings. The duration of the latter condition is recommended to be less than 2 minutes.
4. For 3-State devices driving the 4X/LOOP Pin, the leakage in the 3-State output must be below the specified input current to ensure the pin is biased in the center state to provide the loop back function. For 3-State devices driving the 4X/LOOP pin, the leakage in the 3-State output must be below the specified input current to insure the pin is biased in the center state to provide the loop back function. If the leakage current of the microcontroller is too high, then an alternate approach is to connect a resistor voltage divider between the V_{CC} and ground of the microcontroller's supply to provide approximately 1.45 V bias on the 4X/LOOP pin.

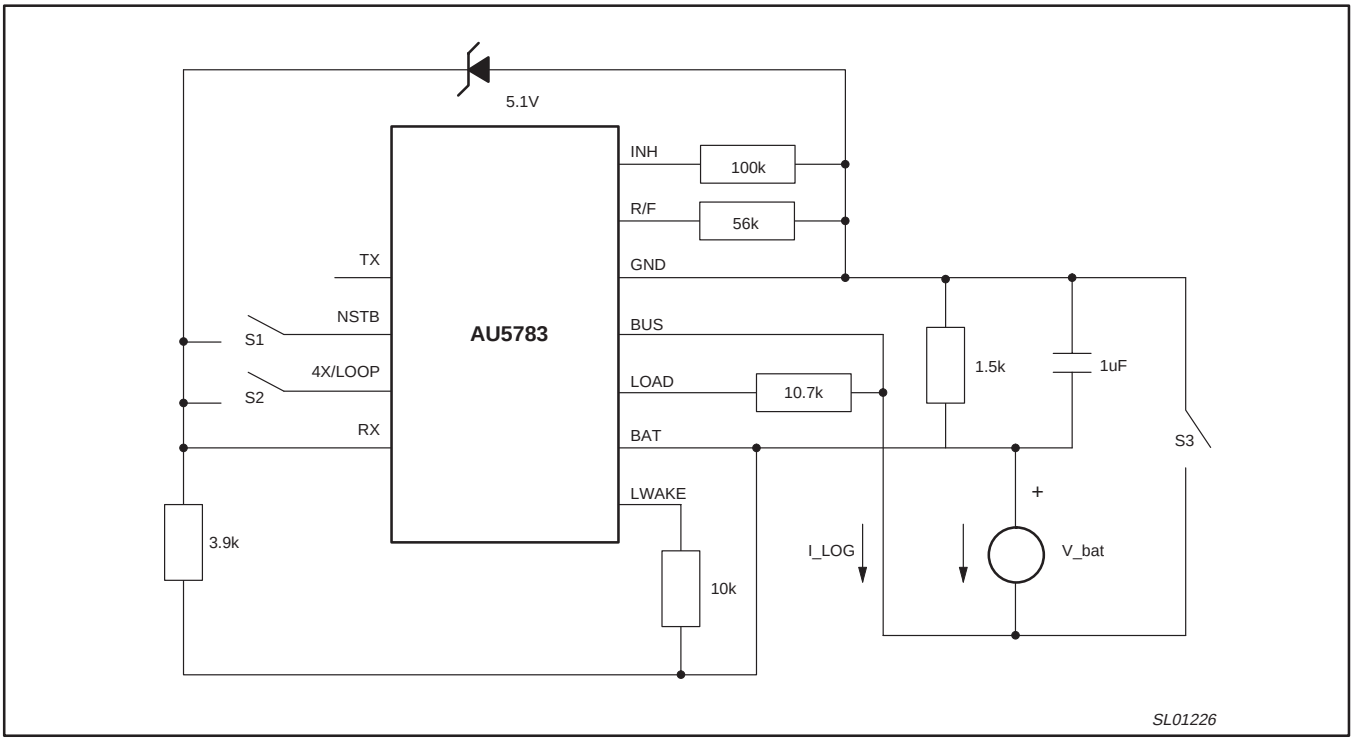
DYNAMIC CHARACTERISTICS

7 V < V_{BAT} < 16 V; –40°C < T_{amb} < +125°C; –2 V < V_{bus} < +9 V; 1.4 kΩ < R_{ld} < 12 kΩ
BUS: 250 Ω < R_L < 1.6 kΩ; 3 nF < C_L < 17 nF; 1.7 µs < (R_L * C_L) < 5.2 µs
Bus load A: R_L = 1.38 kΩ, C_L = 3.3 nF; Bus load B: R_L = 300 Ω, C_L = 16.5 nF
R/F pin: R_s = 56 kΩ ± 1%; INH loaded with 100 kΩ and 30 pF to GND
RX pin: R_d = 3.9 kΩ to 5 V; C_L = 30 pF to GND; NSTB = 5 V; 4X/LOOP = 0 V
Typical values reflect the approximate average value at V_{BAT} = 13 V and T_{amb} = 25°C, unless otherwise specified.
NSTB and 4X/LOOP rise and fall times < 10 ns.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CTX	TX input capacitance	Note 1			15	pF
INH output function						
t_{inhoff}	INH turn-off delay	BUS = 0 V, LWAKE = V_{BAT} or 0 V, go to sleep command, measured from NSTB = 0.9 V to INH = 3.5 V			200	µs
t_{inhonl}	LWAKE to INH turn-on delay	NSTB = 0 V, BUS = 0 V, measured from LWAKE = 3 V to INH = 3.5 V			100	µs
t_{inhonr}	BUS to INH turn-on delay	sleep mode, LWAKE = V_{BAT}, measured from BUS = 3.875 V to INH = 3.5 V			60	µs
BUS output function						
t_{BOon}; t_{BOoff}	Delay TX to BUS rising and falling edge	from TX = 2.5 V to BUS = 3.875 V; bus load A and bus load B	13		22	µs
t_{BrA}	BUS voltage rise time	bus load A, 9 V < V_{BAT} < 16 V, measured at 1.5 V and 6.25 V	11		18	µs
t_{BrB}	BUS voltage rise time	bus load B, 9 V < V_{BAT} < 16 V, measured at 1.5 V and 6.25 V	11		18	µs
t_{BfA}	BUS output voltage fall time	bus load A, 9 V < V_{BAT} < 16 V, measured at 1.5 V and 6.25 V	11		18	µs
t_{BfB}	BUS output voltage fall time	bus load B, 9 V < V_{BAT} < 16 V, measured at 1.5 V and 6.25 V	11		18	µs
t_{ir}	BUS output current rise time	bus load B connected to –2 V, 9 V < V_{BAT} < 16 V, measured at 20% and 80% of load capacitor current	4			µs
t_{if}	BUS output current fall time	bus load B connected to –2 V, 9 V < V_{BAT} < 16 V, measured at 20% and 80% of load capacitor current	4			µs
t_{wBh}	BUS high pulse width	TX = high for 64 µs, bus load condition A, 9 V < V_{BAT} < 16 V; minimum width measured at BUS = 6.25 V, maximum width measured at BUS = 1.5 V	35		93	µs
B_{HRM}	BUS output voltage harmonic content; normal mode	f = 530 kHz to 1670 kHz, bus load B connected to –2 V, TX = 7.81 kHz, 50% duty cycle, 9 V < V_{BAT} < 16 V, Note 1			70	dBµV
t_{BO4Xon}; $t_{BO4Xoff}$	TX to BUS delay in 4X mode	4X/LOOP = 1 V, bus load B, 9 V < V_{BAT} < 16 V, from TX = 1.8 V to BUS = 3.875 V	0.5		5	µs
t_{pon}; t_{poff}	Delay TX to RX rising and falling edge in normal mode	measured from 1.8 V on TX to 2.5 V on RX	13		25	µs
t_{plbon}; t_{plboff}	Delay TX to RX rising and falling edge in loop-back mode	NSTB = 5 V, 4X = floating, measured from 1.8 V on TX to 2.5 V on RX	13		25	µs
BUS input function						
t_{DRXon}; t_{DRXoff}	BUS input delay time, rising and falling edge	measured from V_{BUS} = 3.875 V to V_{RX} = 2.5 V	0.2		2	µs
t_{tRX}	RX output transition time, rising and falling edge	NSTB = 5 V, measured at 10% and 90% of waveform			1	µs
t_{tRXsl}	RX output transition time in standby and sleep mode, rising and falling edge	NSTB = 0 V, measured at 10% and 90% of waveform			5	µs
t_{DRXsl}	BUS to RX delay in sleep and standby modes	NSTB = 0 V, LWAKE = V_{BAT}, measured from BUS = 3.875 V to RX = 2.5 V	8		60	µs

NOTES:
1. This parameter is characterized but not subject to production test.

TEST CIRCUITS

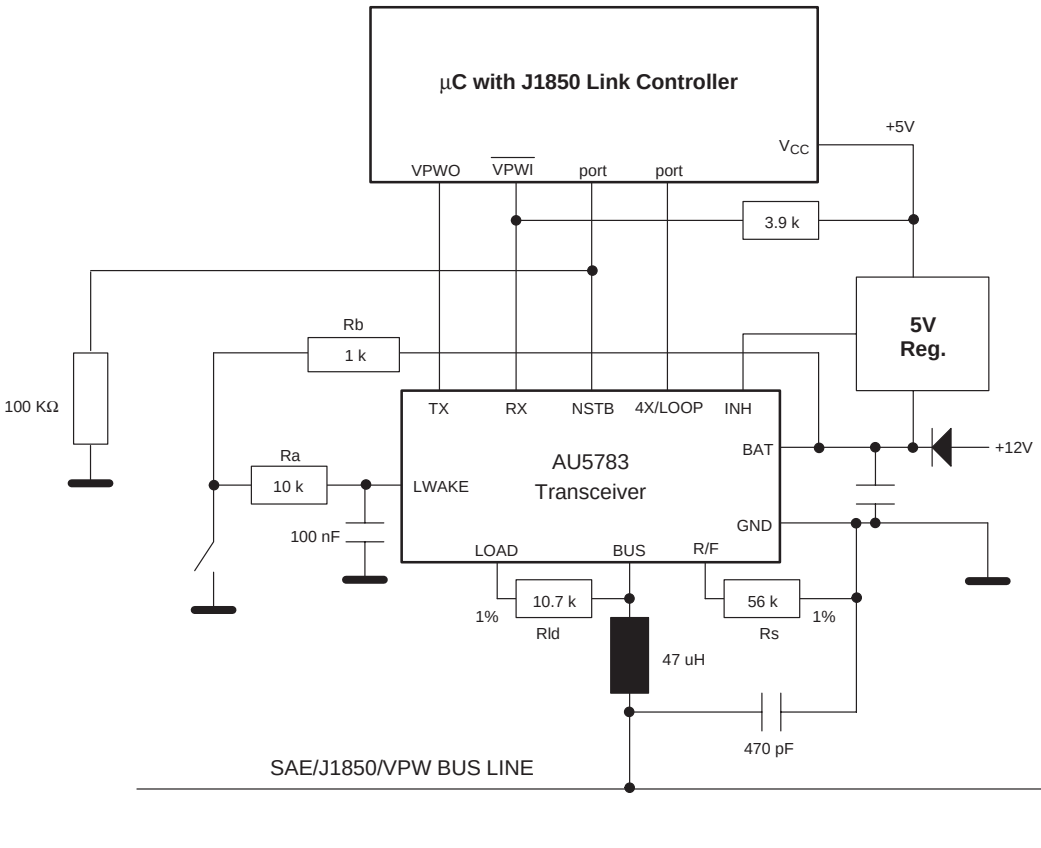


NOTE:

1. Check I_LOG with the following switch positions:
    1. S1 = open = S2
    2. S1 = open, S2 = closed
    3. S1 = closed, S2 = open
    4. S1 = closed = S2

Figure 4. Test circuit for loss of ground condition

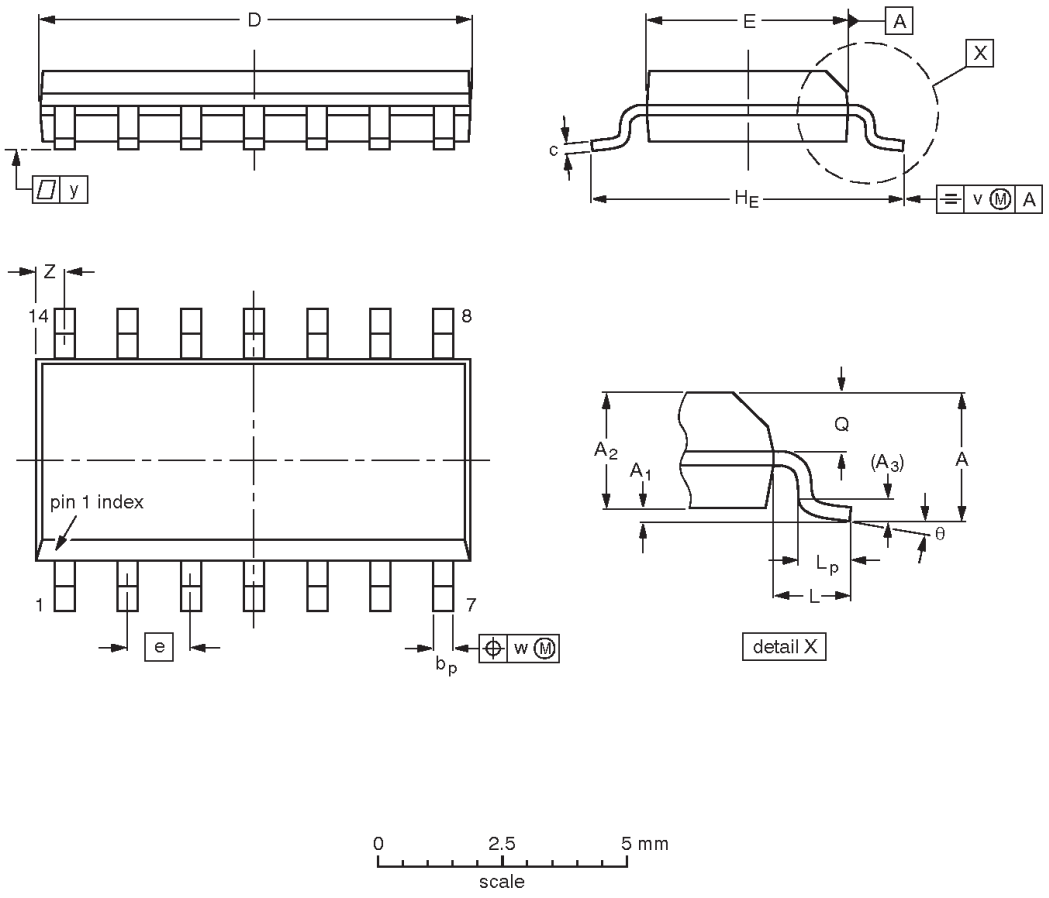
APPLICATION INFORMATION



NOTES:
1. Value of R_{ld} depends, e.g., on type of bus node. Example: secondary node R_{ld} =10.7 k, primary node R_{ld} =1.5 k.
2. For connection of the NSTB and 4X/LOOP pins there are different options, e.g., connect to a port pin or to V_{CC} or to active low reset.

Figure 5. Application of the AU5783 transceiver

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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