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Evaluation Board for the ADG5248F, Overvoltage Protected 8:1 Multiplexer

FEATURES

- Supply voltages
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Protected against overvoltage on source pins
  - Signal voltages up to −55 V and +55 V
- LEDs for visual overvoltage indication
- Parallel interface compatible with 3 V logic
- On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

EVAL-ADG5248FEBZ evaluation board

DOCUMENTS NEEDED

ADG5248F data sheet
EVAL-ADG5248FEBZ user guide

EQUIPMENT NEEDED

- DC voltage source
  - ±22 V for dual supply
  - 44 V for single supply
- Optional digital logic supply: 3 V to 5 V
- Analog signal source
- Method to measure voltage, such as a digital multimeter (DMM)

GENERAL DESCRIPTION

The EVAL-ADG5248FEBZ is the evaluation board for the ADG5248F, featuring an overvoltage protected 8:1 multiplexer. The ADG5248F has overvoltage detection and protection circuitry on the source pins and is protected against signals up to −55 V and +55 V in both the powered and unpowered states.

Figure 1 shows the EVAL-ADG5248FEBZ in a typical evaluation setup. The ADG5248F is soldered to the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, with a fourth terminal providing a user defined digital logic supply voltage, if required. Alternatively, a low dropout (LDO) regulator is provided for a 5 V digital logic supply and to supply the LEDs, which are mounted to provide visual indication of the fault status of the switch.

Full specifications on the ADG5248F are available in the ADG5248F data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

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REVISION HISTORY

5/2016—Rev. 0 to Rev. A

Changes to Figure 2 4
Changes to Table 1 6

7/2015—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

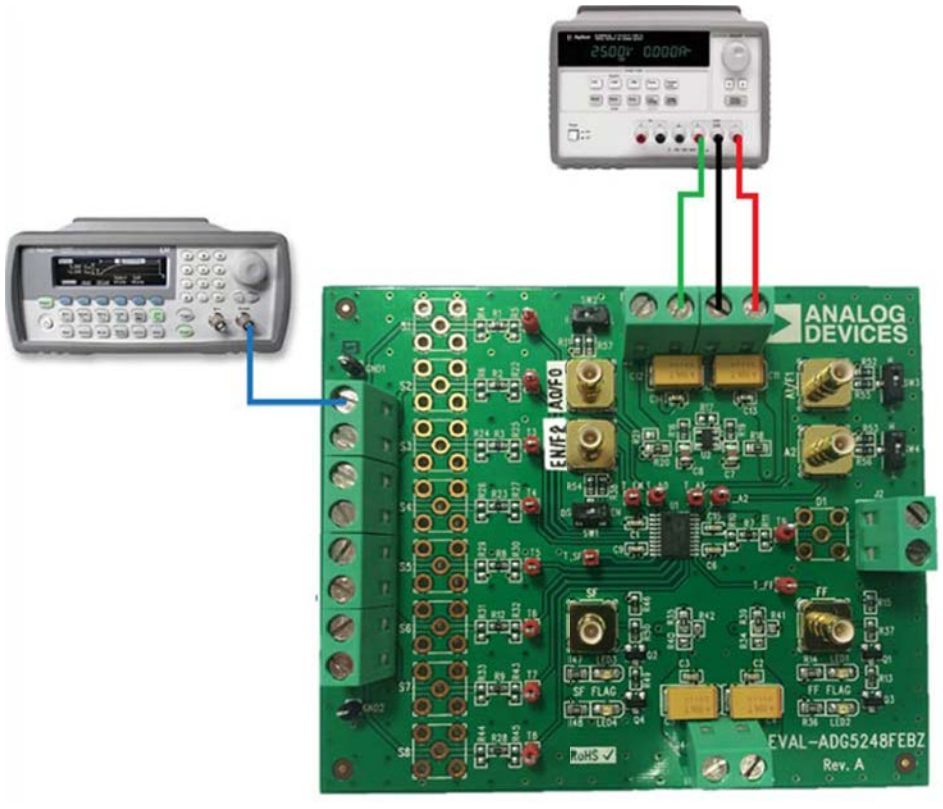

Figure 1.The EVAL-ADG5248FEBZ (on the Lower Right), Power Supply (on the Top Right), and Signal Generator (on the Left)

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5248FEBZ evaluation board operates independently and does not require any additional evaluation boards or software to operate. An on-board LDO regulator is the digital power supply for the LEDs and manually controls the ADG5248F.

Supply the evaluation board with a dual power source of up to ±22 V or a single supply of up to 44 V by connecting V_{SS} and GND together.

Set up a simple functionality test as follows:

1. Connect a power supply to J3. Connect VSS and GND together if a single supply is required.
2. Ensure a 0 Ω resistor is inserted in R18 to use the on-board LDO regulator, and that a 0 Ω resistor inserts into R20. SW1 through SW4 control the digital signals for the ADG5248F.
3. LED1 and LED3 illuminate green to indicate that the multiplexer is operating normally.

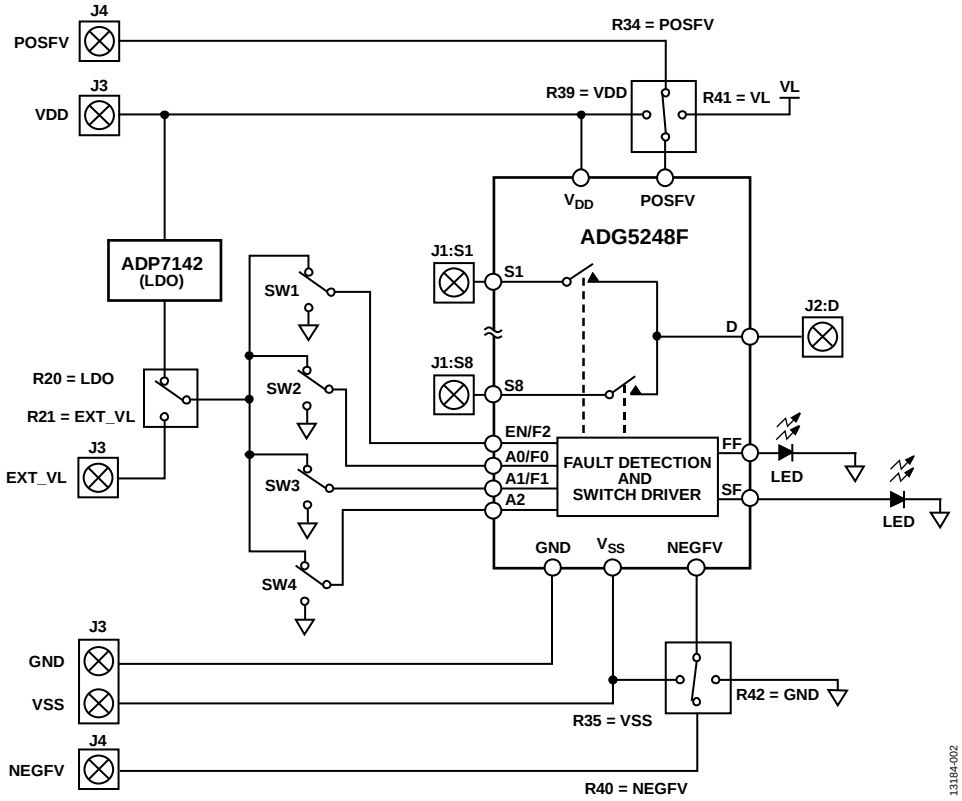

Figure 2. EVAL-ADG5248FEBZ Block Diagram

EVALUATION BOARD HARDWARE

Evaluate the operation of the ADG5248F using the EVAL-ADG5248FEBZ. Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

Using this evaluation board, the ADG5248F passes signals from either the source or drain connectors. The source pins have fault detection circuitry that react to an overvoltage event. During an overvoltage event, the channel where the fault occurs turns off, and the FF pin pulls low. The SF pin pulls low when the A0/F0, A1/F1, and EN/F2 pins select the source where the overvoltage occurs. See the ADG5248F data sheet for more details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the ADG5248F. The VDD, GND, and VSS screw terminals link to the appropriate pins on the ADG5248F. For dual supply voltages, power the evaluation board from ±5 V to ±22 V. For single supply voltages, connect the GND and V_{SS} terminals together, and power the evaluation board with 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. If necessary, connect a secondary voltage source to EXT_VL to control the digital voltages. To use EXT_VL, move the 0 Ω resistor from R20 to R21. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove R18 and supply an alternative digital voltage via EXT_VL if required.

INPUT SIGNALS

Two screw connectors provide access to the source and drain pins of the ADG5248F. Additional Subminiature Version B (SMB) connector pads are available if extra connections are required. The ADG5248F is overvoltage protected on the source side, and each source terminal (S1 to S8) can be presented with a voltage of up to +55 V or −55 V. See the ADG5248F data sheet for more details.

Each trace on the source and drain side includes two sets of 0603 pads, which can be used to place a load on the signal path to ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the 0603 pads create a simple resistor capacitor (RC) filter.

The ADG5248F uses a parallel interface to control the operation of the switches. The switch operation can be manually controlled using the SW1 to SW4 switches, or an external controller can be interfaced directly to the control pins by using the SMB connectors (EN/F2, A0/F0, A1/F1, and A2) and removing the 0 Ω R54 to R57 resistors.

OUTPUT SIGNALS

There are two outputs on the ADG5248F. The FF pin indicates when the device is operating normally or whether there is an overvoltage fault on one of the source pins. The SF pin also indicates when an overvoltage occurs on one of the source pins and transitions low only when an overvoltage occurs on the channel selected by the A0/F0, A1/F1, and EN/F2 inputs.

For visual indication, LEDs are mounted on the evaluation board. When the device is operating normally, the FF and SF pins remain high and LED1 and LED3 illuminate green. If an overvoltage occurs at any of the source pins, the FF pin pulls low and LED2 illuminates red. If an overvoltage occurs at the source pin selected by A0/F0, A1/F1, and EN/F2, the SF pin pulls low and LED4 illuminates red.

SMB connectors interface the evaluation board with external controllers.

JUMPER SETTINGS

SWITCHES AND 0 Ω RESISTORS

The switches on the evaluation board control the ADG5248F manually and 0 Ω resistors configure the VL supply voltage, the voltage present on POSFV and NEGFV, and isolate the LEDs from the rest of the system. Table 2 shows a summary of the uses of the switches and 0 Ω resistors on the evaluation board.

Use SW2 to SW4 to control the switches of the ADG5248F. Position L is tied to GND and sets the logic low. Position H is tied to VL and sets the logic high.

Use SW1 to enable or disable the device. Position DIS is tied to GND and disables the device, and position EN is tied to VL and enables the device.

Table 1. ADG5248F Truth Table

SW4 (A2)	SW3 (A1)	SW2 (A0)	SW1 (EN)	Connected Sx
X[1]	X[1]	X[1]	DIS (disable)	All switches off
L (low)	L (low)	L (low)	EN (enable)	S1
L (low)	L (low)	H (high)	EN (enable)	S2
L (low)	H (high)	L (low)	EN (enable)	S3
L (low)	H (high)	H (high)	EN (enable)	S4
H (high)	L (low)	L (low)	EN (enable)	S5
H (high)	L (low)	H (high)	EN (enable)	S6
H (high)	H (high)	L (low)	EN (enable)	S7
H (high)	H (high)	H (high)	EN (enable)	S8

[1] X = don't care.

R18 connects the on-board LDO regulator to the VDD supply. Remove this header to isolate the LDO regulator from the input screw terminal. Change the 0 Ω resistor from the R20 position to the R21 position to use an alternative digital supply voltage from the EXT_VL screw terminal.

Resistors R14, R36, R47, and R48 connect the LEDs to the digital power supply. R37 and R50 connect the FF and SF pins of the ADG5248F to the LED controls.

Resistors R34, R39, and R41 configure POSFV to either the voltage present on POSFV on J4, VDD, or VL. Resistors R35, R40, and R42 configure NEGFV to either VSS, the voltage present on NEGFV on J4, or GND.

SMB CONNECTORS

The SW1 to SW4 switches allow the user to manually control the parallel interface of the ADG5248F. Alternatively, the SMB connectors (EN/F2, A0/F0, A1/F1, and A2) can allow control via the external control signals. To use the SMB connectors, remove the 0 Ω resistors, R54 to R57. The FF/SF SMB connectors access the FF/SF digital outputs from the ADG5248F.

Table 2. Switch and 0 Ω Resistor Descriptions

Label	Position	Description
SW1	EN (enable)	Logic 0 on EN/F2 pin
	DIS (disable)	Logic 1 on EN/F2 pin
SW2	L (low)	Logic 0 on A0/F0 pin
	H (high)	Logic 1 on A0/F0 pin
SW3	L (low)	Logic 0 on A1/F1 pin
	H (high)	Logic 1 on A1/F1 pin
SW4	L (low)	Logic 0 on A2 pin
	H (high)	Logic 1 on A2 pin
R35, R40, and R42	R35	NEGFV set to VSS
	R40	NEGFV set to voltage on the J4 NEGFV screw terminal
	R42	NEGFV set to GND
R34, R39, and R41	R34	POSFV set to voltage on the J4 POSFV screw terminal
	R39	POSFV set to VDD
	R41	POSFV set to VL
R20 and R21	R20	On-board LDO regulator digital voltage
	R21	EXT_VL digital voltage
R18	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
R37 and R50	Inserted	FF and SF pins connected to LED
	Removed	FF and SF pins disconnected from LED
R14, R36, R47, and R48	Inserted	LED connected to digital supply
	Removed	LED isolated

EVALUATION BOARD SCHEMATICS AND ARTWORK

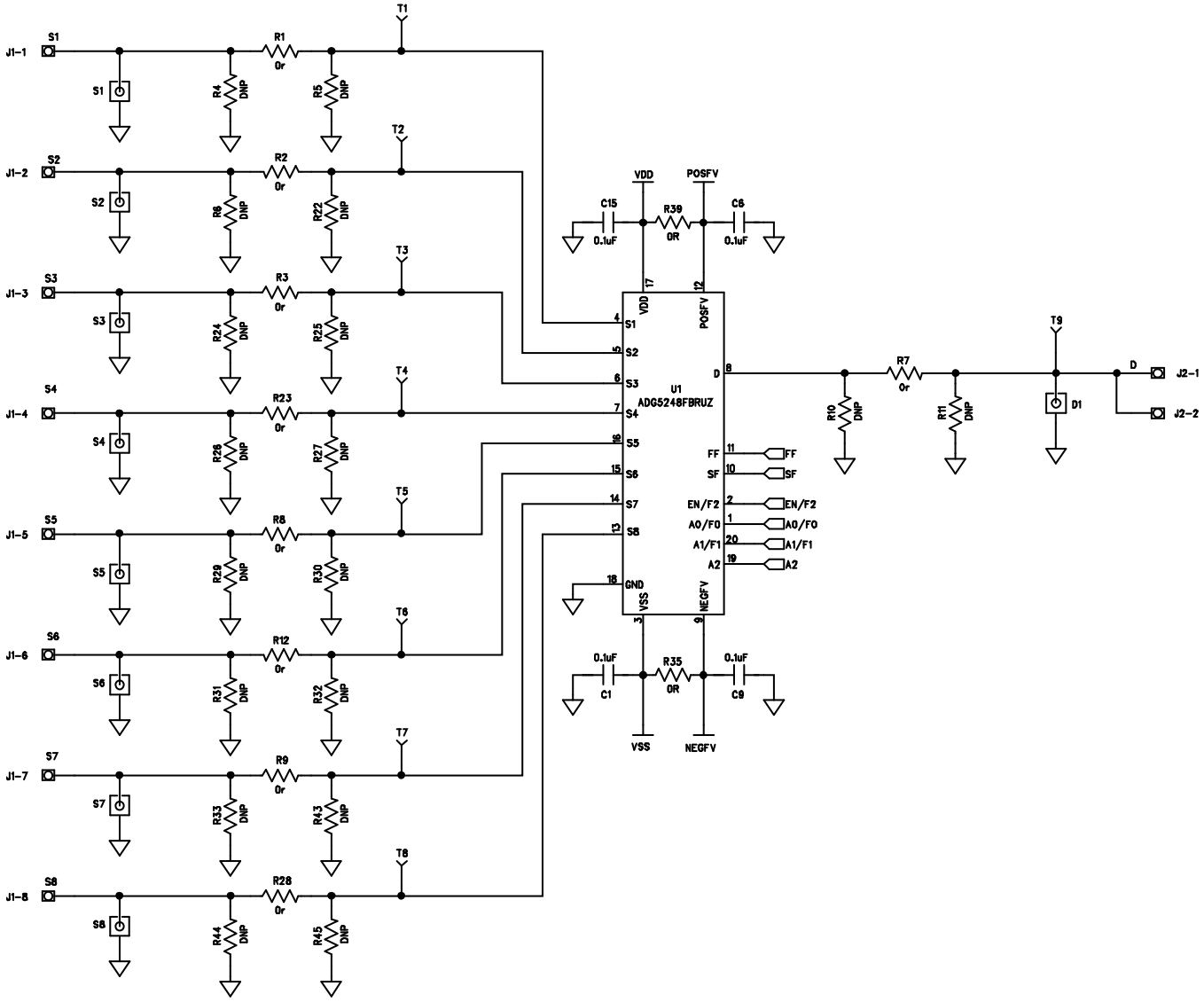

Figure 3. ADG5248F Evaluation Board Schematic (Part 1)

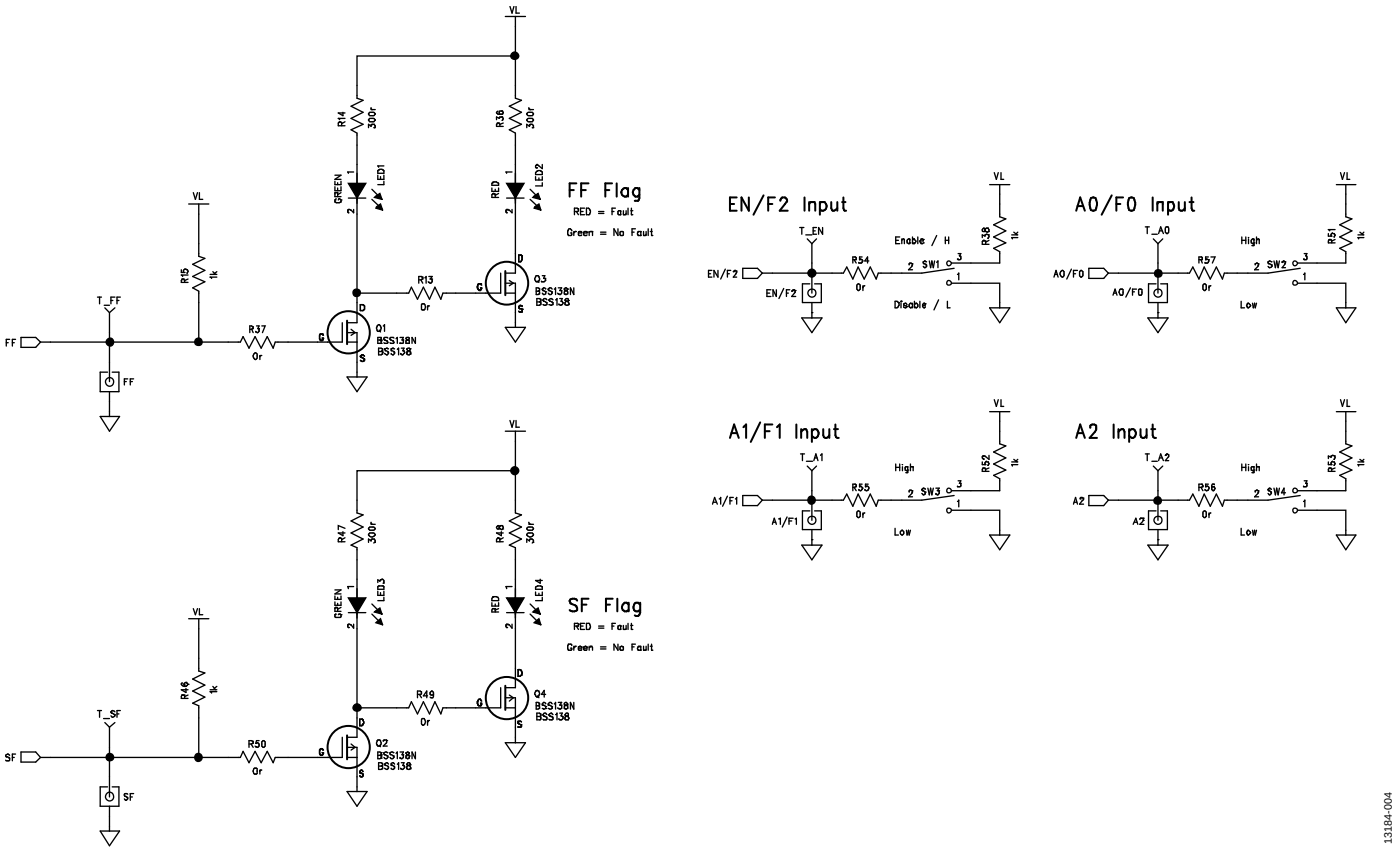

Figure 4. ADG5248F Evaluation Board Schematic (Part 2)

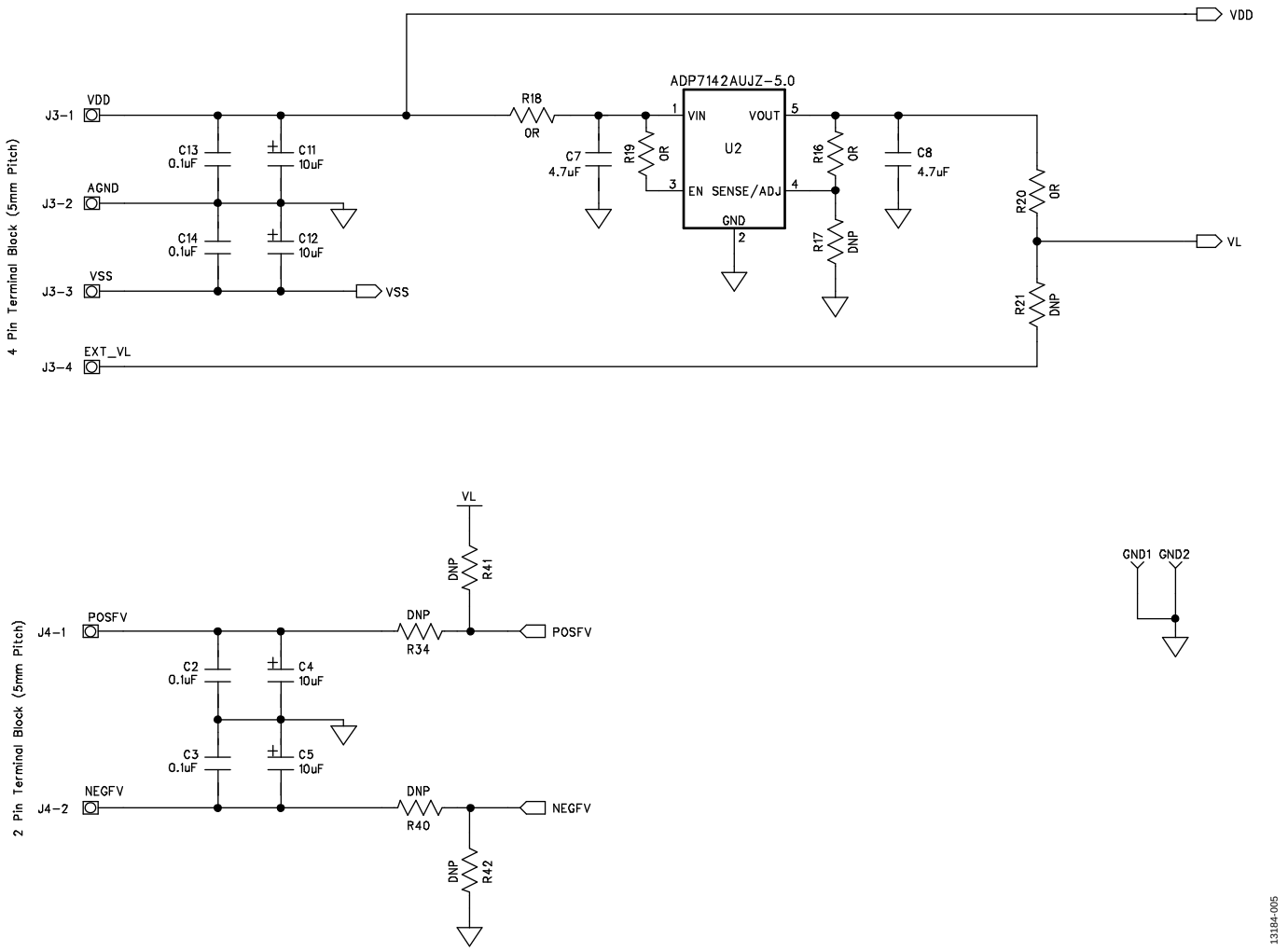

Figure 5. ADG5248F Evaluation Board Schematic (Part 3)

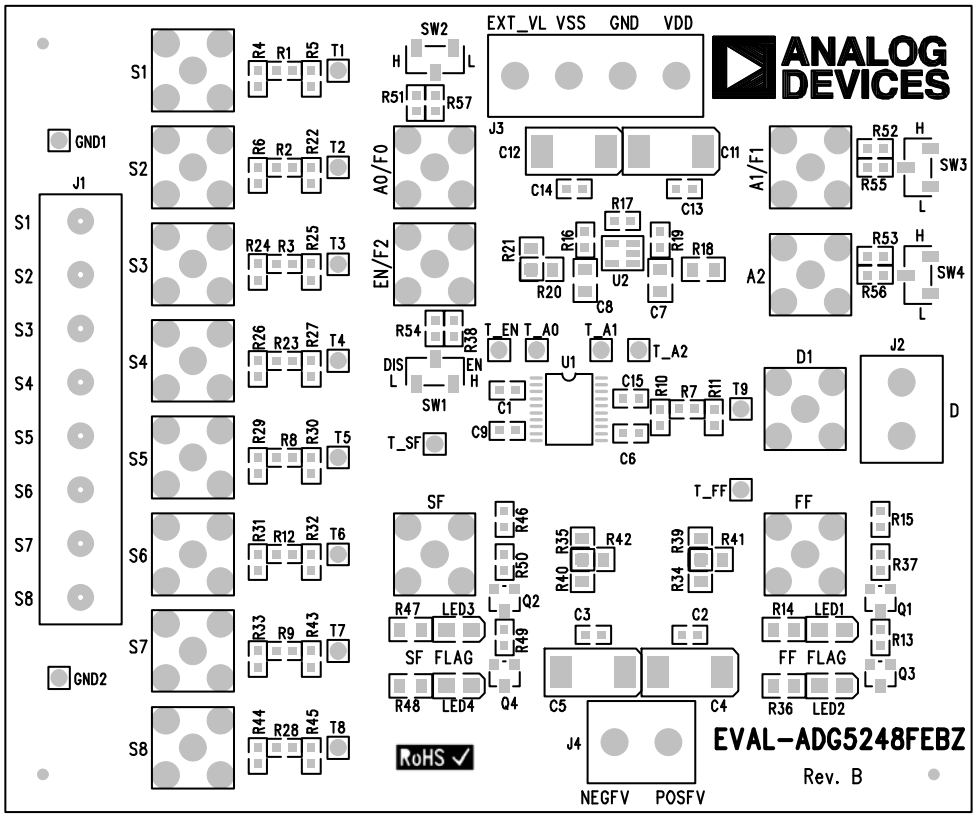

Figure 6. EVAL-ADG5248FEBZ Silk Screen

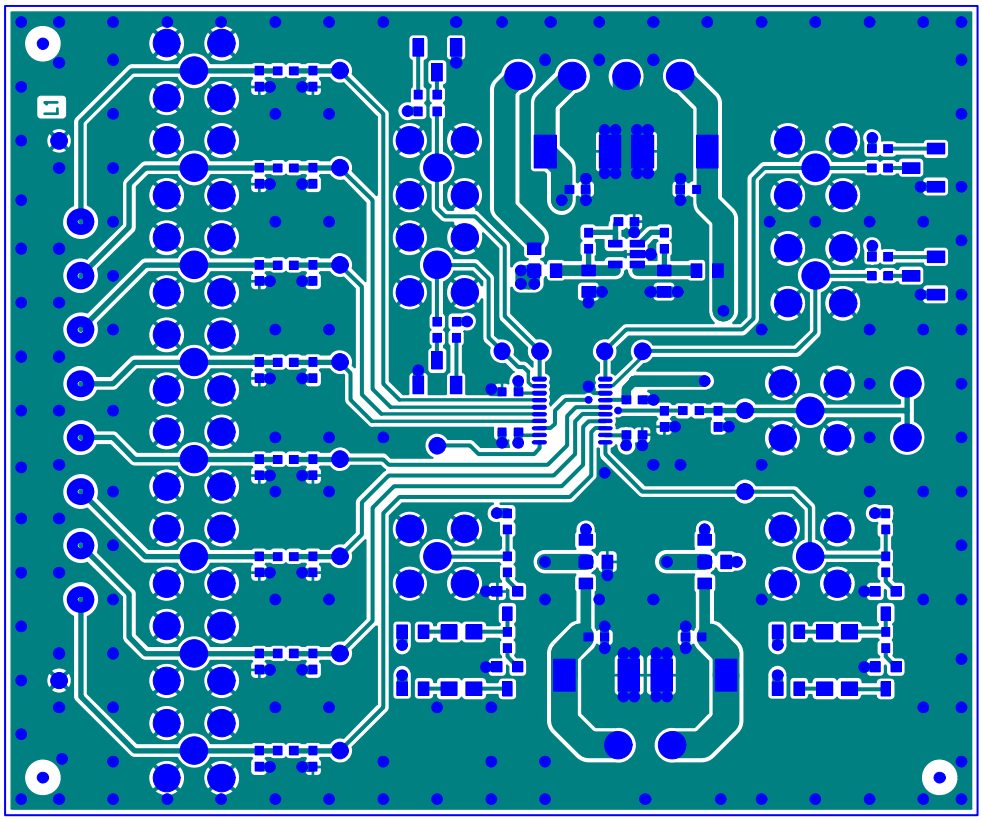

Figure 7. EVAL-ADG5248BFEBZ Top Layer

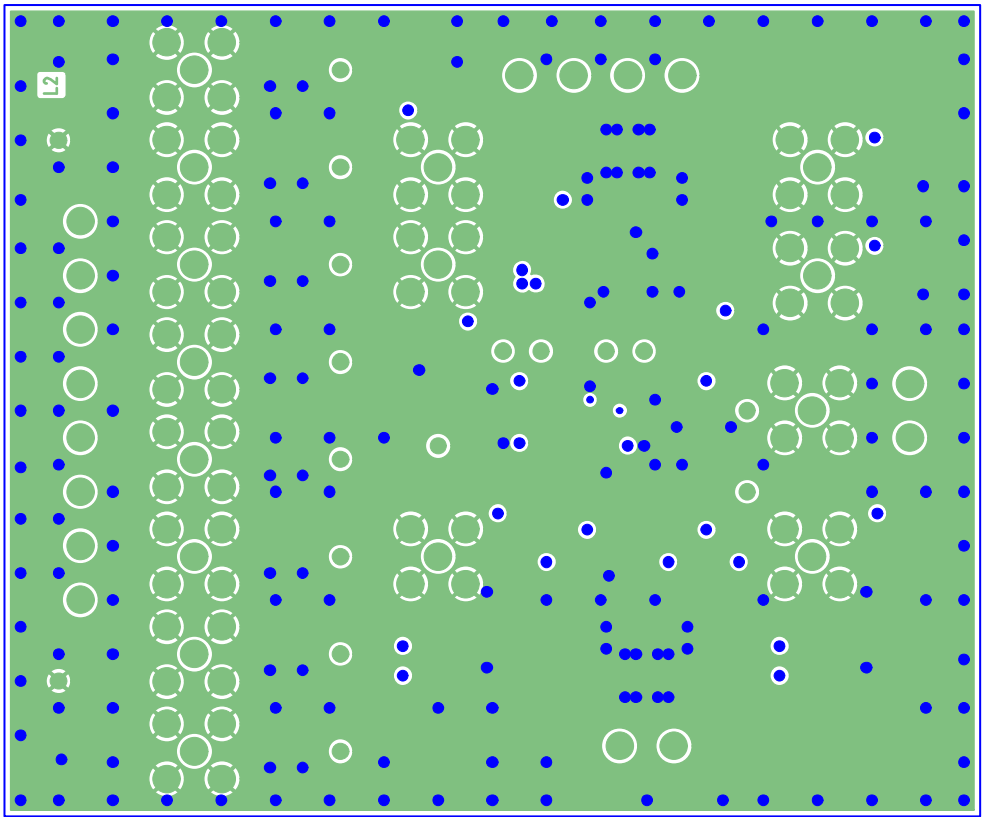

Figure 8. EVAL-ADG5248FEBZ Layer 2

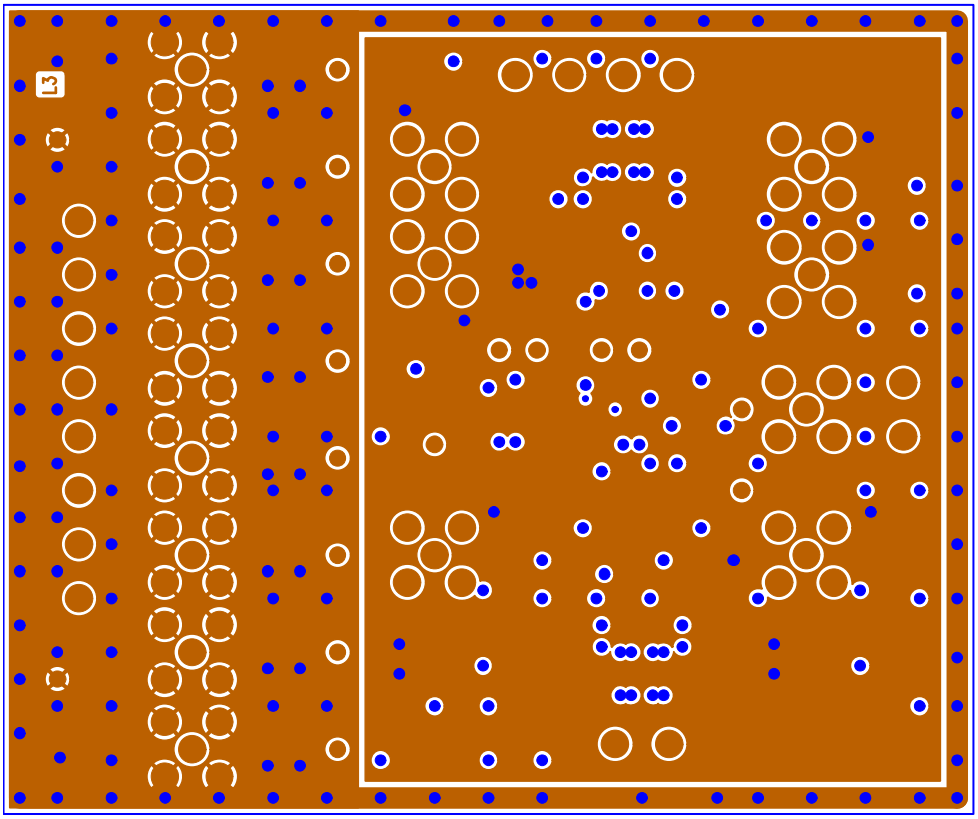

Figure 9. EVAL-ADG5248FEBZ Layer 3

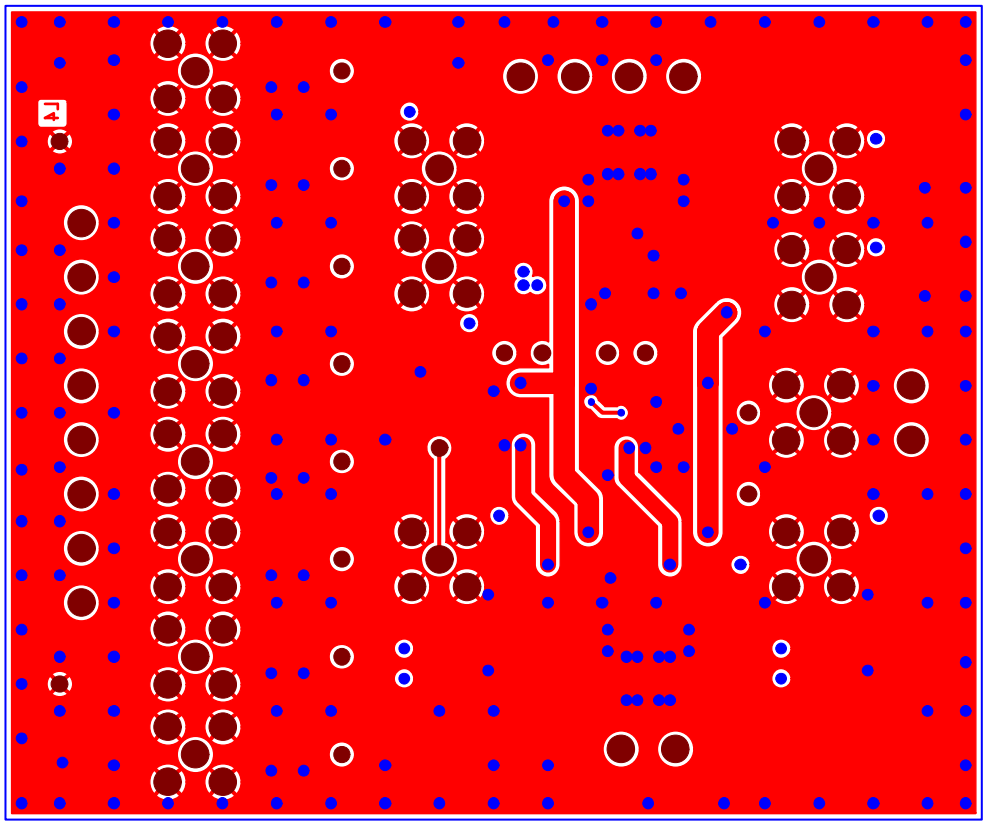

Figure 10. EVAL-ADG5248FEBZ Bottom Layer

BILL OF MATERIALS

Table. 3

Reference Designator	Description	Part Number	Stock Code
A0/F0, A1/F1, A2, EN/F2	50 Ω straight SMB jacks	SMB1251B1-3GT30G-50	FEC 1111349
C1 to C3, C6, C9, C13 to C15	50 V, X7R, multilayer ceramic capacitors, 0603 size, 0.1 µF	GRM188R71H104KA93D	FEC 882-0023
C4, C5, C11, C12	50 V tantalum capacitors, D size, 10 µF	TAJD106K050RNJ	FEC 143-2387
C7, C8	Ceramic multilayer capacitors, 4.7 µF	C2012X5R1H475K125AB	FEC 2346932
D1	50 Ω SMB socket	SMB1251B1-3GT30G-50	Do not insert
FF, SF	50 Ω straight SMB jacks	SMB1251B1-3GT30G-50	FEC 1111349
GND1, GND2	Black test points	20-2137	FEC 873-1128
J1	8-pin terminal block (5 mm pitch)	CTB5000/8	FEC 9633014
J2, J4	2-pin terminal blocks (5 mm pitch)	CTB5000/2	FEC 151789
J3	4-pin terminal block (5 mm pitch)	CTB5000/4	FEC 151791
LED1, LED3	LEDs, SMD green, 0805	KP-2012SGC	FEC 1318243
LED2, LED4	LEDs, SMD red, 0805	KP-2012SRC-PRV	FEC 1318244
Q1 to Q4	Transistors, N-MOSFET, 60 V, 0.23 A, SOT-23	BSS138N	FEC 115-6434
R1 to R3, R7 to R9, R12, R13, R16, R19, R23, R28, R37, R49, R50, R54 to R57	Resistors, 0603, 1%, 0 Ω	MC0063W06030R	FEC 9331662
R4 to R6, R10, R11, R17, R22, R24 to R27, R29, R30 to R33, R43 to R45	SMD resistors, 0603	Not applicable	Do not insert
R14, R36, R47, R48	Resistors, 300 Ω, 0.1 W, 1%, 0805	MC01W08051300R	FEC 9332987
R15, R38, R46, R51 to R53	Resistors, 1 kΩ, 0.063 W, 1%, 0603	MC0063W060311K	FEC 9330380
R18, R20, R35, R39	Resistors, 0805, 1%, 0 Ω	MC01W08050R	FEC 9333681
R21, R34, R40 to R42	SMD resistors, 0805	Not applicable	Do not insert
S1 to S8	50 Ω, SMB sockets	SMB1251B1-3GT30G-50	Do not insert
SW1 to SW4	SPDT, SMT slide switches	CAS-120TA	Digi-Key CAS120JCT-ND
T1 to T9	Red test points	20-313137	FEC 873-1144
T_A0 to T_A2, T_EN, T_FF, T_SF	Red test points	20-313137	FEC 8731144
U1	Fault protection and detection, 1 pC Q_{INJ}, 8:1 multiplexer	ADG5248FBRUZ	ADG5248FBRUZ
U2	Linear regulator, 5.0 V, LDO	ADP7142AUJZ-5.0	ADP7142AUJZ-5.0-R7

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG13184-0-5/16(A)