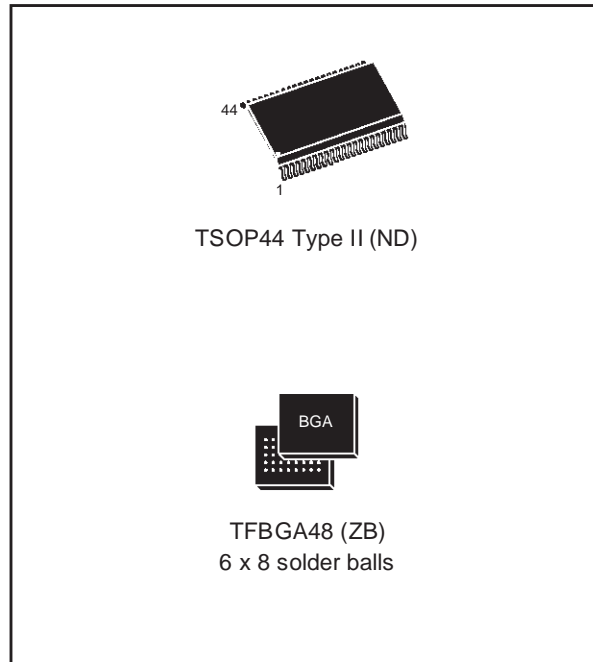# M68AW128M
M68AW128ML

2 Mbit (128K x16) 3.0V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 128K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 1.0V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages

TSOP44 Type II (ND)

TFBGA48 (ZB)
6 x 8 solder balls

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M68AW128M is a 2 Mbit (2,097,152 bit) CMOS SRAM, organized as 131,072 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an au-

tomatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW128M is available in TFBGA48 (0.75 mm pitch) and in TSOP44 Type II packages.

Figure 2. Logic Diagram

Table 1. Signal Names

A0-A16	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TSOP Connections

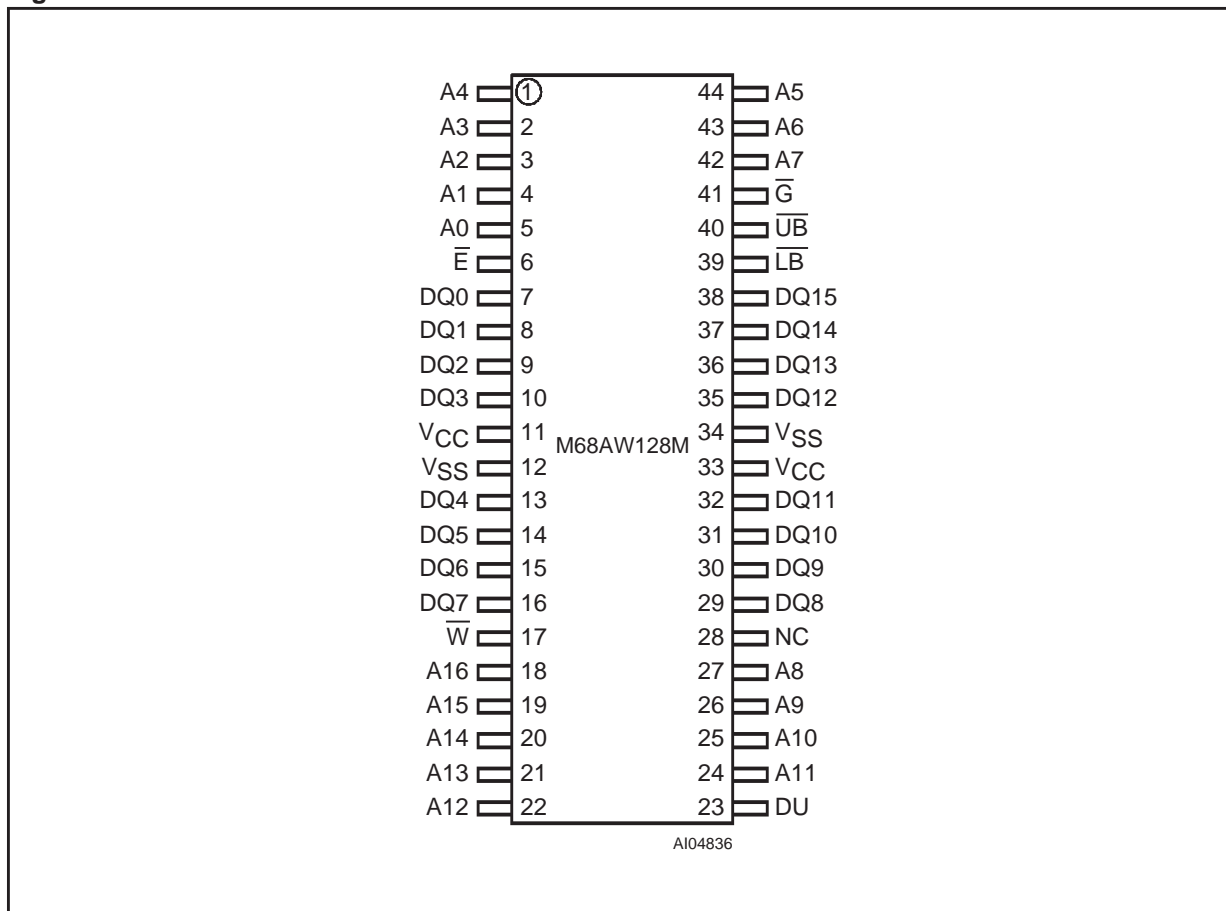| Left	Pin		Pin	Right
A4	1		44	A5
A3	2		43	A6
A2	3		42	A7
A1	4		41	$\overline{G}$
A0	5		40	$\overline{UB}$
$\overline{E}$	6		39	$\overline{LB}$
DQ0	7		38	DQ15
DQ1	8		37	DQ14
DQ2	9		36	DQ13
DQ3	10		35	DQ12
V_{CC}	11	M68AW128M	34	V_{SS}
V_{SS}	12		33	V_{CC}
DQ4	13		32	DQ11
DQ5	14		31	DQ10
DQ6	15		30	DQ9
DQ7	16		29	DQ8
$\overline{W}$	17		28	NC
A16	18		27	A8
A15	19		26	A9
A14	20		25	A10
A13	21		24	A11
A12	22		23	DU

AI04836

Figure 4. TFBGA Connections (Top view through package)
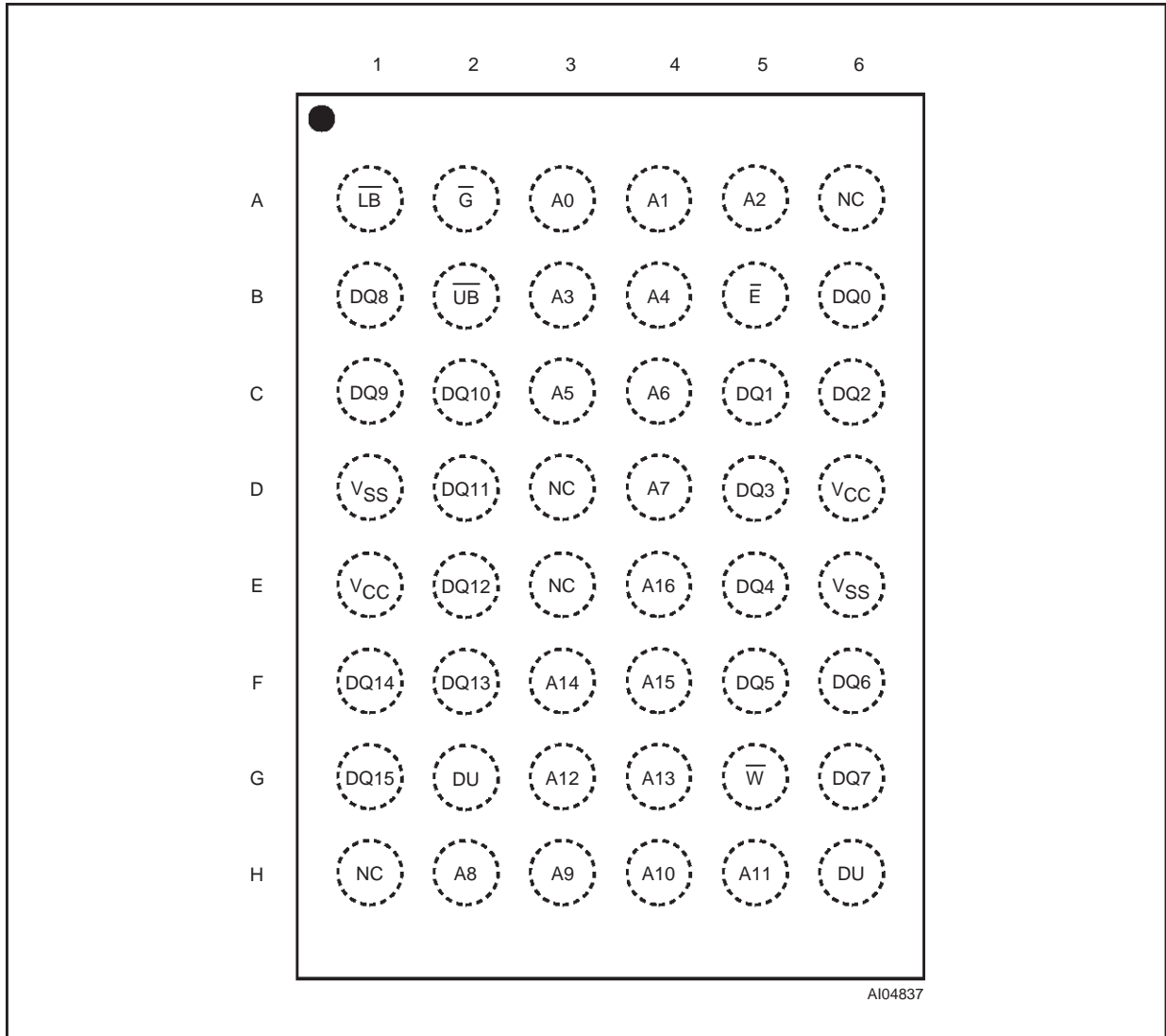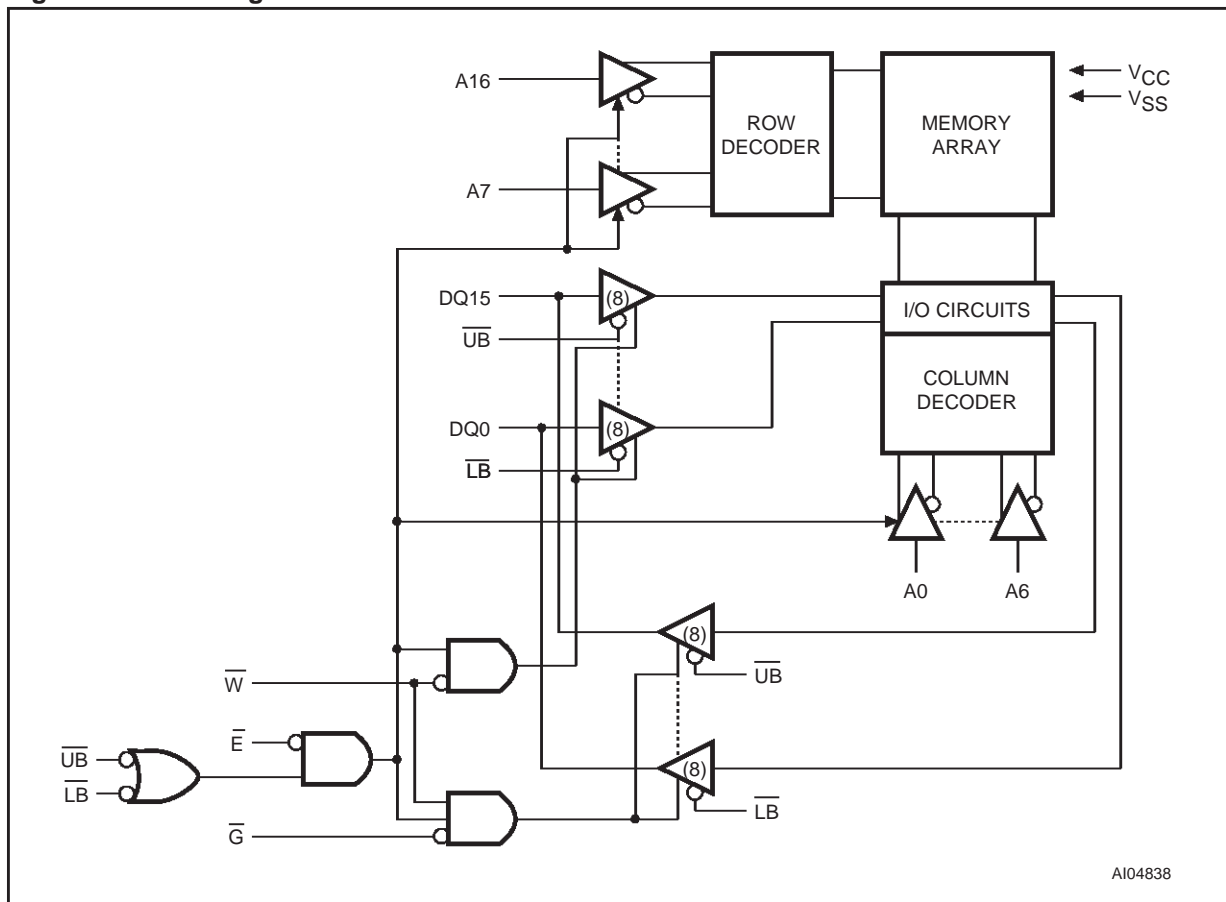

AI04837

Figure 5. Block Diagram

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-plied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_O [1]	Output Current	20	mA
T_A	Ambient Operating Temperature	−55 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
V_{CC}	Supply Voltage	−0.5 to 4.6	V
V_{IO} [2]	Input or Output Voltage	−0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 3.6V only.
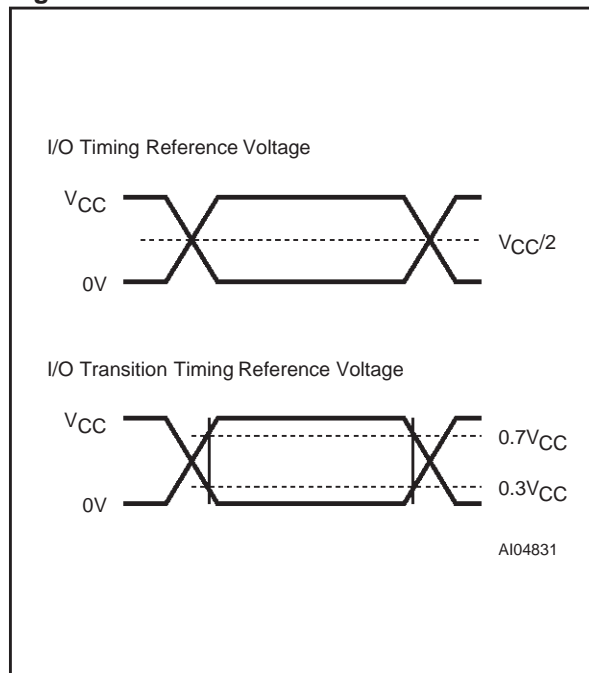
DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure- ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter	M68AW128M
V_{CC} Supply Voltage	2.7 to 3.6V
Ambient Operating Temperature	–40 to 85°C
Load Capacitance (C_L)	30 or 5pF
Output Circuit Protection Resistance (R_1)	1.10kΩ
Load Resistance (R_2)	1.55kΩ
Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V_{CC}
Input and Output Timing Ref. Voltages	$V_{CC}/2$
Input and Output Transition Timing Ref. Voltages	$V_{OL} = 0.3V_{CC}$; $V_{OH} = 0.7V_{CC}$

Figure 6. AC Measurement I/O Waveform

Figure 7. AC Measurement Load Circuit

Table 4. Capacitance

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	$V_{IN} = 0V$		6	pF
C_{OUT}[3]	Output Capacitance	$V_{OUT} = 0V$		8	pF

Note: 1. Sampled only, not 100% tested.
2. At $T_A = 25°C$, f = 1 MHz, $V_{CC} = 3.0V$.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CC1} [1]	Operating Supply Current	$V_{CC} = 3.6V$, f = $1/t_{AVAV}$, $I_{OUT} = 0mA$		7	15	mA
I_{CC2}	Operating Supply Current	$V_{CC} = 3.6V$, f = 1MHz, $I_{OUT} = 0mA$		1	2	mA
I_{SB} [2]	Standby Supply Current CMOS (M68AW128M)	$V_{CC} = 3.6V$, $\overline{E} \geq V_{CC} -0.15V$, f = 0		15		µA
	Standby Supply Current CMOS (M68AW128ML)			1		µA
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	−1		1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ [3]	−1		1	µA
V_{IH}	Input High Voltage	$V_{CC} = 2.7V$	2.2		V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	$V_{CC} = 2.7V$	−0.5		0.8	V
V_{OH}	Output High Voltage	$V_{CC} = 2.7V$, $I_{OH} = −100µA$	2.4			V
V_{OL}	Output Low Voltage	$V_{CC} = 2.7V$, $I_{OL} = 2.1mA$			0.4	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. All other Inputs at $V_{IL} \leq 0.15V$ or $V_{IH} \geq V_{CC} -0.15V$.
3. Output disabled.

OPERATION

The M68AW128M has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E}$ = High) or $\overline{LB}$ and $\overline{UB}$ are de-asserted ($\overline{LB}$ and $\overline{UB}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

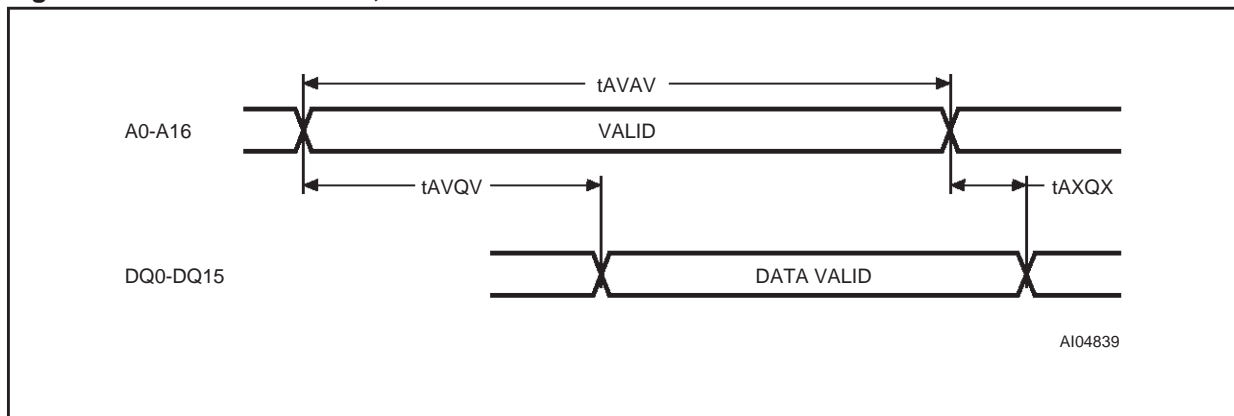| Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected/Power-down	V_{IH}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected/Power-down	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	X	V_{IH}	V_{IL}	X	Hi-Z	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	X	V_{IH}	X	V_{IL}	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})

Note: 1. X = V_{IH} or V_{IL}.

Read Mode

The M68AW128M is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 2,097,152 locations in the static memory array, specified by the 17 address inputs. Valid data will be available 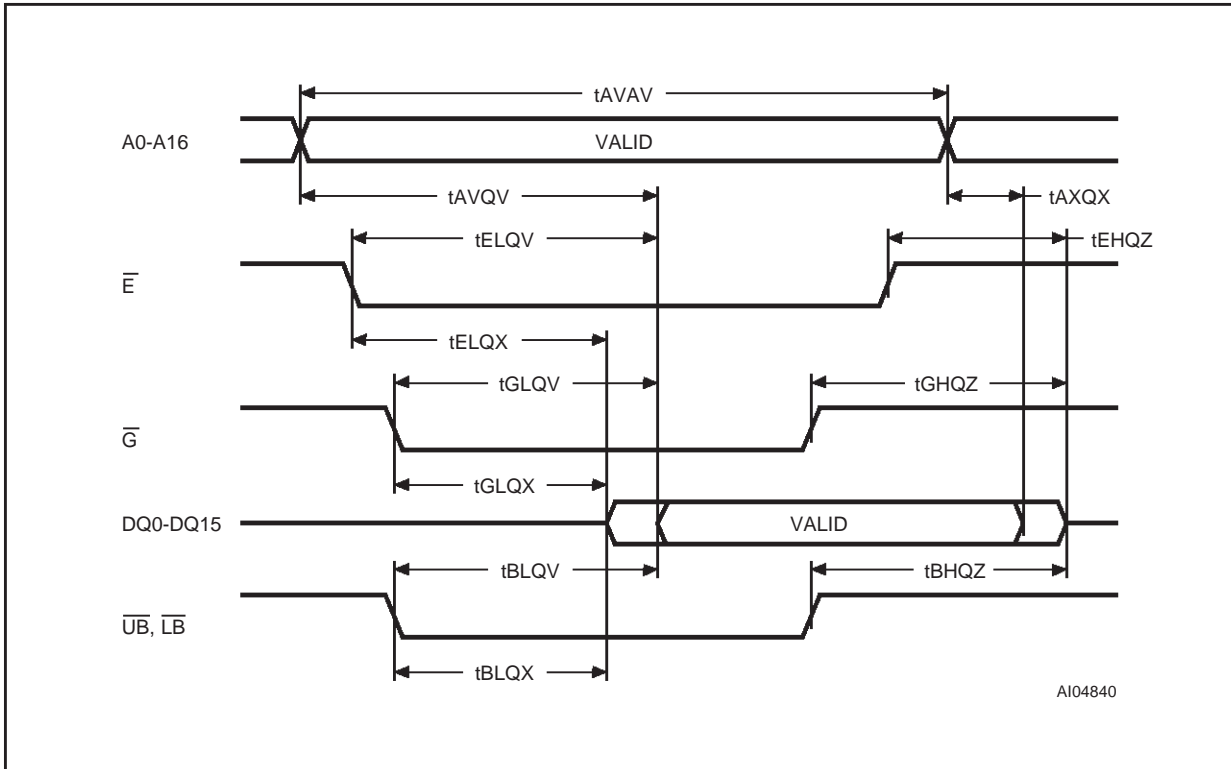at the eight or sixteen output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, t_{GLQX} and t_{BLQX} but data lines will always be valid at t_{AVQV}.

Figure 8. Address Controlled, Read Mode AC Waveforms

Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High, $\overline{UB}$ = Low and/or $\overline{LB}$ = Low.

Figure 9. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.

AI04840

Note: Write Enable ($\overline{W}$) = High.

Figure 10. Chip Enable or $\overline{UB}/\overline{LB}$ Controlled, Standby Mode AC Waveforms

AI03856

Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AW128M		Unit
			55	**70**	
t_{AVAV}	Read Cycle Time	Min	55	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	55	70	ns
t_{AXQX}	Data hold from address change	Min	10	10	ns
t_{BHQZ} [1, 2]	Upper/Lower Byte Enable High to Output Hi-Z	Max	20	20	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid	Max	55	70	ns
t_{BLQX}	Upper/Lower Byte Enable Low to Output Transition	Min	5	10	ns
t_{EHQZ} [1, 2]	Chip Enable High to Output Hi-Z	Max	20	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	55	70	ns
t_{ELQX}	Chip Enable Low to Output Transition	Min	10	10	ns
t_{GHQZ} [1, 2]	Output Enable High to Output Hi-Z	Max	20	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	20	35	ns
t_{GLQX}	Output Enable Low to Output Transition	Min	5	5	ns
t_{PD}	Chip Enable or $\overline{UB}/\overline{LB}$ High to Power Down	Max	55	70	ns
t_{PU}	Chip Enable or $\overline{UB}/\overline{LB}$ Low to Power Up	Min	0	0	ns

Note: 1. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
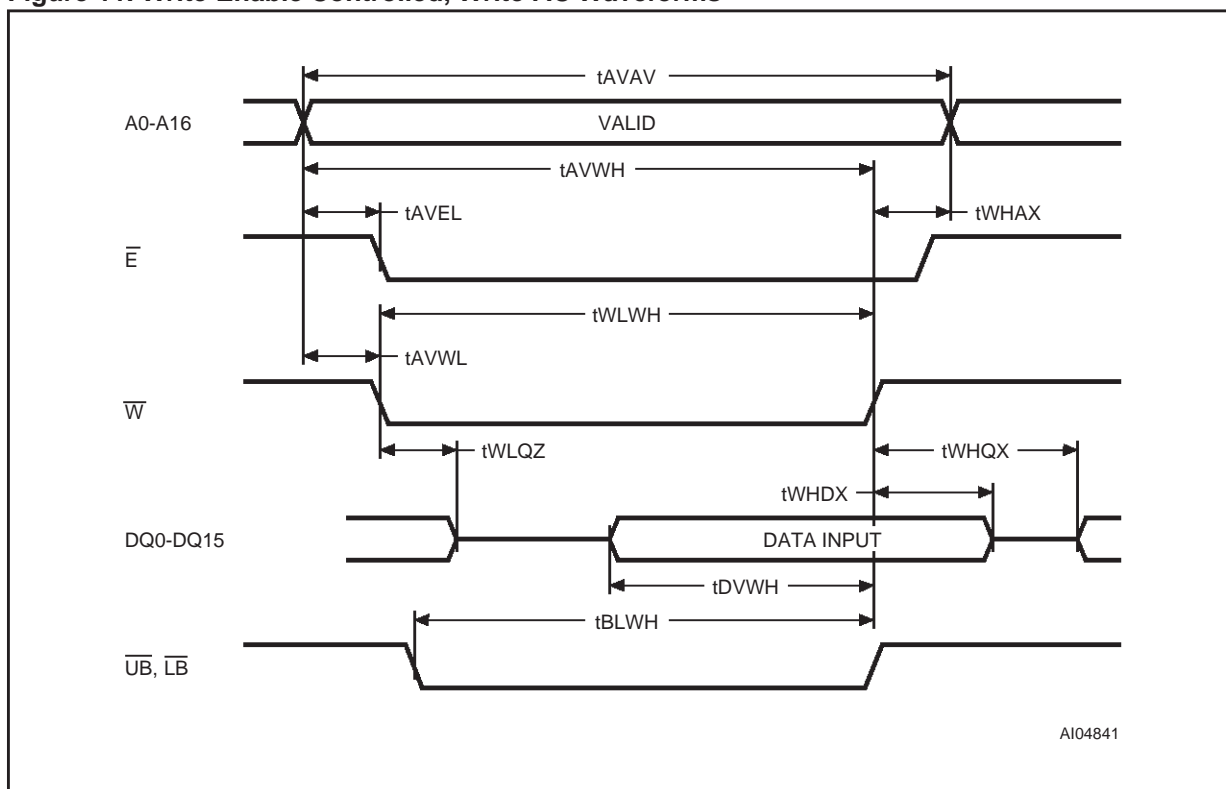   2. C_L = 5pF.

Write Mode

The M68AW128M is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E}$ ($\overline{W}$) is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ ($\overline{E}$)'s falling edge. When $\overline{E}$ and $\overline{W}$ are Low, and $\overline{UB} = \overline{LB}$ = High, write cycle begins on the first falling edge of $\overline{UB}$ or $\overline{LB}$. Therefore, address setup time is referenced to Write Enable, Chip Enable or $\overline{UB}/\overline{LB}$ as t_{AVWL}, t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E}$, $\overline{W}$ or $\overline{UB}/\overline{LB}$.

If the Output is enabled ($\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{LB}$ or $\overline{UB}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, or for t_{DVBH} before the rising edge of $\overline{UB}/\overline{LB}$ whichever occurs first, and remain valid for t_{WHDX}, t_{EHDX} and t_{BHDX} respectively.

Figure 11. Write Enable Controlled, Write AC Waveforms
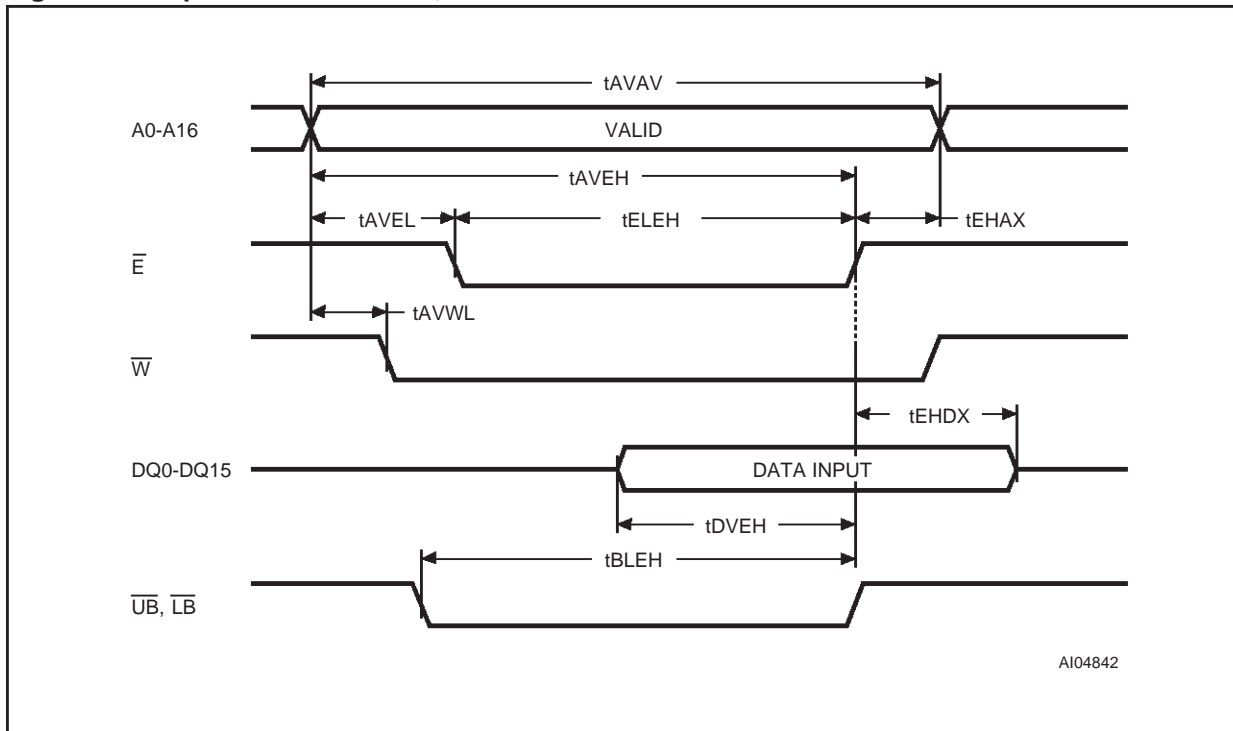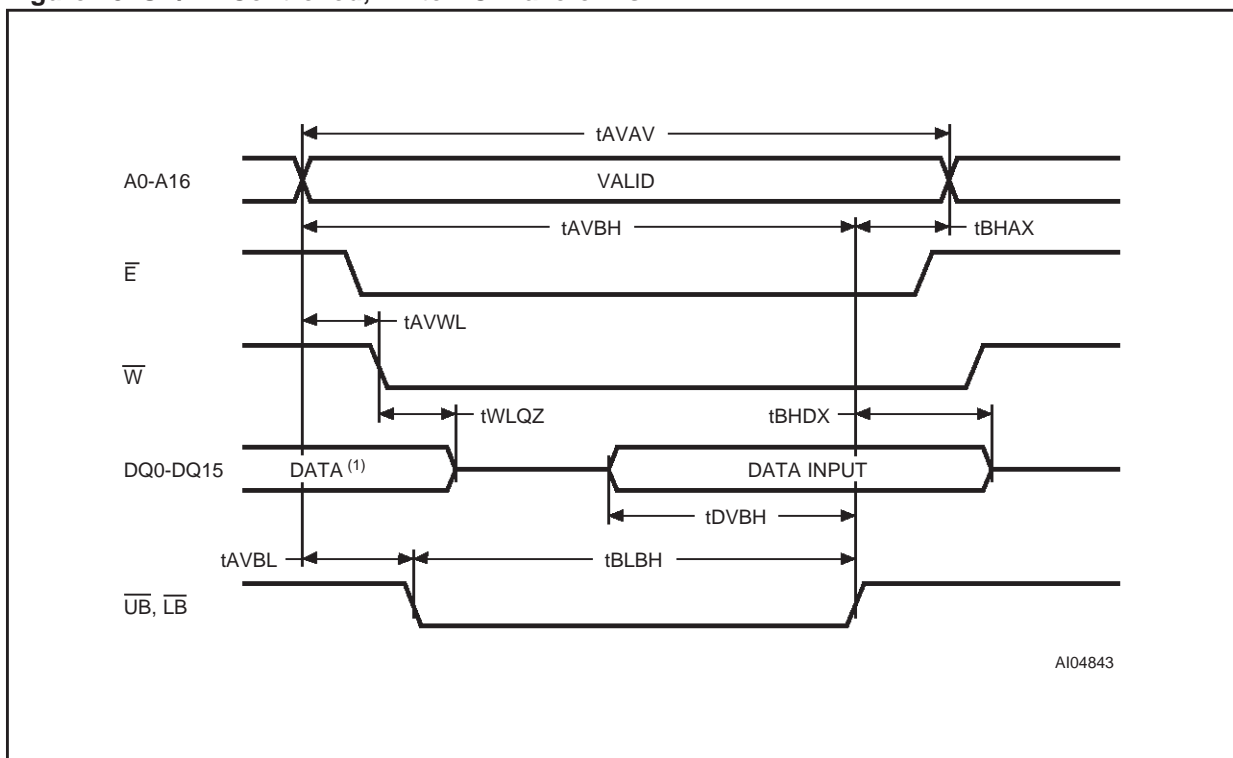
Figure 12. Chip Enable Controlled, Write AC Waveforms

AI04842

Figure 13. UB/LB Controlled, Write AC Waveforms
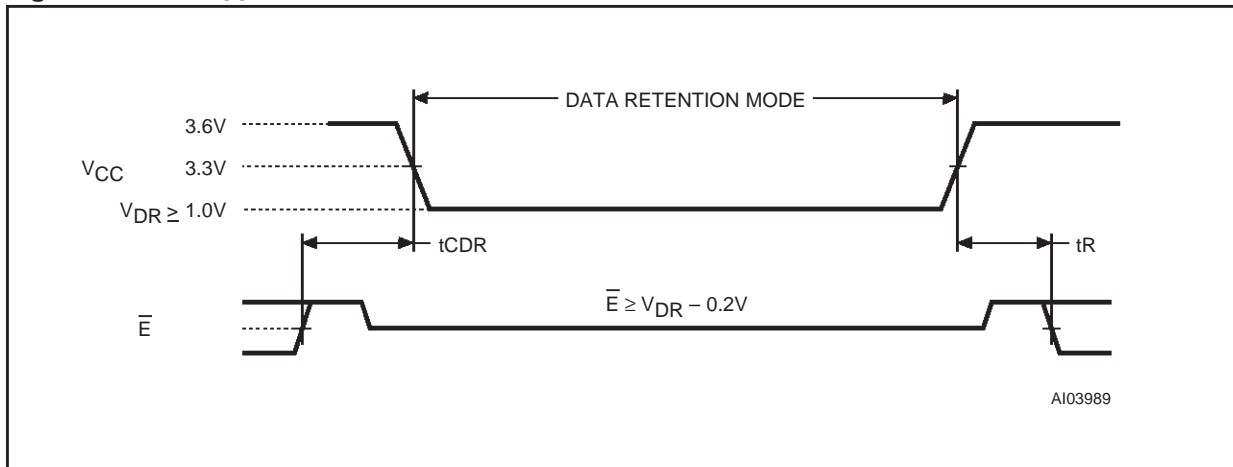

AI04843

Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AW128M 55	70	Unit
t_{AVAV}	Write Cycle Time	Min	55	70	ns
t_{AVBH}	Address Valid to $\overline{LB}$, $\overline{UB}$ High	Min	40	60	ns
t_{AVBL}	Addess Valid to $\overline{LB}$, $\overline{UB}$ Low	Min	0	0	ns
t_{AVEH}	Address Valid to Chip Enable High	Min	40	60	ns
t_{AVEL}	Address valid to Chip Enable Low	Min	0	0	ns
t_{AVWH}	Address Valid to Write Enable High	Min	40	60	ns
t_{AVWL}	Address Valid to Write Enable Low	Min	0	0	ns
t_{BHAX}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	Min	0	0	ns
t_{BHDX}	$\overline{LB}$, $\overline{UB}$ High to Input Transition	Min	0	0	ns
t_{BLBH}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	Min	40	60	ns
t_{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	Min	40	60	ns
t_{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	Min	40	60	ns
t_{DVBH}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	Min	20	25	ns
t_{DVEH}	Input Valid to Chip Enable High	Min	20	25	ns
t_{DVWH}	Input Valid to Write Enable High	Min	20	25	ns
t_{EHAX}	Chip Enable High to Address Transition	Min	0	0	ns
t_{EHDX}	Chip enable High to Input Transition	Min	0	0	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	Min	40	60	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	0	ns
t_{WHDX}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHQX} [1]	Write Enable High to Output Transition	Min	5	5	ns
t_{WLQZ} [1,2]	Write Enable Low to Output Hi-Z	Max	20	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	Min	40	50	ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.
2. C_L = 5pF.

Figure 14. Low V$_{CC}$ Data Retention AC Waveforms

Table 9. Low V$_{CC}$ Data Retention Characteristics

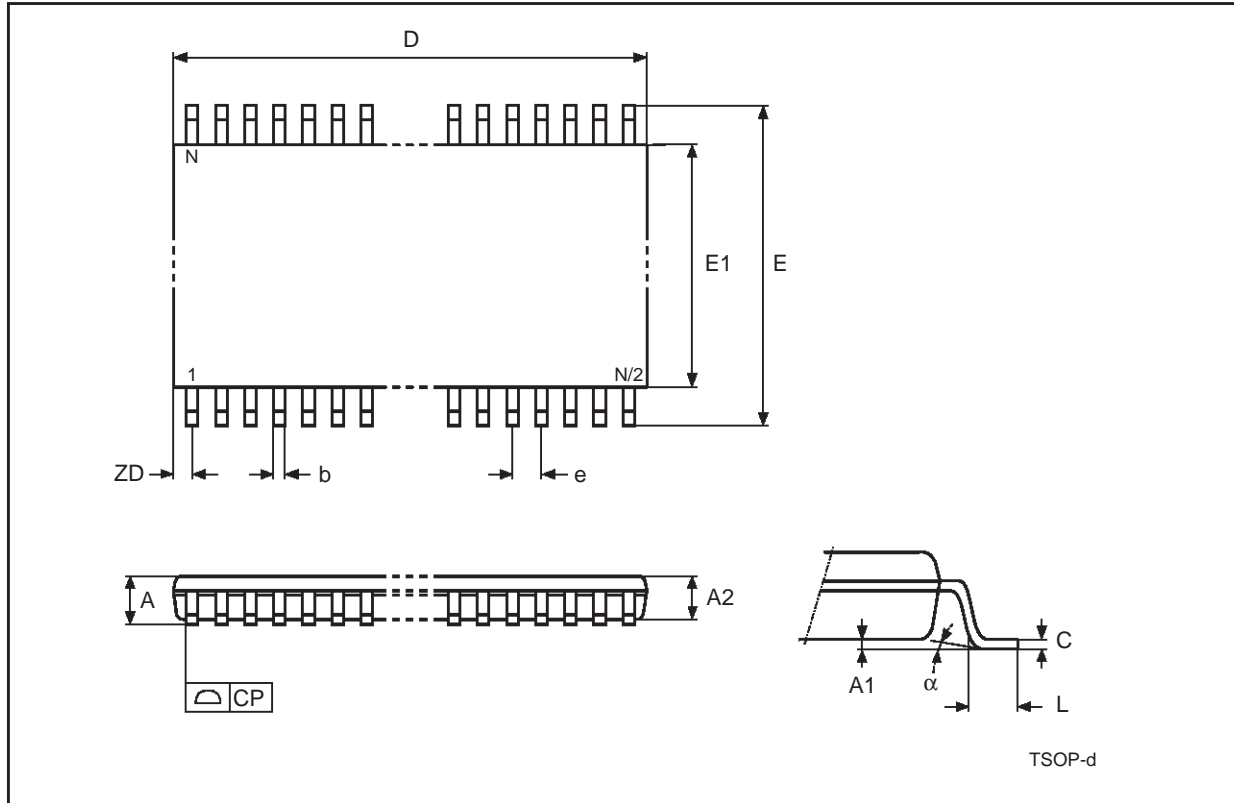| Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I$_{CCDR}$ [1]	Supply Current (Data Retention) (M68AW128M)	V$_{CC}$ = 1.0V, $\overline{E}$ ≥ V$_{CC}$ −0.3V, f = 0 [3]		10	20	µA
	Supply Current (Data Retention) (M68AW128ML)	V$_{CC}$ = 1.0V, $\overline{E}$ ≥ V$_{CC}$ −0.3V, f = 0 [3]		0.1	1	µA
t$_{CDR}$ [1,2]	Chip Deselected to Data Retention Time	$\overline{E}$ ≥ V$_{CC}$ −0.3V, f = 0	t$_{AVAV}$			ns
t$_R$ [2]	Operation Recovery Time		0			ns
V$_{DR}$ [1]	Supply Voltage (Data Retention)	$\overline{E}$ ≥ V$_{CC}$ −0.3V, f = 0	1.0		3.6	V

Note: 1. All other Inputs at V$_{IH}$ ≥ V$_{CC}$ −0.2V or V$_{IL}$ ≤ 0.2V.
2. See Figure 14 for measurement points. Guaranteed but not tested. t$_{AVAV}$ is Read cycle time.
3. No input may exceed V$_{CC}$ +0.3V.

PACKAGE MECHANICAL

Figure 15. TSOP44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Outline
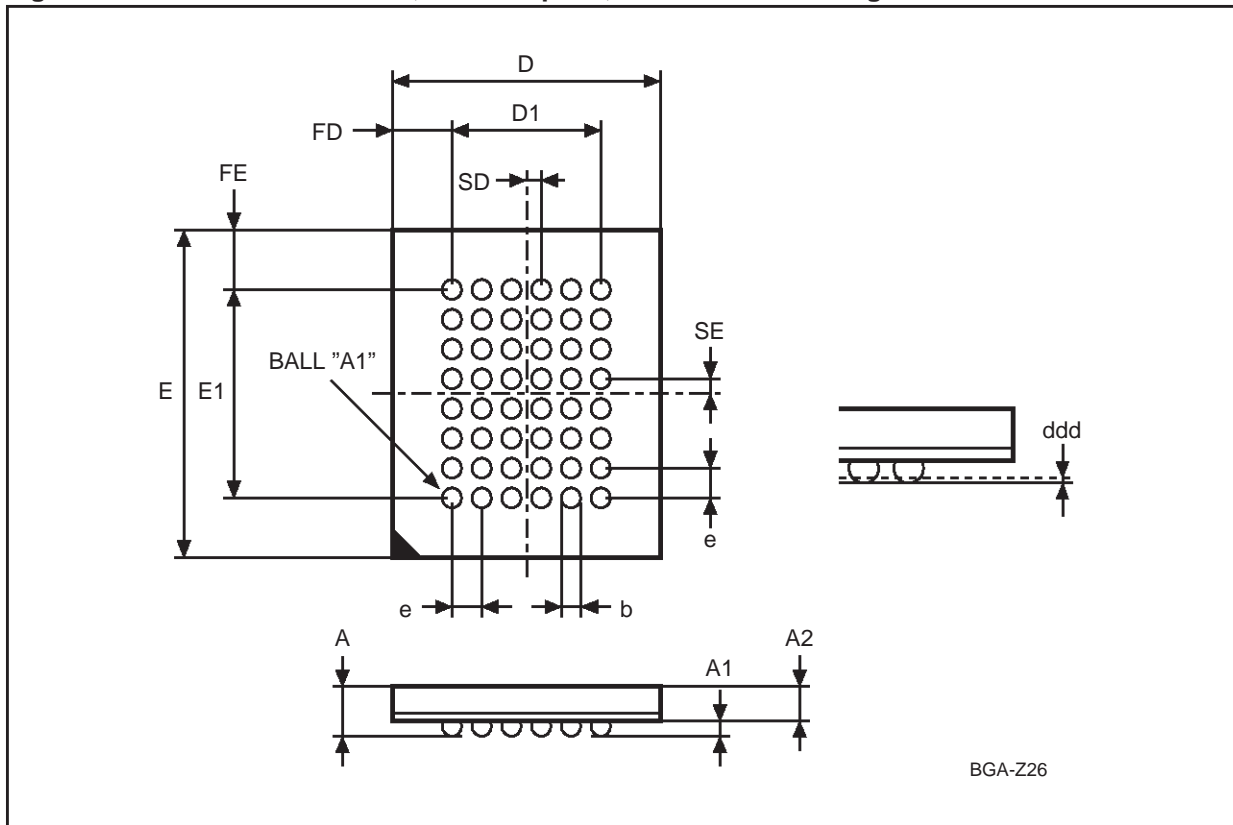

Note: Drawing is not to scale.

Table 10. TSOP 44 Type II - 44 lead Plastic Thin Small Outline Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
b	0.350			0.0138		
c		0.120	0.210		0.0047	0.0083
D	18.410	–	–	0.7248	–	–
e	0.800	–	–	0.0315	–	–
E	11.760	–	–	0.4630	–	–
E1	10.160	–	–	0.4000	–	–
L	0.500	0.400	0.600	0.0197	0.0157	0.0236
ZD	0.805	–	–	0.0317	–	–
alfa		0	5		0	5
CP			0.100			0.0039
N	44			44		

Figure 16. TFBGA48 - 6 x 8 balls, 0.75 mm pitch, Bottom View Package Outline
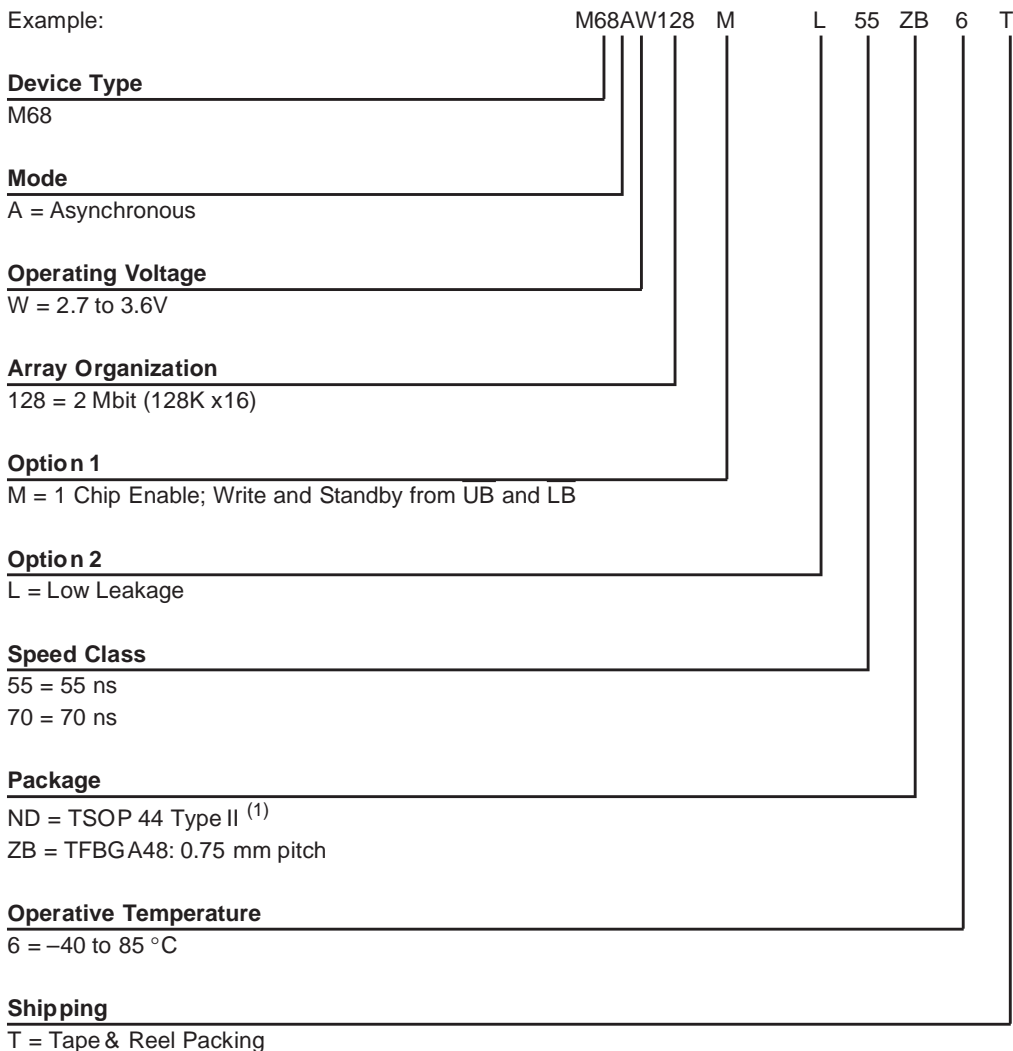

BGA-Z26

Note: Drawing is not to scale.

Table 11. TFBGA48 - 6 x 8 balls, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M68AW128   M   L   55   ZB   6   T

Device Type
M68

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.6V

Array Organization
128 = 2 Mbit (128K x16)

Option 1
M = 1 Chip Enable; Write and Standby from UB and LB

Option 2
L = Low Leakage

Speed Class
55 = 55 ns
70 = 70 ns

Package
ND = TSOP 44 Type II [1]
ZB = TFBGA48: 0.75 mm pitch

Operative Temperature
6 = −40 to 85 °C

Shipping
T = Tape & Reel Packing

Note: 1. Package option available on request. Please contact STMicroelectronics local Sales Office.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 13. Document Revision History

Date	Version	Revision Details
July 2001	-01	First Issue