

Keywords: Leaded packages, SMT, PCB design, SOIC, TSSOP, QSOP, SC70, SOT, SOP, QFP

APPLICATION NOTE 6412

# SMT ASSEMBLY AND PCB DESIGN GUIDELINES FOR LEADED PACKAGES

*Abstract: This application note provides the PCB design and SMT assembly guidelines for Maxim Integrated's leaded packages (SOIC, TSSOP, QSOP, QFP, SC70, SOP, SOT, etc.).*

## Introduction

Leaded packages are surface-mount integrated circuit (IC) packages, including such types as quad flat package (QFP), small outline integrated circuit (SOIC), thin shrink small-outline package (TSSOP), small outline transistor (SOT), SC70, etc. The standard form is a flat rectangular or square body, with leads extending from two or all four sides. The leads are formed in a gull wing shape to allow solid footing during assembly to a PCB. Standard Pb-free lead finish is matte tin. Connection is made through the leads of the package, which can be directly soldered onto the PCB. When an exposed pad is provided in some packages for thermal enhancement purposes, the exposed pad should be directly soldered onto the PCB. **Figure 1** shows the cross-section profile of a leaded package.

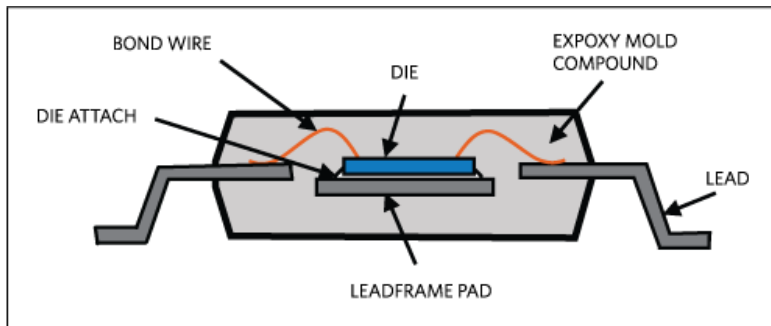


Figure 1. Cross-section view of leaded package.

## Package Outlines

Package information is available on our website at [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Users can review package outline drawings specific to a package type or package code.

## PCB Design

For PCB pad design: a well-designed and manufactured printed circuit board (PCB) is required for optimum manufacturing yields and product performance. Two types of land patterns are used for surface-mount devices: 1) solder mask-defined (SMD) pads have solder mask openings that are smaller than metal pads, and 2) nonsolder mask-defined (NSMD) pads have solder mask openings that are larger than the metal pads. Maxim recommends the use of NSMD pads because they provide a larger metal area for the solder to anchor to the edges of the metal pads. NSMD improves the solder joint reliability. Only one type of a pad (NSMD or SMD) and one type of pad surface finish should be used at a given footprint. **Figure 2** illustrates the NSMD and SMD land pattern design.

Land pattern design should follow Maxim's 90-xxxx series documents corresponding to the specific package code.

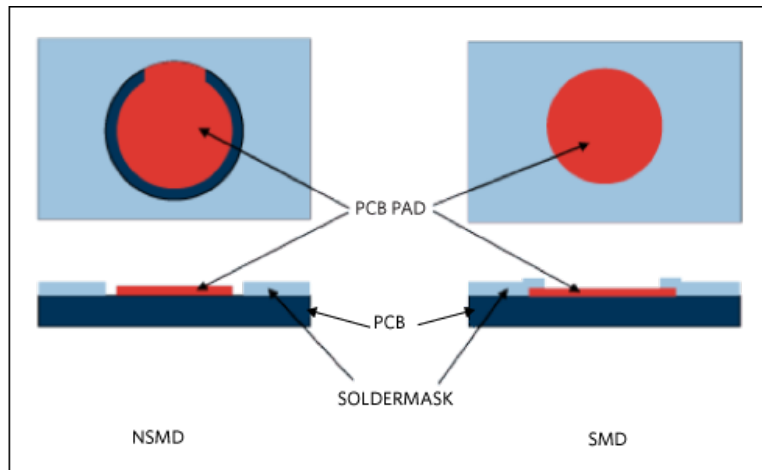


Figure 2. Illustration of NSMD and SMD land pad patterns.

### PCB Design for Exposed Pads (Thermal Pads)

Thermal pads on the PCB should be designed to take advantage of the exposed pads of the packages provided. For a single-layer board, a thermal pad should be connected to a large surface pad, so that heat can be dissipated through the surface pad. For a multiple-layer board, thermal via(s) should be placed under the thermal pad, so that heat can be dissipated to other metal layers to take advantage of metals in those layers. The thermal via(s) design should be optimized based on PCB manufacturer capability and other design limitations.

### PCB Surface Finish

Organic solderability preservative (OSP), electroless nickel immersion gold (ENIG), electrolytic nickel gold, electroless nickel electroless palladium immersion gold (ENEPIG), immersion silver, and immersion tin finishes are used in the industry. OSP and ENIG are recommended for applications that require drop test reliability.

### Stencil Design Guidelines

The stencil thickness and pattern geometry determine the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform solder reflow. Stencils are usually made of stainless steel.

- Stencil thickness: 4- or 5-mil thick stencil is recommended for 0.50mm pitch packages. Package pitches > 0.65mm can accommodate a 6-mil thick stencil.
- Stencil fabrication: Laser-cut with electropolish for better release than the regular laser-cut stencil.
- Stencil aperture: Tolerances must be tightly controlled.
- Walls of the apertures should be smooth, with rounded corners and a trapezoidal cross-section enhance the release of solder paste from the aperture.

### Stencil Design for Exposed Pads (Thermal Pads)

The exposed pad solder land can be segmented into a pad array. The pad array should be created by segmentation of a full copper area by solder mask webbing. The segmented PCB design facilitates the solder paste flux out gassing during reflow, thereby promoting a lower voids percentage of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment. **Figure 3** shows an example of a solder mask design for an exposed pad.

#### Design Recommendation:

**Design Recommendation:**

- 60% to 80% solder paste coverage
- Rounded corners to minimize solder paste clogging
- Positive tape with bottom opening larger than the top

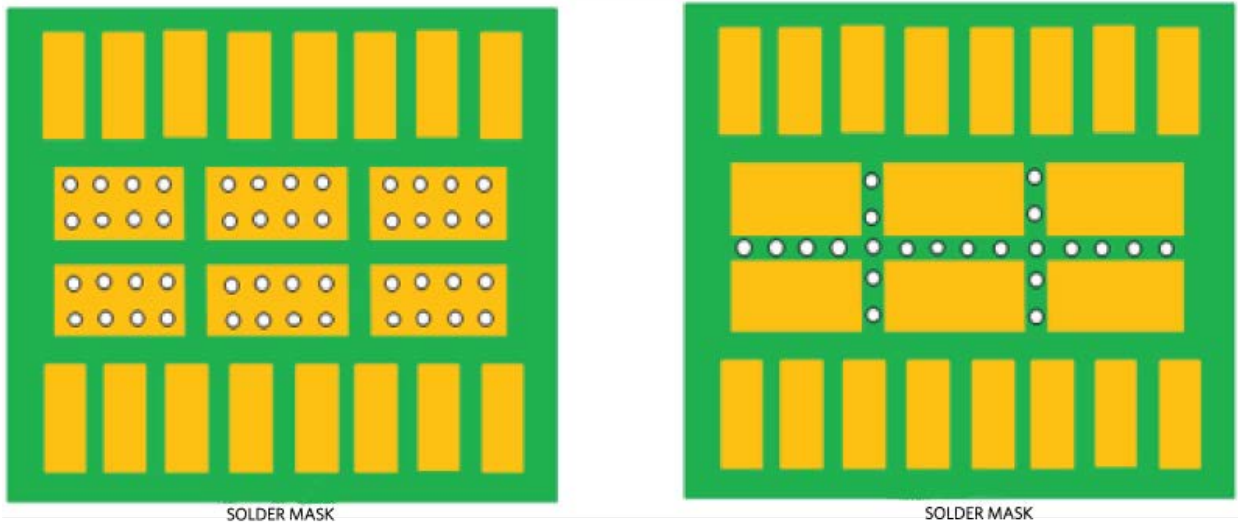


Figure 3. Example of solder mask design for exposed pad.

**Solder Paste**

Solder paste is one of the most important materials in the SMT assembly process. In general, it is recommended to use a no-clean solder paste. However, the end user should evaluate their entire process and usage to ensure desired results. A Type 3 (or finer) solder paste is recommended for 0.5mm pitch printing. Nitrogen purge is recommended during solder reflow.

**Cleaning Requirements**

If a low residue, no-clean solder paste is used, PCB cleaning is not required. However, with different types of no-clean solder pastes available, Maxim recommends application-specific evaluations to check if any remaining residue needs to be removed from the boards.

**Reflow**

Maxim leaded packages are compatible with all industry-standard solder reflow processes. As with all surface-mount devices, it is important that profiles be checked on all new board designs. Additionally, if there are tall components mixed on the board, the profile must be checked at different locations on the board. Component temperatures may vary due to surrounding components, locations of parts on the PCB, and package densities. The reflow profile guidelines are based on the temperature at the actual lead to PCB land pad solder-joint location. The actual temperature of the solder joint is often different than the temperature settings in the reflow system. Therefore, Maxim recommends the profiles be checked using thermocouples at the actual solder joint location. A nitrogen force convention oven should be used. Temperature uniformity should be 5°C.

Maxim suggests following the JEDEC recommended reflow profile, J-STD-020E.

Table 1. Recommended Pb-Free Reflow Profile

Profile Feature	Description	Pb-Free assembly Recommendation
$T_{Smin}$	Min Soak Temperature	150°C
$T_{Smax}$	Max Soak Temperature	200°C
$T_S$	Time Between $T_{Smin}$ and $T_{Smax}$	60–120 Seconds
$T_L$	Liquidous Temperature	217°C
$T_L$	Time Above $T_L$	60-150 seconds
$T_P$	Peak Package Body Temperature	260°C
$T_P$	Time Within 5°C of $T_P$	30 Seconds
Ramp-Up Rate ( $T_L$ to $T_P$ )		3°C/Seconds (max)
Ramp-Down Rate ( $T_P$ to $T_L$ )		6°C/Seconds (max)

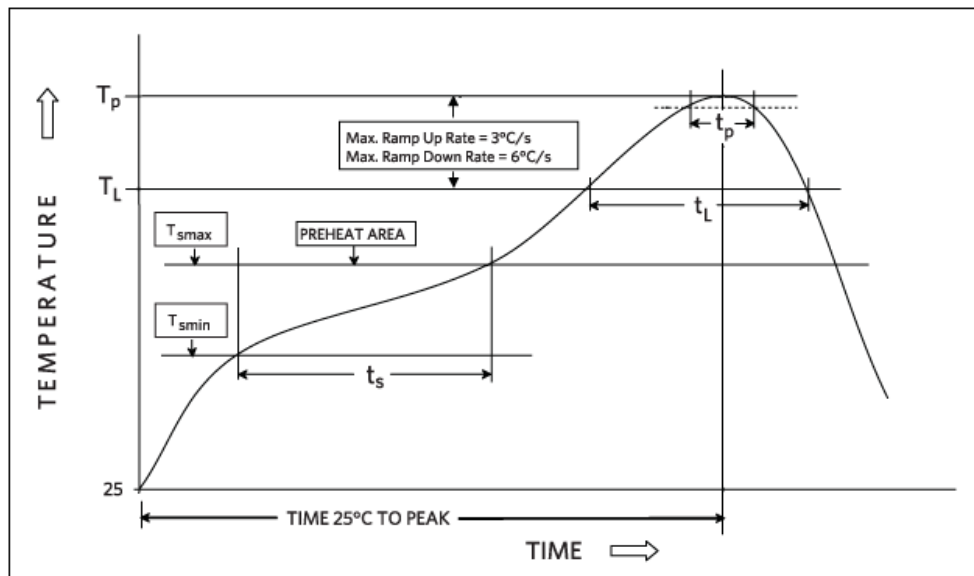


Figure 5. Recommended Pb-Free Reflow profile.

### Inspection

Maxim suggests following the IPC specification for inspection specs. Go to [www.ipc.org](http://www.ipc.org) for more information. Figure 5 shows one example of a well-soldered lead. The solder fillet should be able to be visually inspected at both sides, but not over the solder on top of the leads.

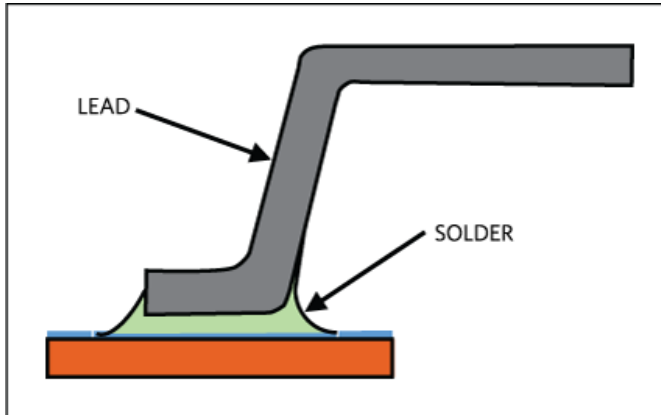


Figure 5. Well-soldered lead on a well-designed PCB.

### Moisture Sensitivity

Maxim leaded packages are classified as JEDEC standard per specification J-STD-020D.

For those packages that only meet MSL3 (typically larger packages and special packages), all parts are baked and dry-packed with desiccants and a humidity indicator card before shipping. If the humidity indicator card has turned pink, or if the parts have been exposed to longer than their floor life, bake the packages +125°C for 48 hours.

Refer to JEDEC specification J-STD-020D for correct use of moisture/reflow sensitive surface-mount devices.

### Rework

The rework quality is not easily controlled. If rework is needed on the parts with soldering defects, Maxim suggests baking the PCB assembly at least 4 hours at +125°C. Use the following steps as minimum:

1. Remove part by unsoldering it from the board. Make sure the heat is locally applied to avoid overheating adjunction components.
2. Remove all the remaining solder on the pads.
3. Clean the board.
4. Apply the solder again by printing with stencil.
5. Place the parts.
6. Reflow.
7. Clean PCB and inspect.

### Pick and Place (P and P)

Conventional placement systems can be employed using either the package outline or the position of the leads as a placement guide. Placement guide using position of the leads tends to be more accurate but slower, and requires a complex vision-processing system. The package outline placement method runs faster, but is less accurate. The contract PCB assembler can determine the most acceptable method to be employed for this process.

### Reference Materials

1. JEDEC Standard J-STD-020E
2. IPC-610
3. IPC-7351
4. Maxim [Application Note 5963](#)

Related Parts		
<a href="#">MAX2204</a>	RF Power Detector	<a href="#">Free Samples</a>
<a href="#">MAX3370</a>	1µA, 2Mbps, Low-Voltage Level Translators in SC70 and µDFN	<a href="#">Free Samples</a>
<a href="#">MAX4729</a>	Low-Voltage 3.5½, SPDT, CMOS Analog Switches	<a href="#">Free Samples</a>
<a href="#">MAX4785</a>	50mA/100mA Current-Limit Switches	<a href="#">Free Samples</a>
<a href="#">MAX9911</a>	200kHz, 4µA, Rail-to-Rail I/O Op Amps with Shutdown	<a href="#">Free Samples</a>

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#### More Information

For Technical Support: <https://www.maximintegrated.com/en/support>

For Samples: <https://www.maximintegrated.com/en/samples>

Other Questions and Comments: <https://www.maximintegrated.com/en/contact>

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Application Note 6412: <https://www.maximintegrated.com/en/an6412>

APPLICATION NOTE 6412, AN6412, AN 6412, APP6412, Appnote6412, Appnote 6412

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