700 MHz, -3 dB Bandwidth; Single SPDT Analog Switch

DESCRIPTION

DG3257 is a low R_{ON}, high bandwidth analog switch configured in single SPDT. It achieves 5 Ω switch on resistance, greater than 700 MHz -3 dB bandwidth with 5 pF load, and a channel to channel crosstalk at -32 dB and isolation at -33 dB. Fabricated with high density sub micro CMOS process, the DG3257 provides low parasitic capacitance, handles bidirectional signal flow with minimized phase distortion. Guaranteed 1.4 V logic high threshold makes it possible to interface directly with low voltage MCUs.

The DG3257 is designed for a wide range of operating voltages from 1.65 V to 5.5 V that can be driven directly from one cell Li-ion battery. On-chip protection circuit protects again fault events when V+ goes zero. Latch up current is 300 mA, as per JESD78, and its ESD tolerance exceeds 6 kV.

Packaged in ultra small µDFN6L (1 mm x 1 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination.

The µDFN6L package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-GE4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL rating. As a further sign of Vishay Siliconix's commitment, the DG3257 is fully RoHS-complaint.

FEATURES

Pb-free

RoHS COMPLIANT

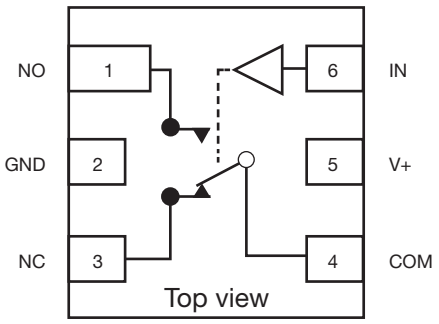
- 1.65 V to 5.5 V single supply operation
- Low resistance: 5 Ω/typ. at 4.2 V
- Switch ON capacitance: 9 pF typical
- -3 dB bandwidth: 700 MHz
- Power down protection
- Signal swing over V+ capable (when signal swing over V+, signal pin current: typically (V_S - 0.6 V)/120 Ω)
- Control logic S pin voltage can go beyond V+
- Break before make switching
- Latch up current: 300 mA (JESD78)
- ESD / HBM: 6 kV,
- ESD / CDM: 1 kV
- TTL/CMOS compatible
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

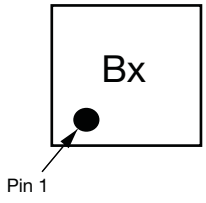
APPLICATIONS

- Smart phones
- Tablet, e-readers
- Camera, audio devices
- Computer and peripherals
- Data storage
- IoT
- Wearable
- Portable healthcare

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

µDFN-6L 1 x 1





Device marking: Bx for DG3257
x = Date / Lot traceability code

ORDERING INFORMATION		
TEMP. RANGE	**PACKAGE**	**PART NUMBER**
-40 °C to +85 °C	µDFN-6L	DG3257DN-T1-GE4

TRUTH TABLE		
IN	NC	NO
0	ON	OFF
1	OFF	ON

PIN DESCRIPTIONS	
PIN NAME	DESCRIPTION
IN	Logic select Input
V+	Power pin
GND	Power ground pin
NC	Normal close data port
NO	Normal open data port
COM	Common data port

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
PARAMETER	CONDITIONS	LIMITS	UNIT
V+, S	Reference to GND	-0.3 to +6	V
COM, NO, NC	Reference to GND	-0.3 to +6	
Maximum continuous switch current		± 50	mA
Maximum pulse switch current	Pulsed at 1 ms, 10 % duty cycle	± 100	
Thermal resistance		407	°C/W
ESD / HBM	EIA / JESD22-A114-A	6000	V
ESD / CDM	EIA /JESD22-C101A	1000	
Temperature			
Operating temperature		-40 to +85	°C
Max. operating junction temperature		150	
Operating junction temperature		125	
Storage temperature		-65 to +150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS V+ = 3 V, V_{INH} = 1.3 V, V_{INL} = 0.5 V OTHERWISE UNLESS SPECIFIED	+25 °C	-40 °C to +85 °C	TYP. [a] / MAX.	UNIT
Analog Switch						
Analog signal range	V_{ANALOG}		0 to 5.5			V
Drain-source on-resistance	$R_{DS(on)}$	V+ = 1.8 V, $V_{NC/NO}$ = 0 V to V+, $I_{S±}$ = 8 mA	28	-	Typ.	Ω
			47	54	Max.	
		V+ = 3 V, $V_{NC/NO}$ = 0.4 V, $I_{S±}$ = 8 mA	7	-	Typ.	
			8	9	Max.	
		V+ = 3.6 V, $V_{NC/NO}$ = 0.4 V, $I_{S±}$ = 8 mA	6	-	Typ.	
			7	8	Max.	
		V+ = 4.2 V, $V_{NC/NO}$ = 0.4 V, $I_{S±}$ = 8 mA	5	-	Typ.	
			6	7	Max.	
		V+ = 5 V, $V_{NC/NO}$ = 0.4 V, $I_{S±}$ = 8 mA	5	-	Typ.	
			5.5	6	Max.	
On-resistance flatness	$R_{flat(on)}$	V+ = 3 V, $V_{NC/NO}$ = 0 V, 1 V, $I_{S±}$ = 8 mA	2	-	Typ.	
			3	6	Max.	
On-resistance matching	$\Delta R_{DS(on)}$	V+ = 2.7 V to 5.5 V, V_S = 0 V to V+, $I_{S±}$ = 8 mA	0.4	-	Typ.	
			0.6	0.8	Max.	
Switch off leakage current	$I_S/I_{d(off)}$	V+ = 5.5 V, V_{COM} = 1 V / 4.5 V, $V_{NC/NO}$ = 4.5 V / 1 V	± 0.2	-	Typ.	nA
			-	± 20	Max.	
Channel on leakage current	$I_{d(on)}$	V+ = 5.5 V, V_{COM} = 1 V / 4.5 V, $V_{NC/NO}$ = open	± 0.2	-	Typ.	
			-	± 20	Max.	
Power down leakage	$I_{COM(PD)}$	V+ = 0 V, V_{COM} = 4.5 V	1	-	Max.	µA

SPECIFICATIONS

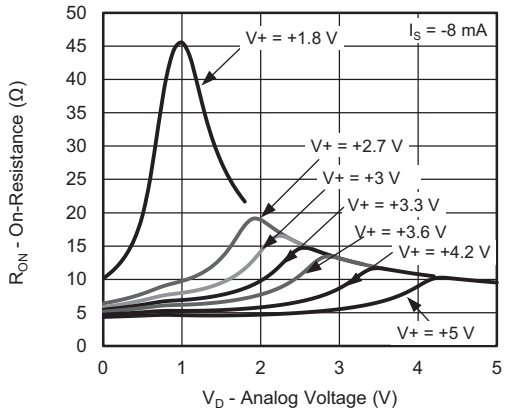
PARAMETER	SYMBOL	TEST CONDITIONS V+ = 3 V, V_{INH} = 1.3 V, V_{INL} = 0.5 V OTHERWISE UNLESS SPECIFIED	+25 °C	-40 °C to +85 °C	TYP. [a] / MAX.	UNIT
Digital Control						
Input voltage high	V_{INH}	V+ = 3 V	-	1.2	Min.	V
		V+ = 5 V	-	1.4	Min.	
Input voltage low	V_{INL}	V+ = 3 V	-	0.45	Max.	
		V+ = 5 V	-	0.5	Max.	
Input leakage	I_{IN}	V+ = 0 V, 5.5 V, V_{IN} = V_{GND} or V+	0.001	-	Typ.	µA
			-	0.23	Max.	
Digital input capacitance	C_{IN}		5.6	-	Typ.	pF
Dynamic Characteristics						
Break-before-make-time	t_{OPEN}	V_{NO} = V_{NC} = 1.5 V; R_L = 300 Ω, C_L = 35 pF	6	-	Typ.	ns
			-	2	Min.	
Turn-on time	t_{ON}	V_{NC} = V_{NO} = V+; R_L = 50 Ω, C_L = 35 pF	17	-	Typ.	
			40	50	Max.	
Turn-off time	t_{OFF}		9	-	Typ.	
			35	45	Max.	
Propagation delay [b]	t_{PD}		100	-	Typ.	ps
Charge injection [b]	Q_{INJ}	C_L = 1 nF, R_{GEN} = 0 Ω, V_{COM} = 1.5 V	4	-	Typ.	pC
Off-isolation [b]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 240 MHz	-33	-	Typ.	dB
Crosstalk [b]	X_{TALK}		-32	-	Typ.	
Insertion loss [b]		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	-0.62	-	Typ.	
Total harmonic distortion + Noise [b]	THD + N	R_L = 600 Ω, V_{PP} = 0.5 V_{p-p}, f = 20 Hz to 20 kHz	0.025	-	Typ.	%
Bandwidth, -3 dB [b]	BW	R_L = 50 Ω, C_L = 5 pF	714	-	Typ.	MHz
Source off capacitance [b]	$C_{S\ (off)}$	f = 240 MHz	3	-	Typ.	pF
Drain on capacitance [b]	$C_{D(on)}$		9	-	Typ.	
Power Requirements						
Power supply range		GND = 0 V	+1.65 / +5.5 min. / max.			V
Power supply current	I+	Digital Inputs 0 V or V+, V+ = 2.7 V to 5.5 V	0.001	-	Typ.	µA
			-	0.4	Max.	
		Digital inputs 1.8 V, V+ = 3 V	1	-	Typ.	
			-	1.5	Max.	

Notes

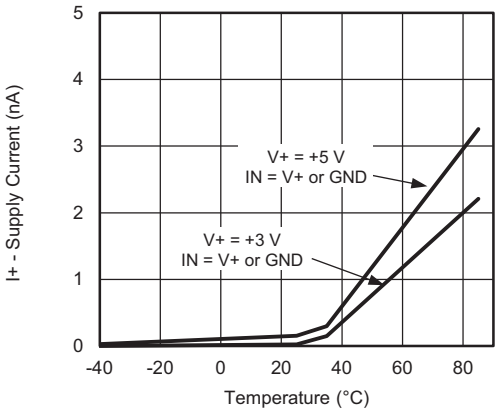
a. Typical values are for design aid only, not guaranteed nor subject to production testing.

b. Guarantee by design, not subjected to production test.

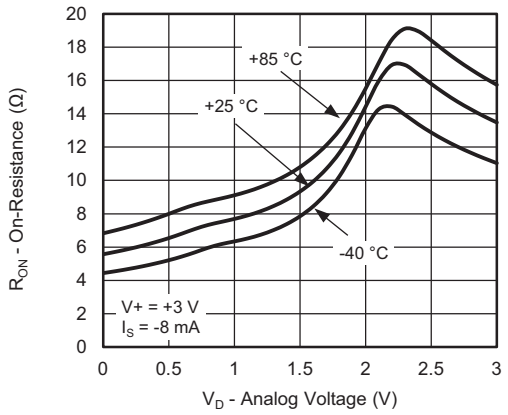
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



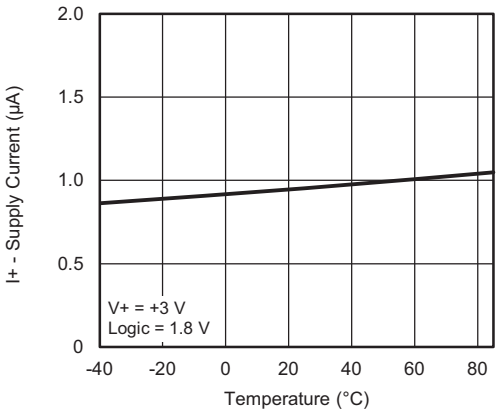
R_{ON} vs. V_D and Single Supply Voltage



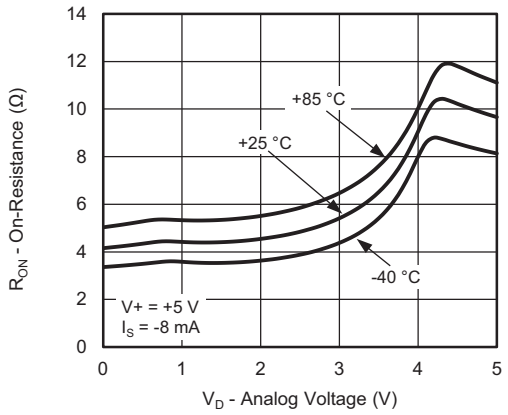
Supply Current vs. Temperature



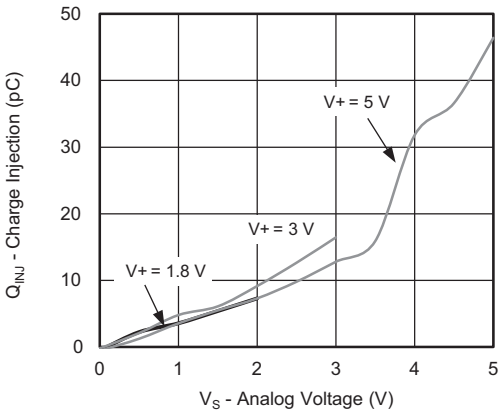
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

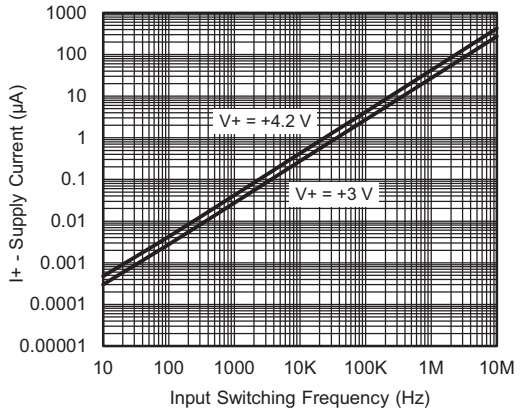


R_{ON} vs. Analog Voltage and Temperature

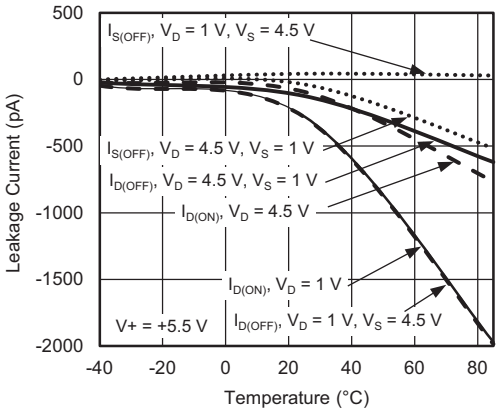


Charge Injection vs. Analog Voltage

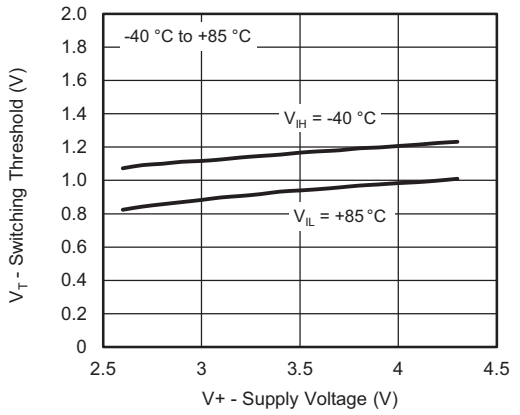
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



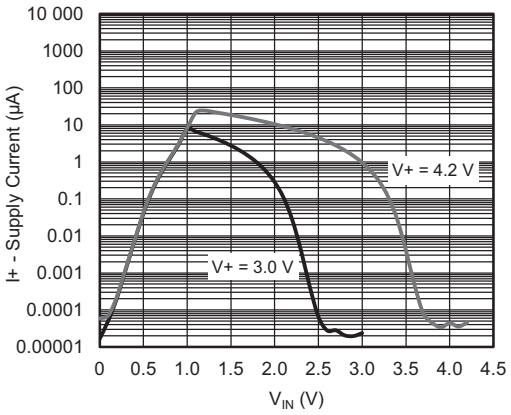
Supply Current vs. Input Switching Frequency



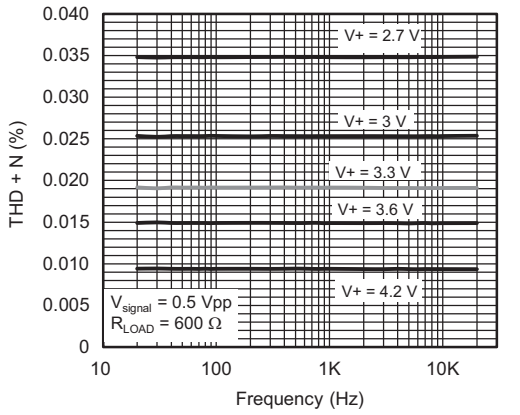
Leakage Current vs. Temperature



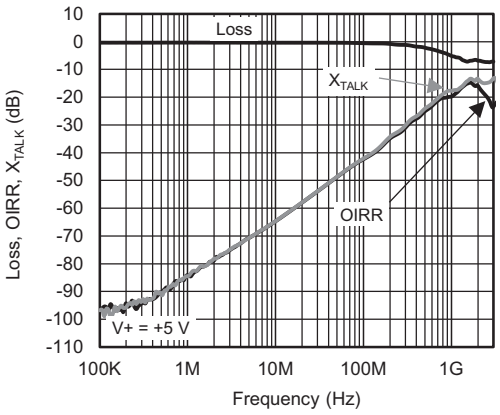
Switching Threshold vs. Supply Voltage



Supply Current vs. V_{IN}

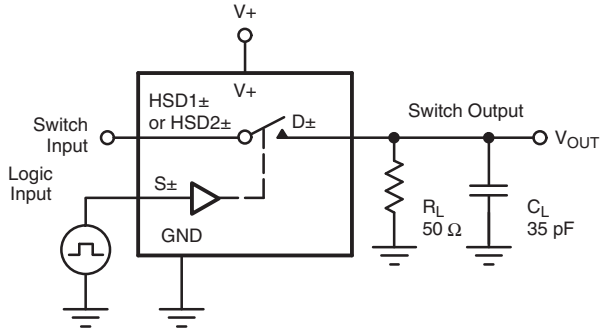


THD + N vs. Frequency



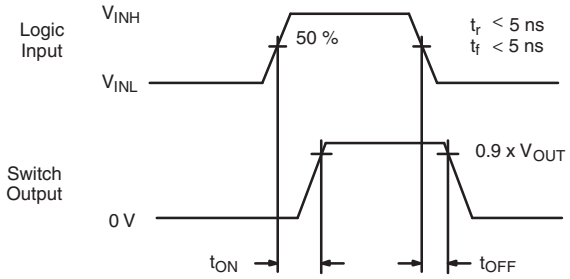
X_{TALK}, V+ = 5 V

TEST CIRCUITS



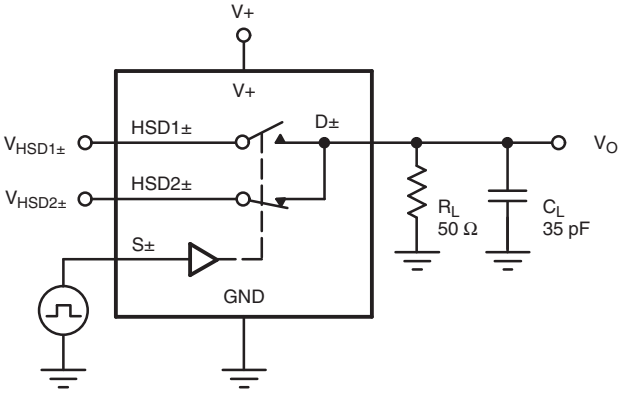
C_L (includes fixture and stray capacitance)

$$V_{OUT} = D\pm \left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

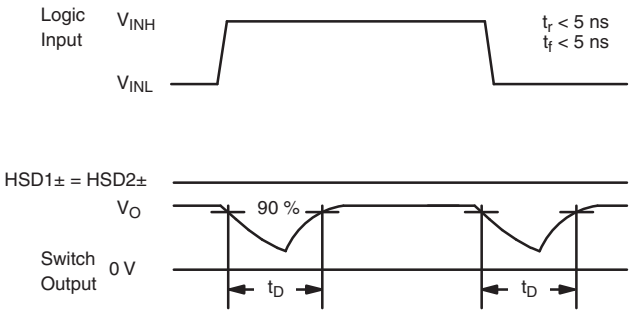
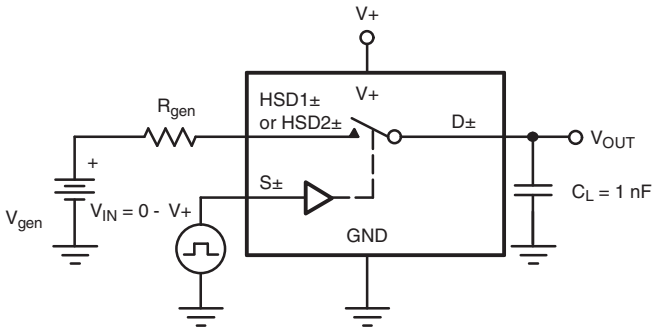
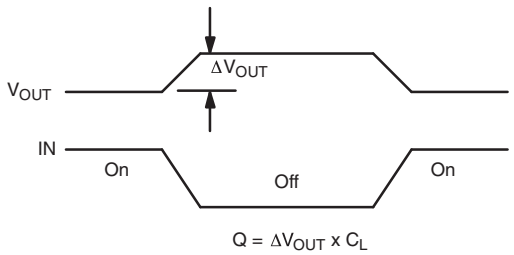


Fig. 2 - Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

TEST CIRCUITS

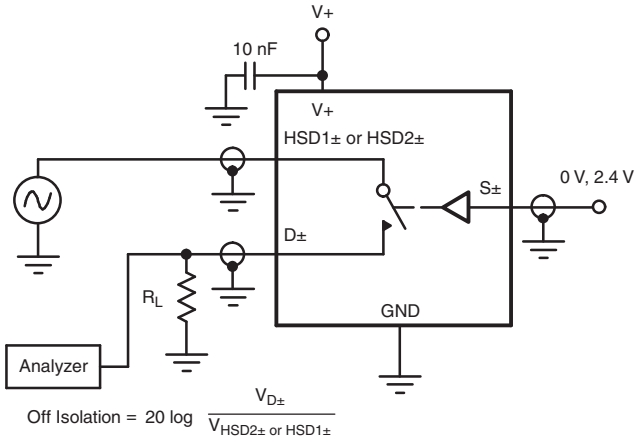


Fig. 4 - Off-Isolation

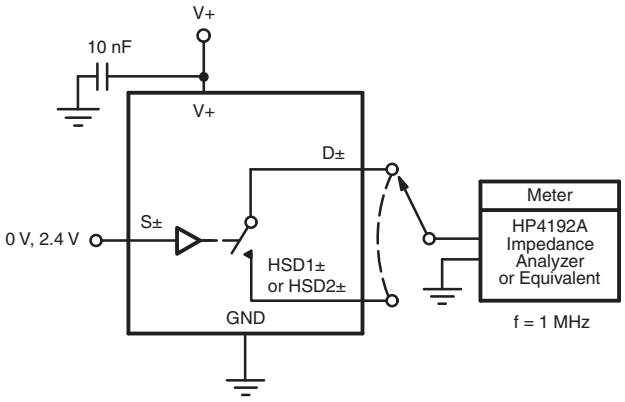
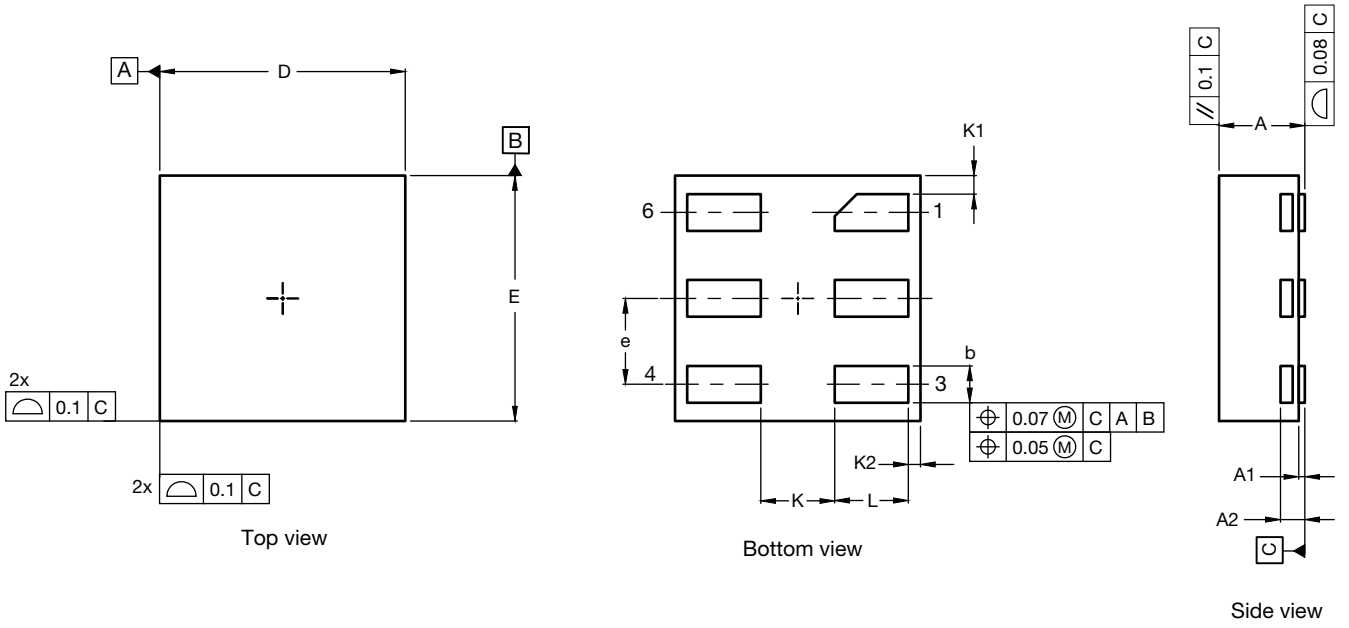


Fig. 5 - Channel Off / On Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75945.

µDFN-6L 1 mm x 1 mm Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.32	0.35	0.38	0.013	0.014	0.015
A1	0.00	-	0.05	0.000	-	0.002
A2	0.10 Ref.			0.004 Ref.		
b	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.35 BSC			0.014 BSC		
K	0.30 Ref.			0.012 Ref.		
K1	0.075 Ref.			0.003 Ref.		
K2	0.05 Ref.			0.002 Ref.		
L	0.27	0.30	0.33	0.011	0.012	0.013

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M-1994.
(3) N is the number of terminals.
Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

ECN: T16-0553-Rev. A, 26-Sep-16
DWG: 6053

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