

# BUK755R2-40B

## N-channel TrenchMOS standard level FET

Rev. 02 — 16 January 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

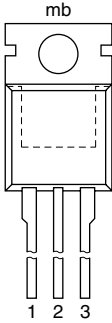
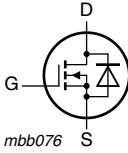
Table 1. Quick reference

| Symbol                         | Parameter                                    | Conditions  | Min | Typ | Max | Unit       |
|--------------------------------|--|---|-----|-----|-----|------------|
| $V_{DS}$                       | drain-source voltage                         | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$   | -   | -   | 40  | V          |
| $I_D$                          | drain current                                | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$<br>see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ;                           | [1] | -   | 75  | A          |
| $P_{tot}$                      | total power dissipation                      | $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>   | -   | -   | 203 | W          |
| <b>Avalanche ruggedness</b>    |  |   |     |     |     |            |
| $E_{DS(AL)S}$                  | non-repetitive drain-source avalanche energy | $I_D = 75\text{ A}; V_{sup} \leq 40\text{ V};$<br>$R_{GS} = 50\ \Omega; V_{GS} = 10\text{ V};$<br>$T_{j(init)} = 25\text{ °C};$ unclamped | -   | -   | 494 | mJ         |
| <b>Dynamic characteristics</b> |  |   |     |     |     |            |
| $Q_{GD}$                       | gate-drain charge                            | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$<br>$V_{DS} = 32\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 14</a>                   | -   | 16  | -   | nC         |
| <b>Static characteristics</b>  |  |   |     |     |     |            |
| $R_{DSon}$                     | drain-source on-state resistance             | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 11</a> ;<br>see <a href="#">Figure 12</a>      | -   | 4.4 | 5.2 | m $\Omega$ |

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description                       | Simplified outline   | Graphic symbol  |
|-----|--------|-----------------------------------|--|---|
| 1   | G      | gate                              |  |  |
| 2   | D      | drain                             |  |   |
| 3   | S      | source                            |  |   |
| mb  | D      | mounting base; connected to drain |  |   |

**SOT78A**  
(3-lead TO-220AB; SC-46)

## 3. Ordering information

**Table 3. Ordering information**

| Type number  | Package          |  | Description  | Version |
|--------------|------------------|--|--|---------|
|              | Name             |  |  |         |
| BUK755R2-40B | 3-lead TO-220AB; |  | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78A  |
|              | SC-46            |  |  |         |

## 4. Limiting values

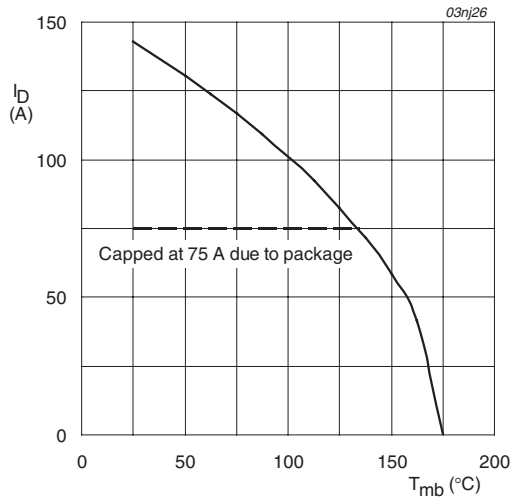
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions   | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|
| $V_{DS}$                    | drain-source voltage                         | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$  | -   | 40  | V    |
| $V_{DGR}$                   | drain-gate voltage                           | $R_{GS} = 20\text{ k}\Omega$   | -   | 40  | V    |
| $V_{GS}$                    | gate-source voltage                          |  | -20 | 20  | V    |
| $I_D$                       | drain current                                | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; [1]                           | -   | 143 | A    |
|                             |  | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; [2]                           | -   | 75  | A    |
|                             |  | $T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> ; [2]   | -   | 75  | A    |
| $I_{DM}$                    | peak drain current                           | $T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see <a href="#">Figure 3</a>  | -   | 573 | A    |
| $P_{tot}$                   | total power dissipation                      | $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>  | -   | 203 | W    |
| $T_{stg}$                   | storage temperature                          |  | -55 | 175 | °C   |
| $T_j$                       | junction temperature                         |  | -55 | 175 | °C   |
| <b>Source-drain diode</b>   |  |  |     |     |      |
| $I_S$                       | source current                               | $T_{mb} = 25\text{ °C};$ [1]   | -   | 143 | A    |
|                             |  | $T_{mb} = 25\text{ °C};$ [2]   | -   | 75  | A    |
| $I_{SM}$                    | peak source current                          | $t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$  | -   | 573 | A    |
| <b>Avalanche ruggedness</b> |  |  |     |     |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $I_D = 75\text{ A}; V_{sup} \leq 40\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V};$<br>$T_{j(init)} = 25\text{ °C};$ unclamped | -   | 494 | mJ   |

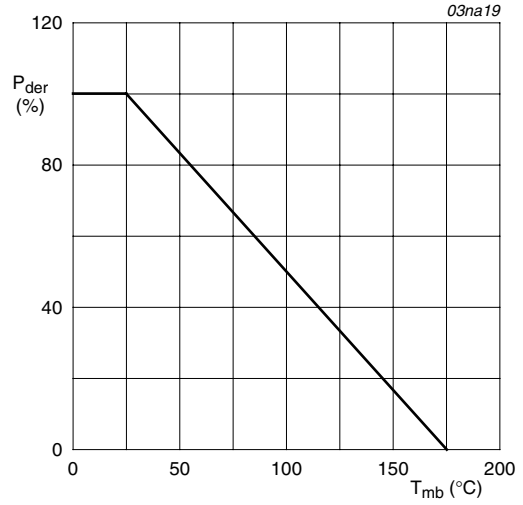
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



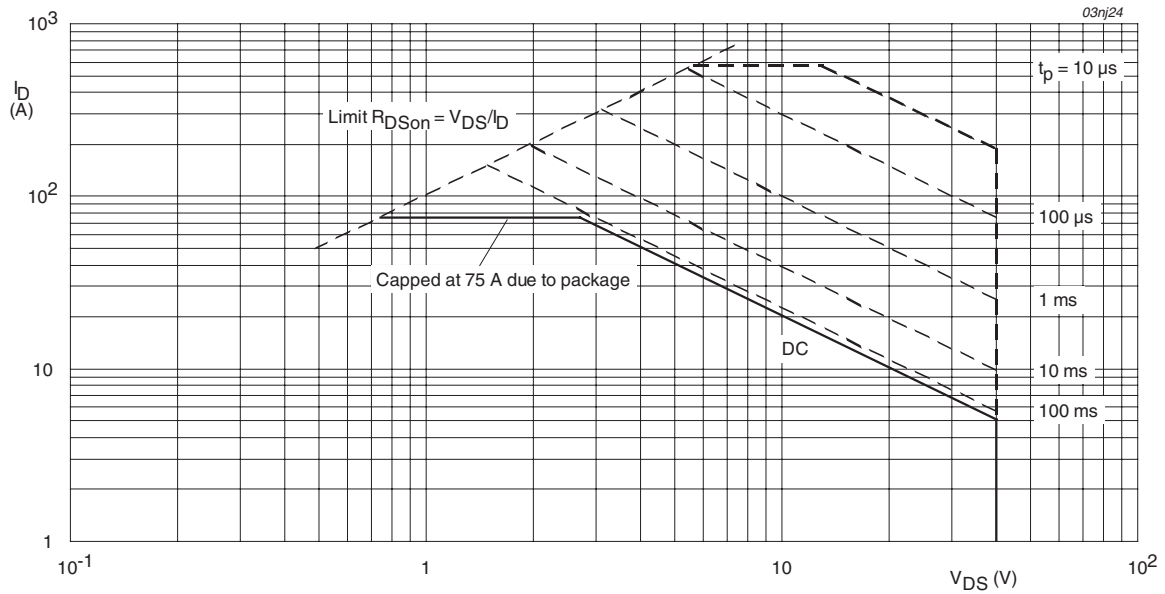
$$V_{GS} \geq 4.5V$$

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



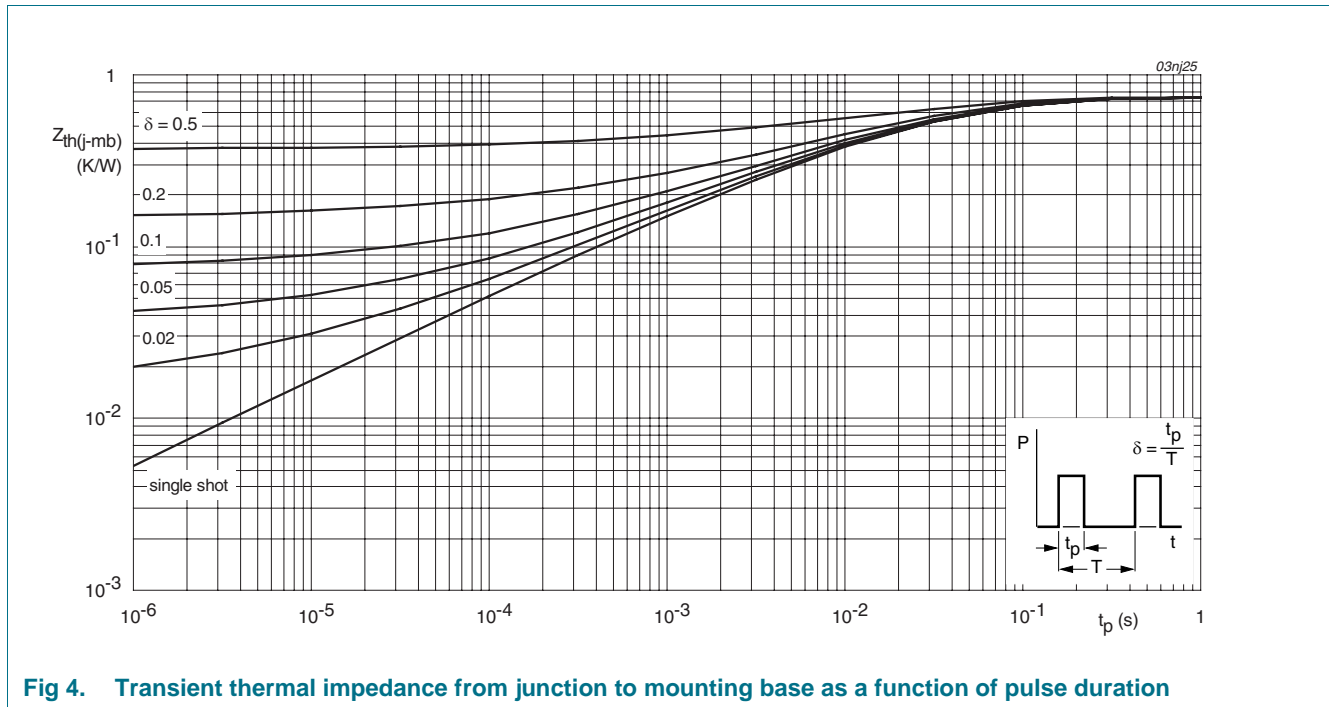
$$T_{mb} = 25^\circ C; I_{DM} \text{ is single pulse}$$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol         | Parameter   | Conditions                   | Min | Typ | Max  | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a> | -   | -   | 0.74 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | vertical in still air        | -   | 60  | -    | K/W  |

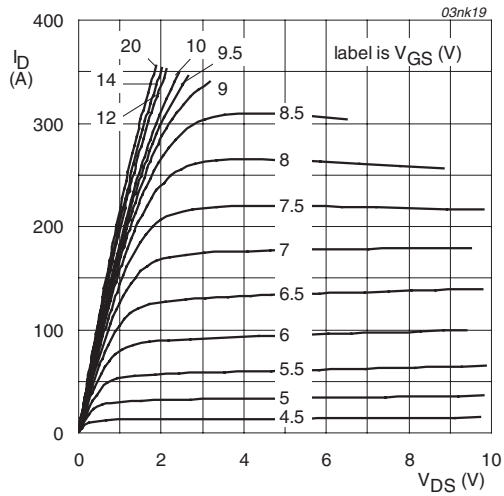


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

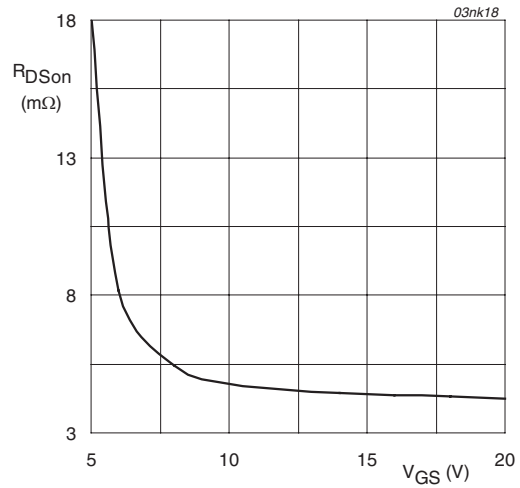
**Table 6. Characteristics**

| Symbol                         | Parameter                        | Conditions  | Min | Typ  | Max  | Unit          |
|--------------------------------|----------------------------------|---|-----|------|------|---------------|
| <b>Static characteristics</b>  |                                  |   |     |      |      |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage   | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | 40  | -    | -    | V             |
|                                |                                  | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$   | 36  | -    | -    | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>  | 2   | 3    | 4    | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>                                       | 1   | -    | -    | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 10</a>                                       | -   | -    | 4.4  | V             |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | 0.02 | 1    | $\mu\text{A}$ |
|                                |                                  | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$   | -   | -    | 500  | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current             | $V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | 2    | 100  | nA            |
|                                |                                  | $V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -   | 2    | 100  | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>  | -   | 4.4  | 5.2  | m $\Omega$    |
|                                |                                  | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a> | -   | -    | 9.9  | m $\Omega$    |
| <b>Dynamic characteristics</b> |                                  |   |     |      |      |               |
| $Q_{G(tot)}$                   | total gate charge                | $I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 14</a>           | -   | 52   | -    | nC            |
| $Q_{GS}$                       | gate-source charge               |   | -   | 12   | -    | nC            |
| $Q_{GD}$                       | gate-drain charge                |   | -   | 16   | -    | nC            |
| $C_{iss}$                      | input capacitance                | $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 15</a>             | -   | 2842 | 3789 | pF            |
| $C_{oss}$                      | output capacitance               |   | -   | 711  | 853  | pF            |
| $C_{rss}$                      | reverse transfer capacitance     |   | -   | 296  | 406  | pF            |
| $t_{d(on)}$                    | turn-on delay time               | $V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$   | -   | 15   | -    | ns            |
| $t_r$                          | rise time                        |   | -   | 51   | -    | ns            |
| $t_{d(off)}$                   | turn-off delay time              |   | -   | 81   | -    | ns            |
| $t_f$                          | fall time                        |   | -   | 56   | -    | ns            |
| $L_D$                          | internal drain inductance        | from drain lead 6 mm from package to centre of die; $T_j = 25 \text{ }^\circ\text{C}$   | -   | 4.5  | -    | nH            |
|                                |                                  | from contact screw on mounting base to centre of die; $T_j = 25 \text{ }^\circ\text{C}$   | -   | 3.5  | -    | nH            |
| $L_S$                          | internal source inductance       | from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$  | -   | 7.5  | -    | nH            |
| <b>Source-drain diode</b>      |                                  |   |     |      |      |               |
| $V_{SD}$                       | source-drain voltage             | $I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>                                   | -   | 0.85 | 1.2  | V             |
| $t_{rr}$                       | reverse recovery time            | $I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -10 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$    | -   | 54   | -    | ns            |
| $Q_r$                          | recovered charge                 |   | -   | 38   | -    | nC            |



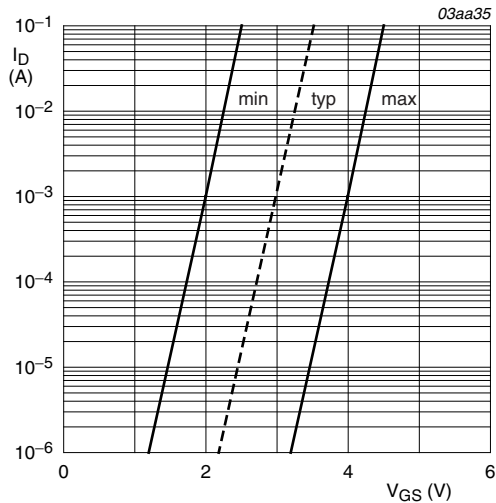
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



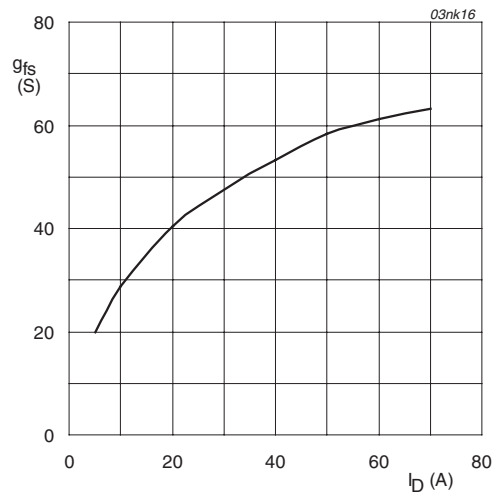
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



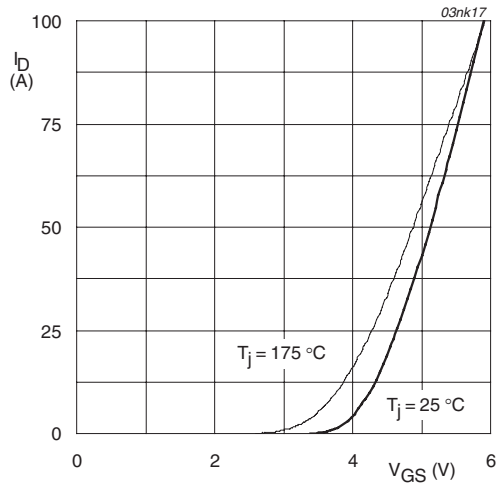
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



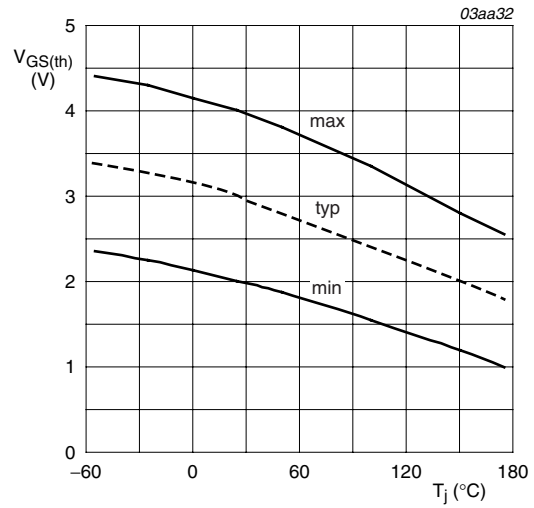
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

**Fig 8. Forward transconductance as a function of drain current; typical values**



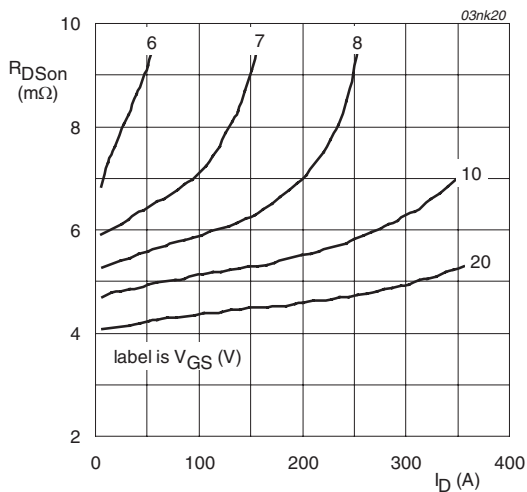
$$V_{DS} = 25V$$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



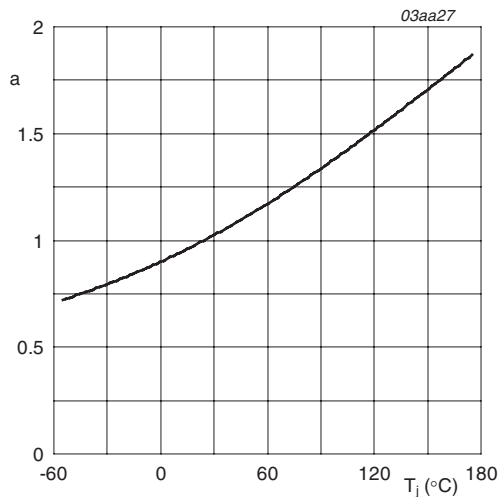
$$I_D = 1mA; V_{DS} = V_{GS}$$

**Fig 10. Gate-source threshold voltage as a function of junction temperature**



$$T_j = 25^{\circ}C$$

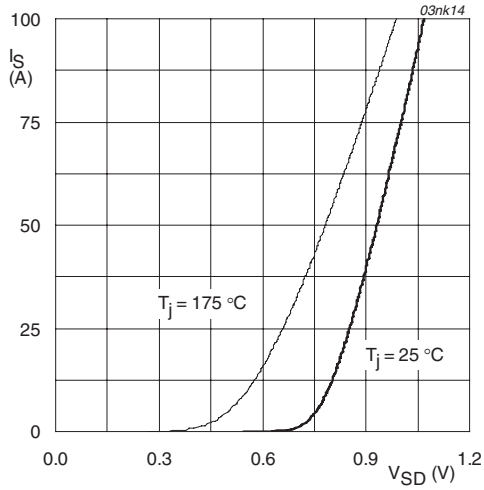
**Fig 11. Drain-source on-state resistance as a function of drain current; typical values**



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

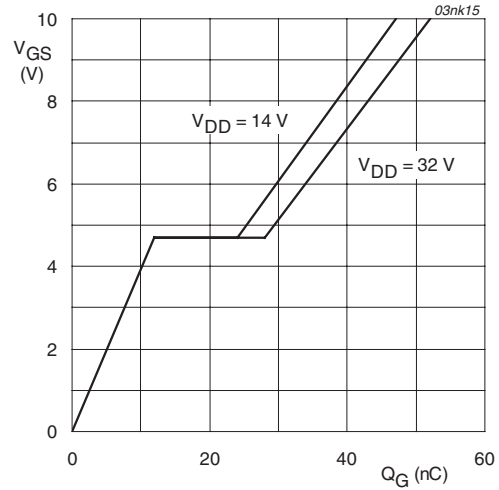
**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**





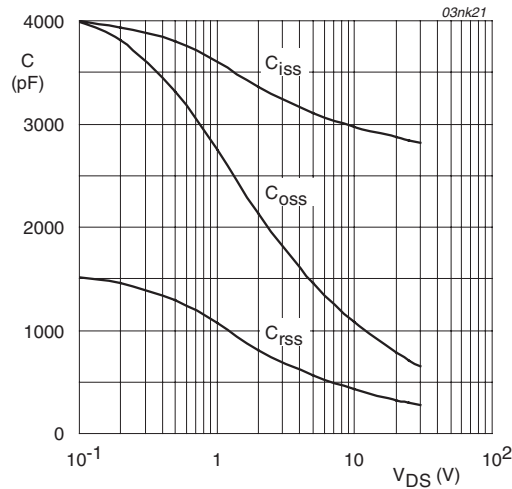
$V_{GS} = 0V$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$T_j = 25^\circ C; I_D = 25A$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



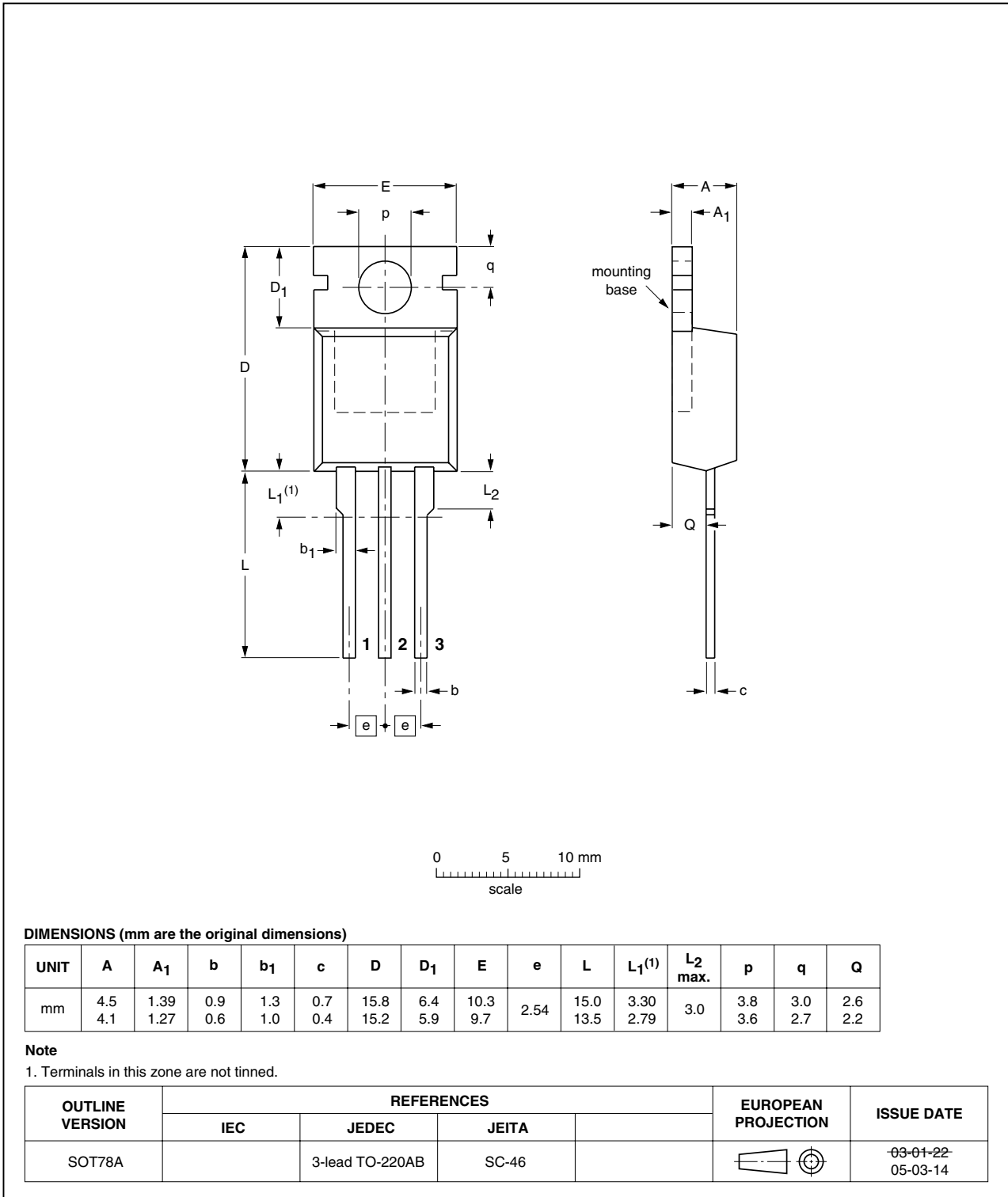
$V_{GS} = 0V; f = 1MHz$

**Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

**7. Package outline**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A



**Fig 16. Package outline SOT78A (3-lead TO-220AB; SC-46)**

## 8. Revision history

Table 7. Revision history

| Document ID        | Release date | Data sheet status  | Change notice | Supersedes         |
|--------------------|--------------|--|---------------|--------------------|
| BUK755R2-40B_2     | 20090116     | Product data sheet   | -             | BUK75_765R2_40B-01 |
| Modifications:     |              | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number BUK755R2-40B separated from data sheet BUK75_765R2_40B-01.</li><li>• Package outline updated.</li></ul> |               |                    |
| BUK75_765R2_40B-01 | 20030514     | Product data sheet   | -             | -                  |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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 Date of release: 16 January 2009  
 Document identifier: BUK755R2-40B\_2