VTR-S1000

Evaluation and Product Development Platform

User Guide

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Table of Contents

Preface

About This User Guide

This User Guide describes the features and operations of the SOC VTR-S1000 Evaluation and Product Development Platform. Details on the I/O interfaces and the corresponding components are provided.

Related Documents

Data Sheets of IP Cores

- Datasheet - H.265 Encoder IP Cores
- Datasheet - H.265 Decoder IP Cores
- Datasheet - H.264 Encoder IP Cores
- Datasheet - H.264 Decoder IP Cores
- Datasheet – MPEG-2 Encoder IP Cores
- Datasheet – MPEG-2 Decoder IP Cores
- Datasheet – H.264-to-H.265 Transcoder IP Cores
- Datasheet – H.265-to-H.264 Transcoder IP Cores
- Datasheet - MPEG2-to-H.264 Transcoder IP Cores
- Datasheet - H.264-to-MPEG2 Transcoder IP Cores

Integration Sheets of IP Cores

- Integration Sheet - H.265 Encoder IP Cores
- Integration Sheet - H.265 Decoder IP Cores
- Integration Sheet - H.264 Encoder IP Cores
- Integration Sheet - H.264 Decoder IP Cores
- Integration Sheet - H.265 4k Encoder IP Cores
- Integration Sheet - H.265 4k Decoder IP Cores
- Integration Sheet - H.264 4k Encoder IP Cores
- Integration Sheet - H.264 4k Decoder IP Cores
- Integration Sheet - MPEG-2 Encoder IP Cores
- Integration Sheet - MPEG-2 Decoder IP Cores
- Integration Sheet - H.264-to-MPEG2 Transcode IP Cores
- Integration Sheet - MPEG2-to-H264 Transcoder IP Cores

Data Sheets of Codec Modules

- Datasheet - H.264 Encoder Modules
- Datasheet - H.264 Decoder Modules

Data Sheets of Codec Chipsets

- Datasheet - H.264 Encoder Chipsets
- Datasheet - H.264 Decoder Chipsets

VTR-S1000 Evaluation and Product Development Platform

1. Overview

The SOC VTR-S1000 Evaluation and FPGA Development Platform is designed for four major functions:

1. As an evaluation board for the SOC MPEG codec modules and IP Cores (encoders, decoders, and transcoders).

2. As a product development platform for systems that use the SOC MPEG codec modules or IP cores.

3. As a development board for product development based on the SOC Generic System-on-Module (G-SoM) Modules.

4. As an OEM product of H.265/H.264/MPEG2 video/audio (HDMI) over IP transponder.

A unique feature of the VTR-S1000 is its small size, which allows for direct applications as a product. It can be used as an evaluation board for the SOC MPEG codec modules or IP cores, and then use the same board for product development. Users can also enclose the VTR-S1000 into a customer enclosure and market as a finished product (OEM product).

The VTR-S1000 has its own FPGA chip (the Xilinx Spartan-6 XC6SLX45T) which controls the I/Os and can be combined with the FPGA on the G-SoM module. This allows for the product development of multiple FPGA based systems.

The VTR-S1000 with an encoder or decoder module can be a fully functional H.265 (or H.264 or MPEG-2) video/audio over the Internet (IP) transmitter or receiver that can be packaged into an enclosure box for end-user uses. It provides HDMI input, HDMI output, 3G/HD SDI input or output, and an Ethernet port with the UDP/RTP/IP compatibilities. The VTR-S1000 also has extension headers for additional I/Os, such as a WiFi module for wireless video transmission or reception. Contact SOC sales@soctechnologies.com for details.

The VTR-S1000 Evaluation Board and FPGA Development Platform is shown in Figure 1 (top view) and Figure 2 (bottom view) with the SOC Codec module plugged on to the DDR3 connectors.

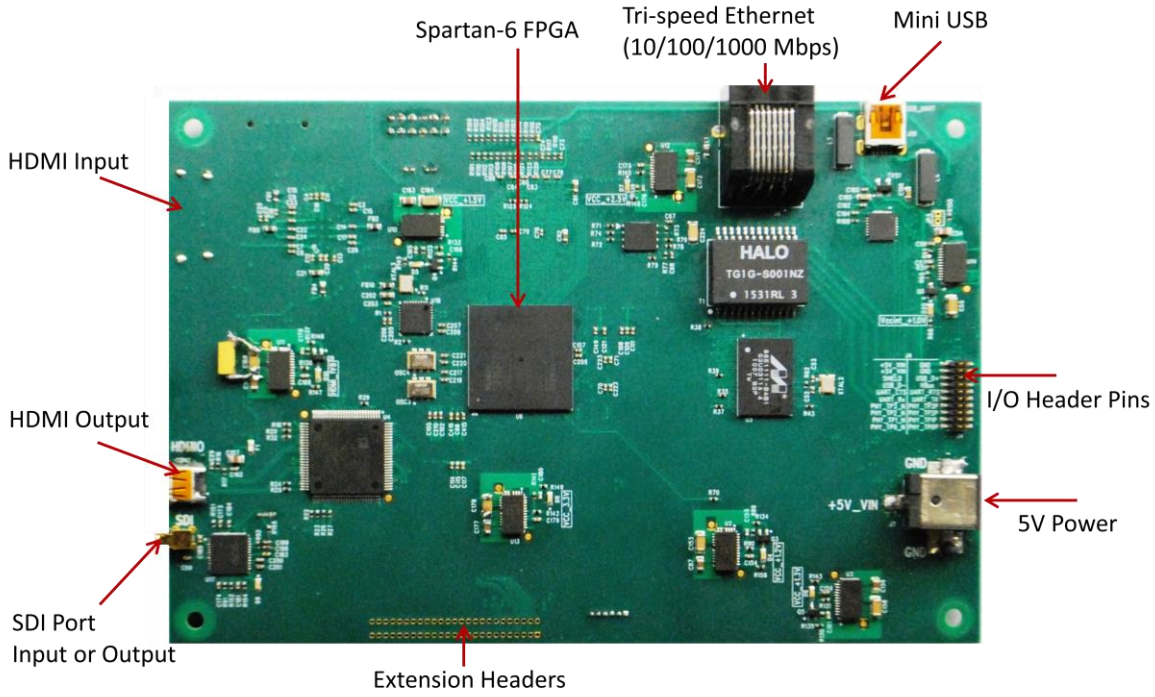

Fig.1 VTR-S1000 Top View

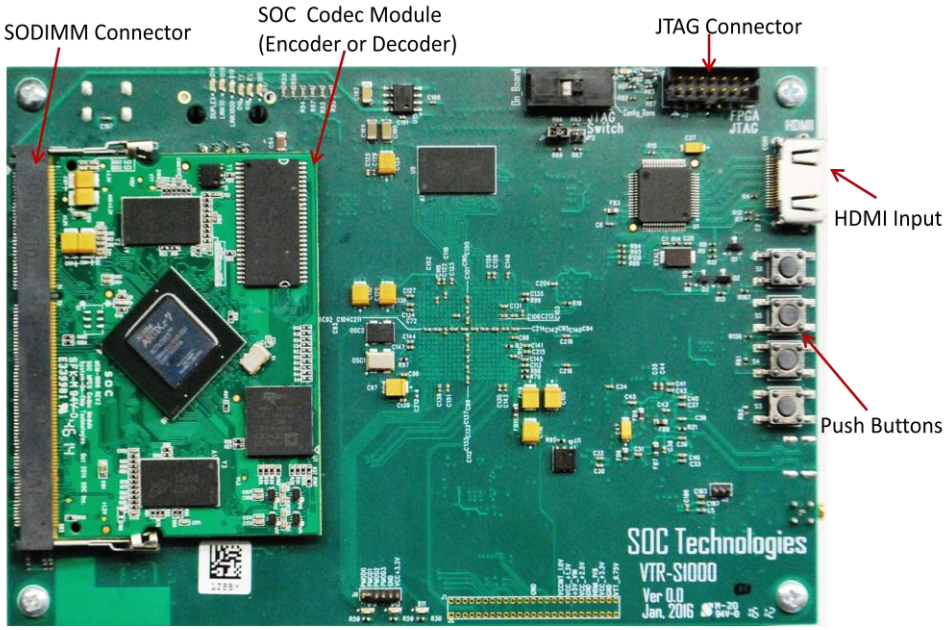

Fig. 2 VTR-S1000 bottom View

Key Features

- Xilinx XC6SLX45T FPGA
- 2 GB DDR3 RAM
- One DDR3 SODIMM connector for SOC MPEG Codec Module (encoder or decoder)
- HDMI input
- HDMI output
- 3G/HD-SDI input or output (configurable)
- Ethernet (Tri-speed of 10/100/1000 Mbps)
- Mini USB
- Extension Headers
- Push buttons
- LEDs
- Power rails for SOC MPEG Codec Module

VRT-1000 Dimension

- Length = 6”
- Width = 4”

2. Functions the VTR-S1000

2.1 For Evaluating the SOC MPEG Codec Modules

The VTR-S1000 is preloaded with firmware for evaluating the SOC MPEG codec modules. It is a plug-and-play system that allows the user to insert the desired module (encoder, decoder, or transcoder), and connect the I/O devices to start the evaluation.

For encoder evaluation, the input video source is sent to the VTR-S1000 via the HDMI or SDI input port; the encoded stream is sent to the computer through the Ethernet port. Users can decode the encoded streams by using standard software decoders, or a second VTR-S1000 as a decoder.

For decoder evaluation, the compressed streams are sent to the VTR-S1000 through the Ethernet. The software for sending the streams is provided as part of the VTR-S1000 package. The decoded video and audio streams are sent to the HDMI or SDI output port for display.

For simultaneous evaluation of the encoder and the decoder, the input video stream is sent to the VTR-S1000 via the HDMI or SDI input port. The input video stream is encoded by the encoder, and then sent to the decoder for decoding. The decoded video stream is sent to the HDMI or SDI output port for display. The end-to-end latency of encoding and decoding can be measured by observing the time difference of the input video stream versus the output video stream.

For transcoder evaluation, both the input stream and transcoded stream are sent through the Ethernet port.

Detailed instructions for evaluating the SOC encoders and decoders using the VTR-S1000 are provided in “Instruction Sheet of Using the VTR-S1000 to Evaluate SOC Codec Modules and IP cores”.

2.2 For Product Development

The VTR-S1000 is a versatile platform for product development, based on the SOC MPEG codec modules (or IP cores).

SOC provides (under licensing agreement) a “netlist” IP cores for all the I/O ports, including the network stack for the VTR-S1000, so that the users can drop them into their own designs without having to implement the I/O modules.

Design templates of the I/O drivers and the network stack IP cores are available for licensing. These can greatly speed up the development process.

The schematics design of the VTR-S1000 is available to the customers who have purchased the board, which provides the details information for using the board and a reference for user product design.

Users can also purchase the design files (e.g. Gerber file) from SOC, which can be used as a reference for the user PCB once the product is developed. Contact SOC sales (sales@soctechnologies.com) for details.

2.3 For Product Development based on the SOC G-SoM

The SOC SoM modules can also be used as generic System on Module (SoM) platform for user designs. The VTR-S1000 is equipped with one FPGA, one DSP, and with the required memory blocks. This allows users to download their own firmware/software to configure the module according to their specific design. Once configured, the module can be used as SoM module for user applications. This accelerates product development and saves costs. Refer to the datasheet of the G-SoM-1000 for further details.

2.4 As an H.264 (or MPEG-2) Video over Internet (IP) OEM Product

The VTR-S1000, with a H.264 (MPEG-2) encoder or a decoder module, is a ready to use H.264 (or MPEG-2) video/audio over IP transmitter or receiver which is offered as an OEM product by SOC. Contact SCO sales@soctechnologies.com for information.

2.5 The SOC Product Code System

The products described in the previous sub-sections, from 2.1 to 2.4, are the combinations of the VTR-S1000 (as the carrier board), the modules, and the MPEG codec IP cores. These products are standard offerings of SOC Technologies. Furthermore, SOC also has a series of carrier boards, in parallel with the VTR-S1000, which includes VoIP-I-4K, VoIP-X-4K, VTR-4000C, and PCIe-I-8K etc. These carrier boards in combination with the SOC modules and codec IP cores form the SOC MPEG codec related product families. Figure 3 shows the Product Code system for these products.

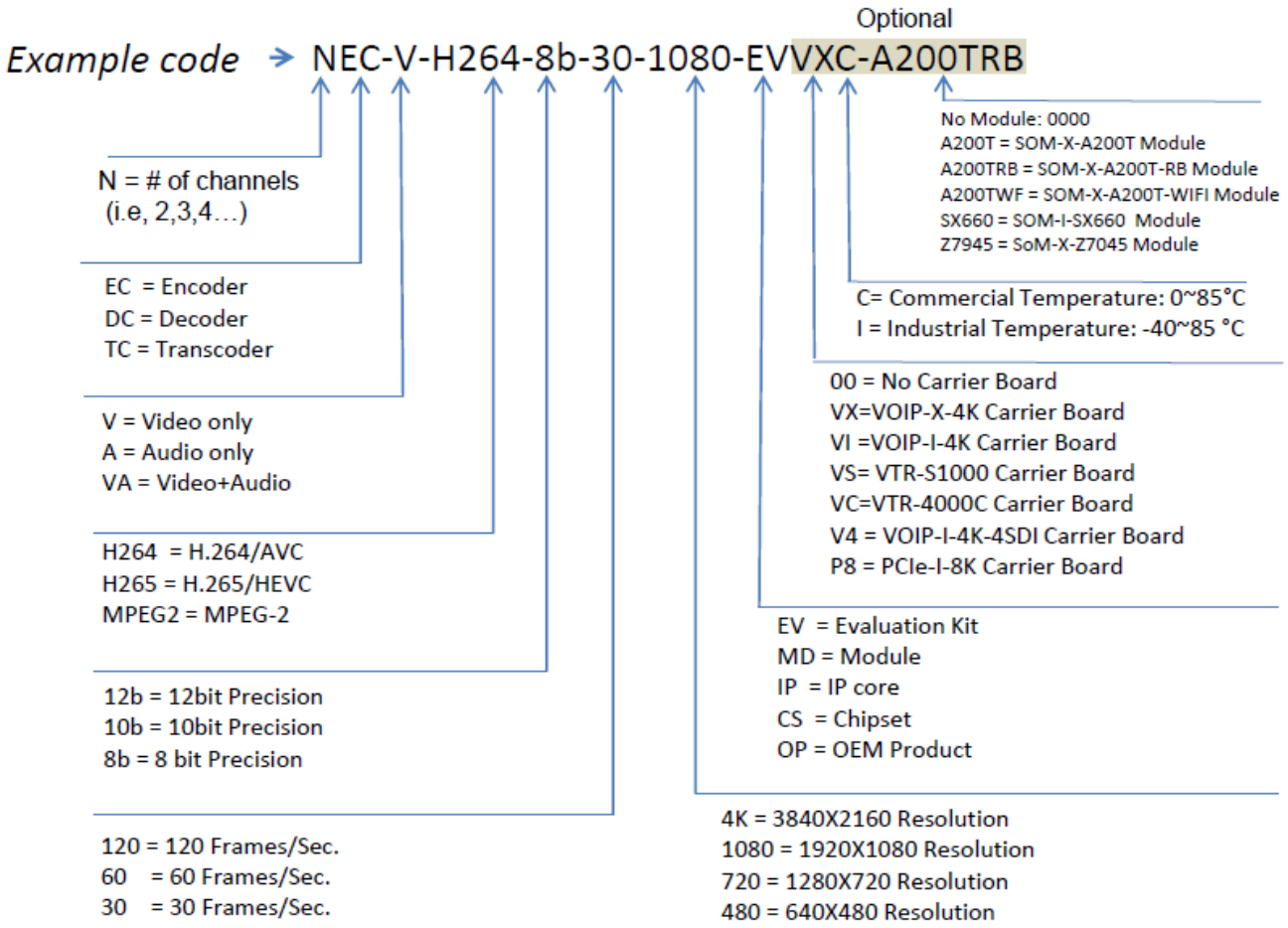

Fig. 3 The SOC product code format for the MPEG codec related products

3. Detailed Descriptions

Table-1 lists the components on the VT-S1000 that are important to the users. Refer to the schematics of the VTR-S1000 for the circuit design and the auxiliary components. The Schematics can be licensed for design references.

The following Sections describe the components listed in Table-1. Refer to the datasheets of the components for further details.

Table-1 Major components on the VTR-S1000

Item	Reference in Schematics	Part Name	Description	Manufacturer
1	U6	XC6SLX45T-2FGG484C	FPGA, Spartan-6, LX150/LX100/LX75/LX45	Xilinx
2	U9	MT41J128M16JT-125:K	DDR3 SDRAM 2GBit	Micron Technology Inc
3	U4	ADV7511KSTZ-P	HDMI Transmitter	Analog Devices Inc
4	U1	ADV7611BSWZ-P	HDMI receiver	Analog Devices Inc
5	U19	LMH0387	3 Gbps HD/SD SDI Interface (input or output)	TI
6	U5	88E1111_BAB1C000	Gigabit Ethernet Transceiver, 10/100/1000	Marvell
7	U8	N25Q128A13EF740F	128Mb, Serial Flash Memory	MICRON
8	Y3	ASFL1-27.000MHZ-L-T	OSCILLATOR 27.000 MHZ 3.3V	ABRACON
9	Y4	ASFLMB-100.000MHZ-XY-T	OSCILLATOR MEMS 100.000 MHZ	ABRACON
10	Y1	ABM3-28.6363MHZ-B2-T	CRYSTAL 28.6363MHZ 18PF	Abracon Corporation
11	Y2	ABM8-25.000MHZ-B2-T	CRYSTAL 25.000MHZ 18PF	Abracon Corporation
12	J2	MM80-204B1	CONN 204POS DDR3 SDRAM SODIMM	JAE Electronics
13	U7	DS28E01P-100+	1Kb PROTECTED 1-WIRE EEPROM	MAXIM

3.1 FPGA On the VTR-S1000

The FPGA on the VTR-S1000 is Xilinx XC6SLX45T. Refer to the schematics of the VRT-S1000 and Data Sheet of the FPGAs for further details.

3.2 DDR3 RAM

The VTR-S1000 is equipped with an off-chip DDR3 RAM of 2Gbit, which can be used for systems that require off-the-chip memory blocks. Refer to the datasheet of MT41J128M16JT-125 for the specifications and the allocations of this memory block.

The SOC VTR-S1000 Reference Design provides an example of using this DDR3 RAM.

3.3 HDMI Transmitter

The HDMI Transmitter is the ADV7511KSTZ-P by Analog Devices. Refer to the Datasheet of ADV7511KSTZ-P for details.

SOC provides the configuration file for ADV7511KSTZ-P which is a part of the I/O driver package. For evaluations, the ADV7511KSTZ-P is preconfigured for plug-and-play.

The SOC VTR-S1000 Reference Design provides an example of using ADV7511KSTZ-P.

3.4 HDMI Receiver

The HDMI Receiver is the ADV7611BSWZ-P by Analog Devices. Refer to the Datasheet of ADV7611BSWZ-P for details.

SOC provides the configuration file for ADV7611BSWZ-P which is a part of the I/O driver package. For evaluations, the ADV7611BSWZ-P is preconfigured for plug-and-play.

The SOC VTR-S1000 Reference Design provides an example of using ADV7611BSWZ-P.

3.5 3Gbps HD/SD SID Port

The VTR-S1000 provides a 3 Gbps HD/SD SDI port driven by the TI LMH0387 interface chip, which can be configured into either input (receiver) or output (transmitter). An SDI IP core inside the FPGA, Xilinx Spartan-6 XC6SLX45T can function as a transmitter or receiver. The SDI IP core is pre-loaded onto the VRT-S1000, when the VTR-S1000 is used for evaluating the SOC codec modules or IP cores. For product development purposes, the SDI IP core is available for licensing.

3.6 Gigabit Ethernet

The Ethernet PHY is the 88E1111_BAB1C000 by Marvel. It can be used for 10Mbps/100Mbps/1000Mbps. The configuration file is included in the I/O package. An Ethernet MAC core is a part of the Ethernet/UDP/IP network stack which can be licensed. For evaluations, the networks stack is preloaded to allow a plug-and-play system.

The SOC VTR-S1000 Reference Design provides an example of using M88E1111_BAB1C000.

3.7 Serial Flash Memory

The serial flash memory, N25Q128A13EF740F, is used to store the firmware of the FPGA. For evaluation, the I/O drivers and the Ethernet/UDP/IP network stack are pre-stored in the N25Q128A13EF740F. When the FMC-MCM-1000 is booted, the firmware stored in the

N25Q128A13EF740F will configure the FPGA and make the board a plug-and-play device to facilitate the evaluations of the SOC MPEG codec modules.

After the evaluation, users can store their own firmware into the N25Q128A13EF740F for product development. For product development purposes, the I/O driver and the Ethernet/UDP/IP network stack IP core in “netlist” format are available for licensing. The method of downloading the firmware into the N25Q128A13EF740F is detailed in Appendix-C.

4. Ordering Information

The VTR-S1000 can be ordered from SOC directly or through the distributors of SOC. Refer to the SOC web site, www.soctechnologies.com , for distributor locations and contact information.

SOC contacts:

E-mail: sale@soctechnologies.com

Telephone: 1-519-880-8609

5. Revision History

The following table shows the revision history for this document.

Date	Version	Revision
1/10/2013	SOC initial Release	
20/11/2014	Version 1.00	Rev. 1
02/12/2014	Version 1.10	Rev. 2
09/07/2015	Version 1.20	Rev. 3
20/12/2016	Version 2.00	Rev. 4
01/03/2020	Version 3.00	Rev. 5