STK672-630C-E

Thick-Film Hybrid IC

2-phase Stepping Motor Driver

ON Semiconductor®

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Overview

The STK672-630C-E is a hybrid IC for use as a unipolar, 2-phase stepping motor driver with PWM current control.

Applications

- Office photocopiers, printers, etc.

Features

- Built-in opened motor pin detection function (output current OFF).
- Built-in overcurrent detection function (output current OFF).
- Built-in overheat detection function (output current OFF).
- If opened motor pin, over-current, or overheat detection function is activated, the FAULT1 signal (active low) is output. The FAULT2 signal is used to output the result of activation of protection circuit detection at 3 levels.
- Built-in power on reset function.
- The motor speed is controlled by the frequency of an external clock signal.
- 2 phase or 1-2 phase excitation switching function.
- Using either or both edges of the clock signal switching function.
- Phase is maintained even when the excitation mode is switched.
- Rotational direction switching function.
- Supports schmitt input for 2.5V high level input.
- Incorporating a current detection resistor (0.141Ω: resistor tolerance $\pm2\%$), motor current can be set using two external resistors.
- The ENABLE pin can be used to cut output current while maintaining the excitation mode.
- With a wide current setting range, power consumption can be reduced during standby.
- No motor sound is generated during hold mode due to external excitation current control.

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage 1	V_{CC} max	No signal	50	V
Maximum supply voltage 2	V_{DD} max	No signal	-0.3 to +6.0	V
Input voltage	V_{IN} max	Logic input pins	-0.3 to +6.0	V
Output current 1	I_{OP} max	10μA, 1 pulse (resistance load)	10	A
Output current 2	I_{OH} max	V_{DD}=5V, CLOCK≥200Hz	2.65	A
Output current 3	I_{OF} max	Pin16 output current	10	mA
Allowable power dissipation 1	PdMF max	With an arbitrarily large heat sink. Per MOSFET	7.3	W
Allowable power dissipation 2	PdPK max	No heat sink	3.1	W
Operating substrate temperature	Tc		-20 to +105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta=25°C

Parameter	Symbol	Conditions	Ratings	unit
Operating supply voltage 1	V_{CC}	With signals applied	0 to 46	V
Operating supply voltage 2	V_{DD}	With signals applied	5±5%	V
Input high voltage	V_{IH}	Pins 10, 12, 13, 14, 15, 17 V_{DD}=5±5%	2.5 to V_{DD}	V
Input low voltage	V_{IL}	Pins 10, 12, 13, 14, 15, 17 V_{DD}=5±5%	0 to 0.8	V
Output current 1	$I_{OH}1$	Tc=105°C, CLOCK≥200Hz, Continuous operation, duty=100%	2.0	A
Output current 2	$I_{OH}2$	Tc=80°C, CLOCK≥200Hz, Continuous operation, duty=100%, See the motor current (I_{OH}) derating curve	2.2	A
CLOCK frequency	f_{CL}	Minimum pulse width: at least 10μs	0 to 50	kHz
Recommended Vref range	Vref	Tc=105°C	0.14 to 1.38	V

Electrical Characteristics at Tc=25°C, V_{CC}=24V, V_{DD}=5.0V

Parameter	Symbol	Conditions	min	typ	max	unit
V_{DD} supply current	I_{CCO}	Pin 9 current CLOCK=GND		5	8	mA
Output average current*	Ioave	R/L=1Ω/0.62mH in each phase	0.32	0.38	0.45	A
FET diode forward voltage	Vdf	If=1A (R_L=23Ω)		0.92	1.6	V
Output saturation voltage	Vsat	R_L=23Ω		0.33	0.48	V
Input high voltage	V_{IH}	Pins 10, 12, 13, 14, 15, 17	2.5			V
Input low voltage	V_{IL}	Pins 10, 12, 13, 14, 15, 17			0.8	V
FAULT1 low output voltage	V_{OLF}	Pin 16 (I_O=5mA)		0.25	0.5	V
5V level FAULT leakage current	I_{ILF}	Pin 16=5V			10	μA
FAULT2 opened motor pin detection output voltage	$V_{OF}1$		0.00	0.01	0.20	
FAULT2 Overcurrent detection output voltage	$V_{OF}2$	Pin 8 (when all protection functions have been activated)	2.4	2.5	2.6	V
FAULT2 Overheat detection output voltage	$V_{OF}3$		3.1	3.3	3.5	
5V level input current	I_{ILH}	Pins 10, 12, 13, 14, 15, 17=5V		50	75	μA
GND level input current	I_{ILL}	Pins 10, 12, 13, 14, 15, 17=GND			10	μA
Vref input bias current	I_{IB}	Pin 19=1.0V			1	μA
PWM frequency	fc		29	45	61	kHz
Overheat detection temperature	TSD	Design guarantee		144		°C
Drain-to-Source leakage current	I_{DSS}	V_{DS}=100V, Pins 2, 6, 9, and 18=GND			1	μA

* Maximum value of operating supply voltage 1 (V_{CC}) can not supply to STK672-630C-E, depending on motor current value. Refer to "8. Precautions, etc" of Usage Notes.
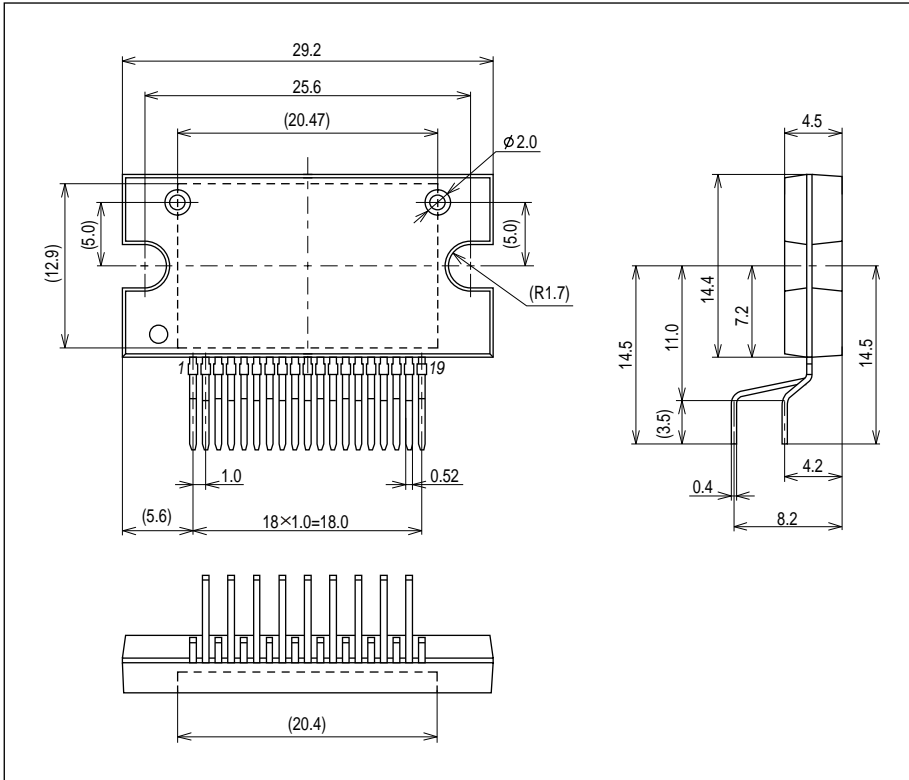
*Ioave values are for when the lead frame of the product is soldered to the mounting substrate.
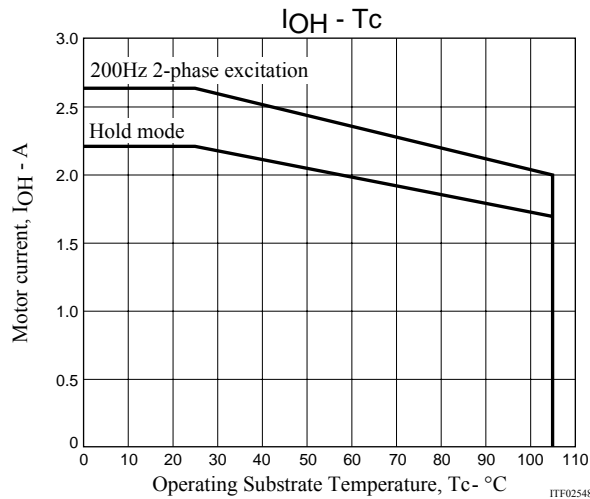
Notes: A fixed-voltage power supply must be used.

Package Dimensions

unit:mm (typ)

Derating curve of motor current, I_{OH}, vs. STK672-630C-E Operating substrate temperature, Tc

I_{OH} - Tc

200Hz 2-phase excitation

Hold mode

Motor current, I_{OH} - A

Operating Substrate Temperature, Tc - °C

ITF02548

Notes

• The current range given above represents conditions when output voltage is not in the avalanche state.

• If the output voltage is in the avalanche state, see the allowable avalanche energy for STK672-6** series hybrid ICs given in a separate document.

• The operating substrate temperature, Tc, given above is measured while the motor is operating.

• Because Tc varies depending on the ambient temperature, Ta, the value of I_{OH}, and the continuous or intermittent operation of I_{OH}, always verify this value using an actual set.

• The Tc temperature should be checked in the center of the metal surface of the product package.

Block Diagram
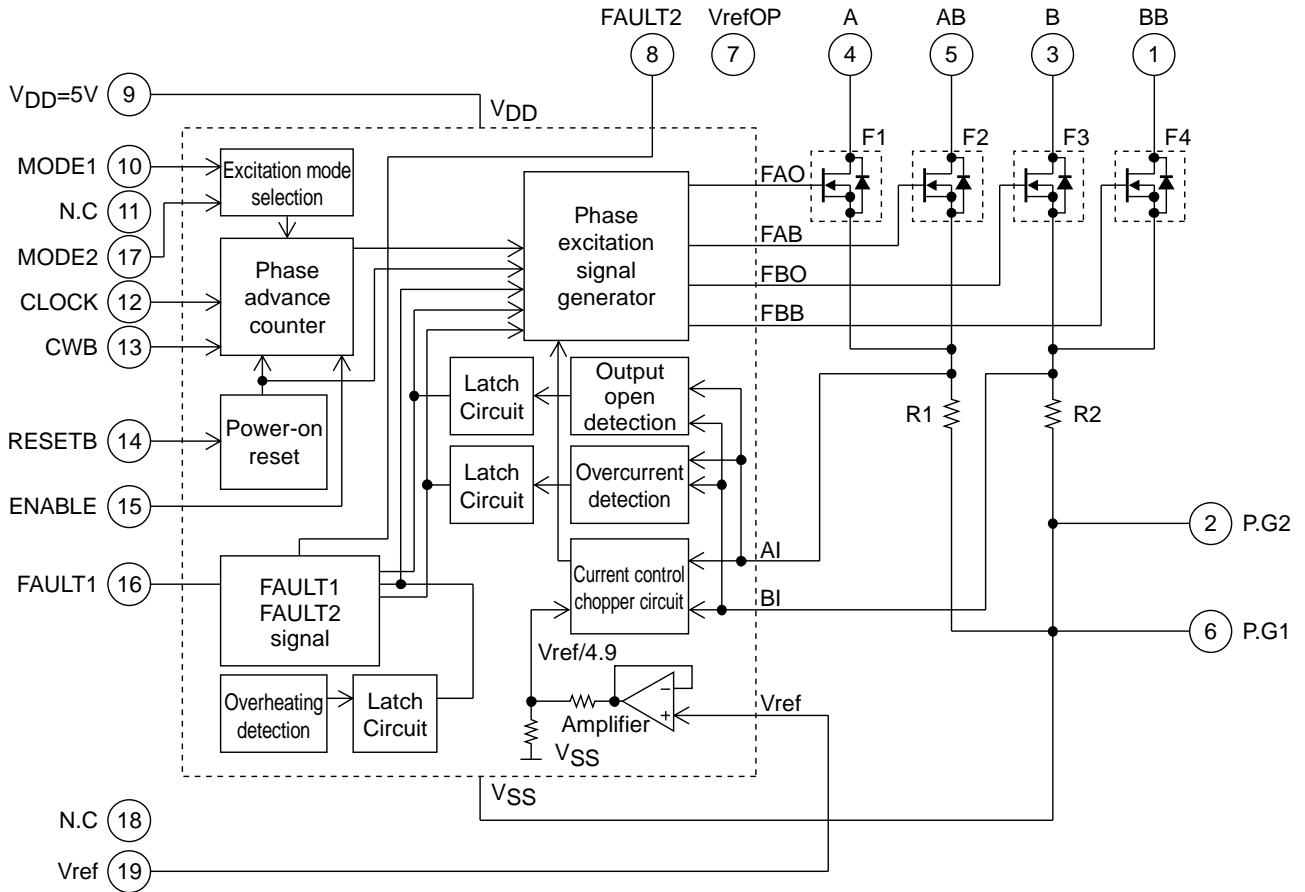
## Sample Application Circuit
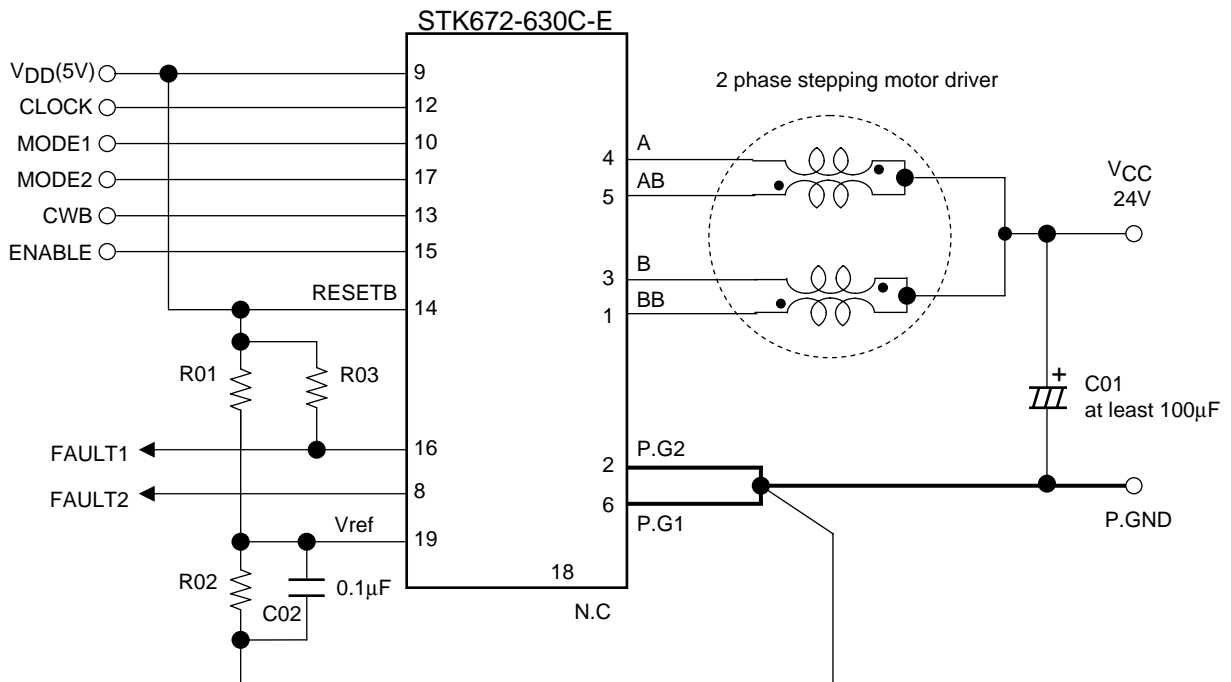
Precautions

[GND wiring]
- To reduce noise on the 5V system, be sure to place the GND of C01 in the circuit given above as close as possible to Pin 2 and Pin 6 of the hybrid IC. Also, to achieve accurate current settings, be sure to connect Vref GND to the point where P.G1 and P.G2 share a connection.

[Input pins]
- If V_{DD} is being applied, use care that each input pin does not apply a negative voltage less than -0.3V to PG and DO not apply a voltage greater than or equal to V_{DD} voltage.
- Do not wire by connecting the circuit pattern on the P.C.B side to N.C Pins. shown in the internal block diagram.
- Apply 2.5V high level input to pins 10, 12, 13, 14, 15, and 17.
- Since the input pins do not have built-in pull-up resistors, when the open-collector type pins 10, 12, 13, 14, 15, and 17 are used as inputs, a 1 to 20kΩ pull-up resistor (to V_{DD}) must be used.
  At this time, use a device for the open collector driver that has output current specifications that pull the voltage down to less than 0.8V at Low level (less than 0.8V at Low level when I_{OL}=5mA).

[Current setting Vref]
  If the motor current is temporarily reduced, the circuit given below (STK672-632C-E, 630C-E : I_{OH}>0.2A STK672-642C-E, 640C-E : I_{OH}>0.3A) is recommended.
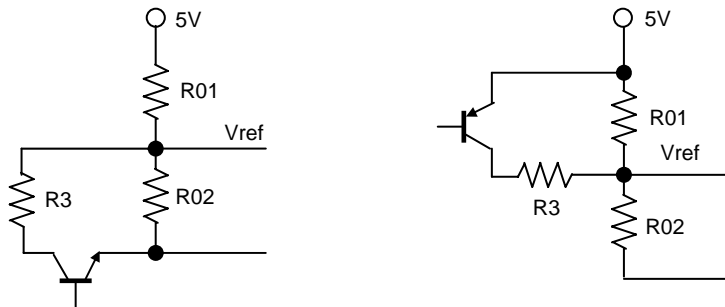
- Motor current peak value I_{OH} setting
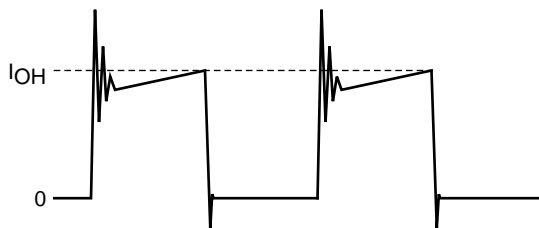
  I_{OH}=(Vref÷4.9) ÷Rs
  The value of 4.9 in Equation above represents the Vref voltage as divided by a circuit inside the control IC.
  Vref=(R02÷ (R01+R02)) ×5V(or 3.3V)
  Rs is an internal current detection resistor value of the hybrid IC.
  Rs=0.141Ω when using the STK672-630C-E
  Rs=0.089Ω when using the STK672-642C-E, -640C-E

Input Pin Functions

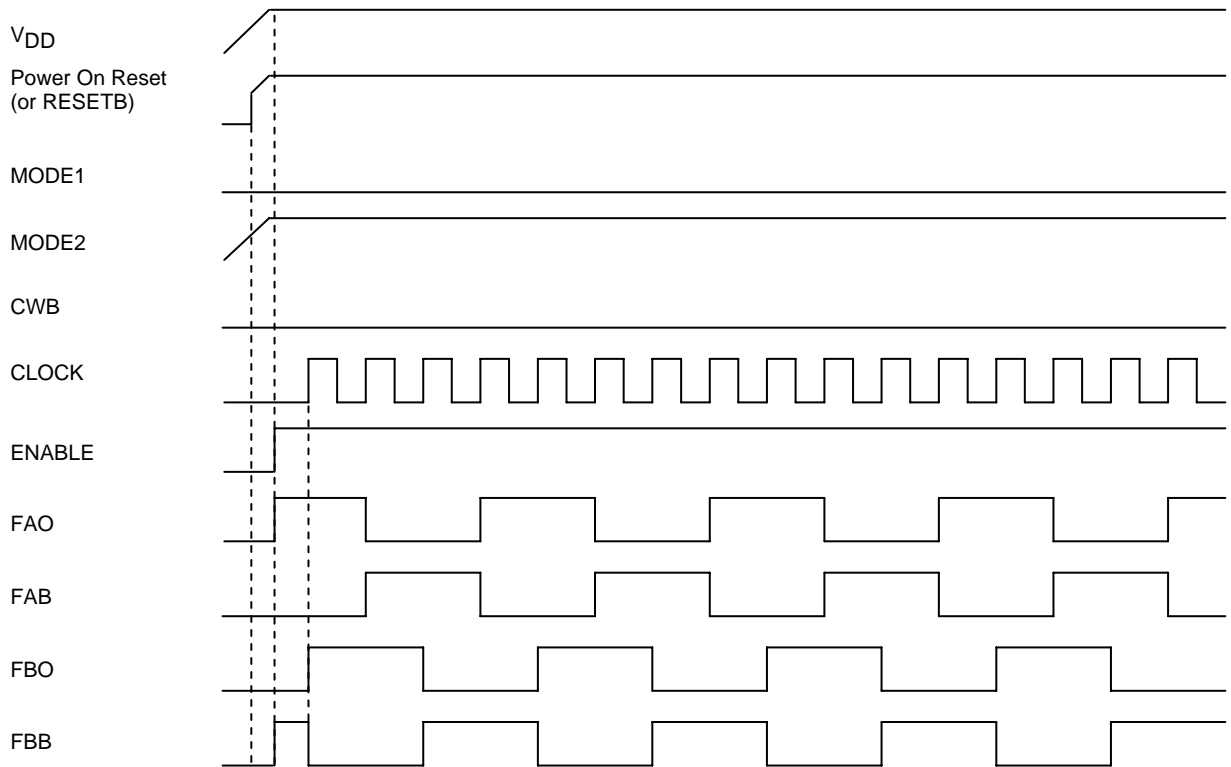| Pin Name	Pin No.	Function	Input Conditions When Operating
CLOCK	12	Reference clock for motor phase current switching	Operates on the rising edge of the signal (MODE2=H)
MODE1	10	Excitation mode selection	Low: 2-phase excitation
			High: 1-2 phase excitation
MODE2	17		High: Rising edge
			Low: Rising and falling edge
CWB	13	Motor direction switching	Low: CW (forward)
			High: CCW (reverse)
RESETB	14	System reset Initial state of A and BB phase excitation in the timing charts is set by switching from low to high.	A reset is applied by a low level
ENABLE	15	The A, AB, B, and BB outputs are turned off, and after operation is restored by returning the ENABLE pin to the high level, operation continues with the same excitation timing as before the low-level input.	The A, AB, B, and BB outputs are turned off by a low-level input.

Output Pin Functions

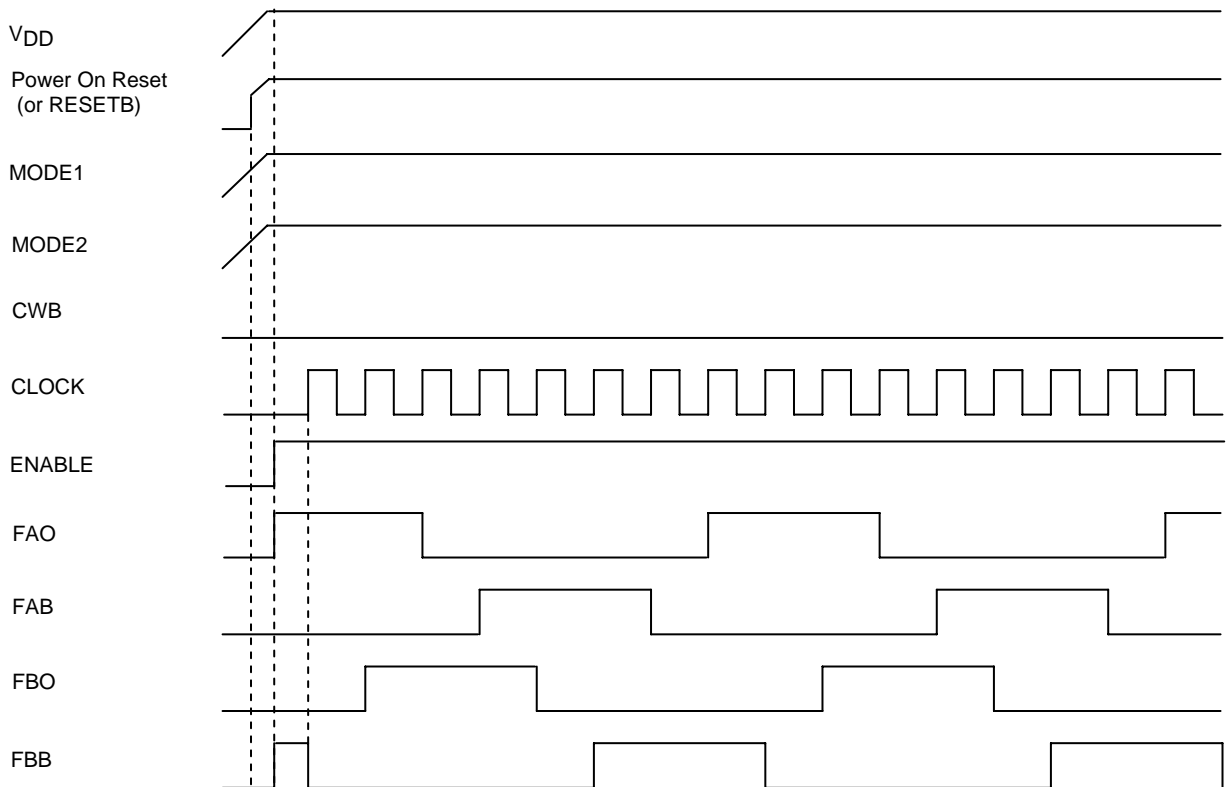| Pin Name	Pin No.	Function	Input Conditions When Operating
FAULT1	16	Monitor pin used when opened motor pin, over-current detection, or overheat detection function is activated.	Low level is output when detected.
FAULT2	8	The result of activation of protection circuit detection is output.	3 levels output voltage
VrefOP	7	Monitor pin of reference voltage used when opened motor pin detection.	Normal DC voltage output (typ98mV)

Note: See the timing chart for the concrete details on circuit operation.
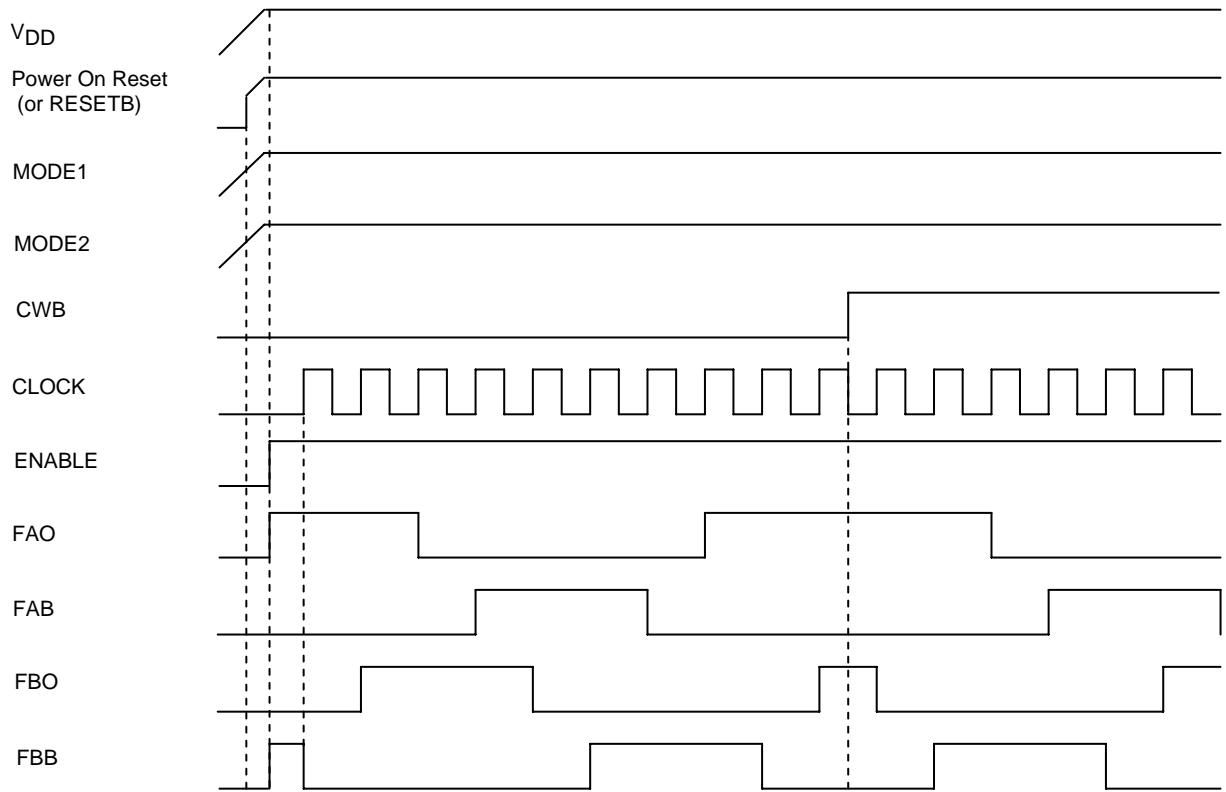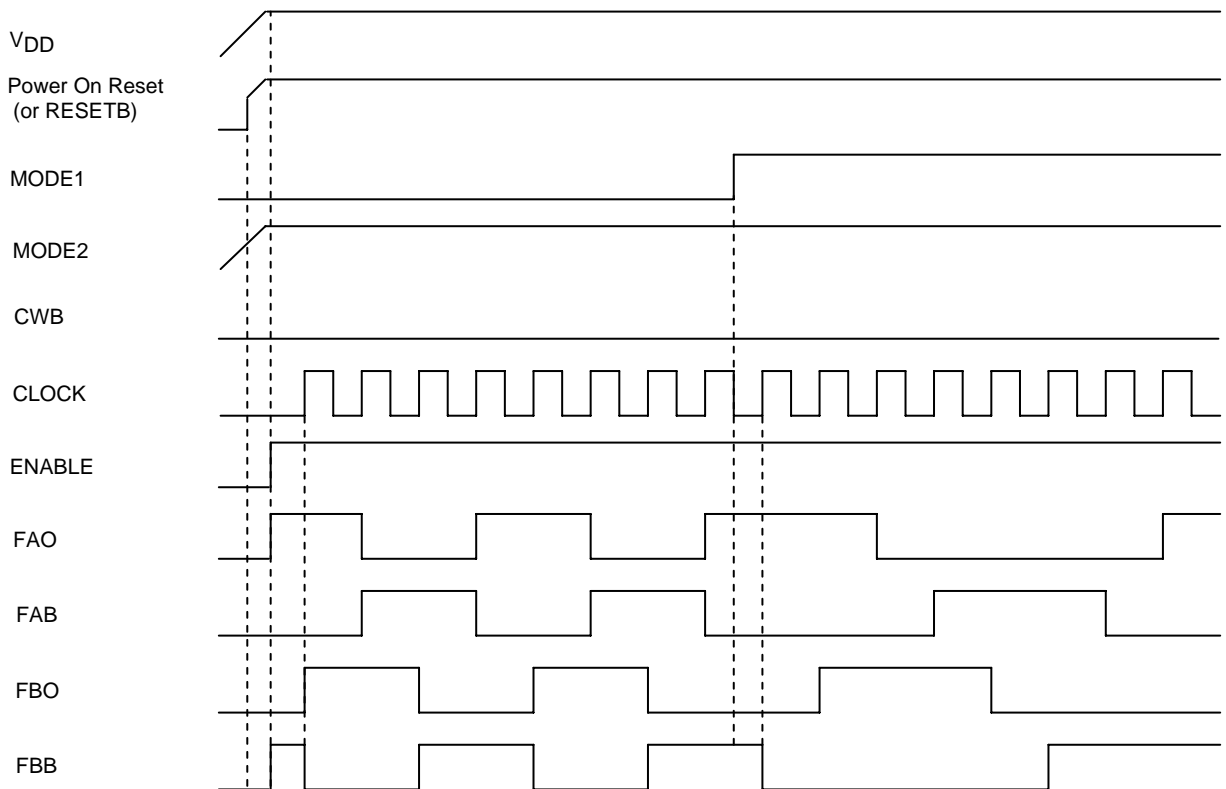
Timing Charts

2-phase excitation

V_{DD}	
Power On Reset (or RESETB)	
MODE1	
MODE2	
CWB	
CLOCK	
ENABLE	
FAO	
FAB	
FBO	
FBB	

1-2 phase excitation

V_{DD}	
Power On Reset (or RESETB)	
MODE1	
MODE2	
CWB	
CLOCK	
ENABLE	
FAO	
FAB	
FBO	
FBB	

1-2 phase excitation (CWB)

2 phase excitation → Switch to 1-2 phase excitation

1-2 phase excitation (ENABLE)

V$_{DD}$	
Power On Reset (or RESETB)	
MODE1	
MODE2	
CWB	
CLOCK	
ENABLE	
FAO	
FAB	
FBO	
FBB	
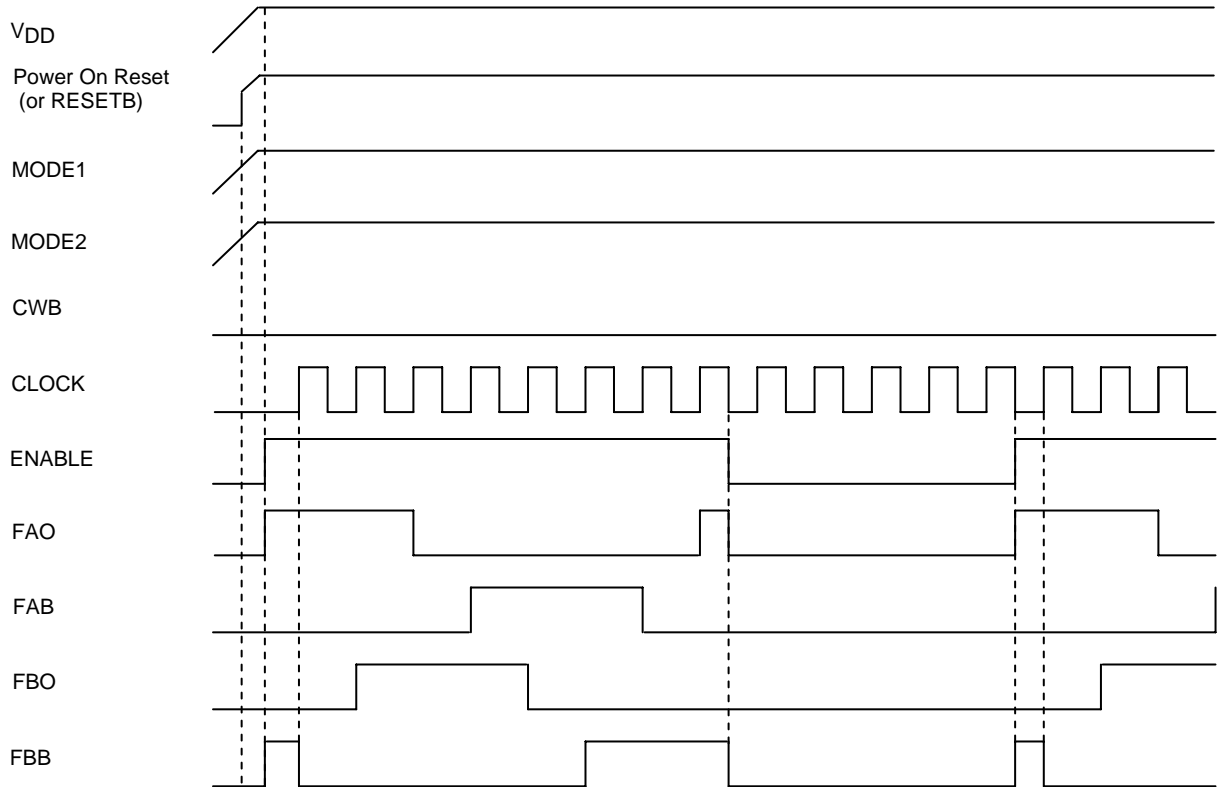
1-2 phase excitation (Hold operation results during fixed CLOCK)

V$_{DD}$	
Power On Reset (or RESETB)	
MODE1	
MODE2	
CWB	
CLOCK	
ENABLE	
FAO	Hold operation
FAB	
FBO	
FBB	
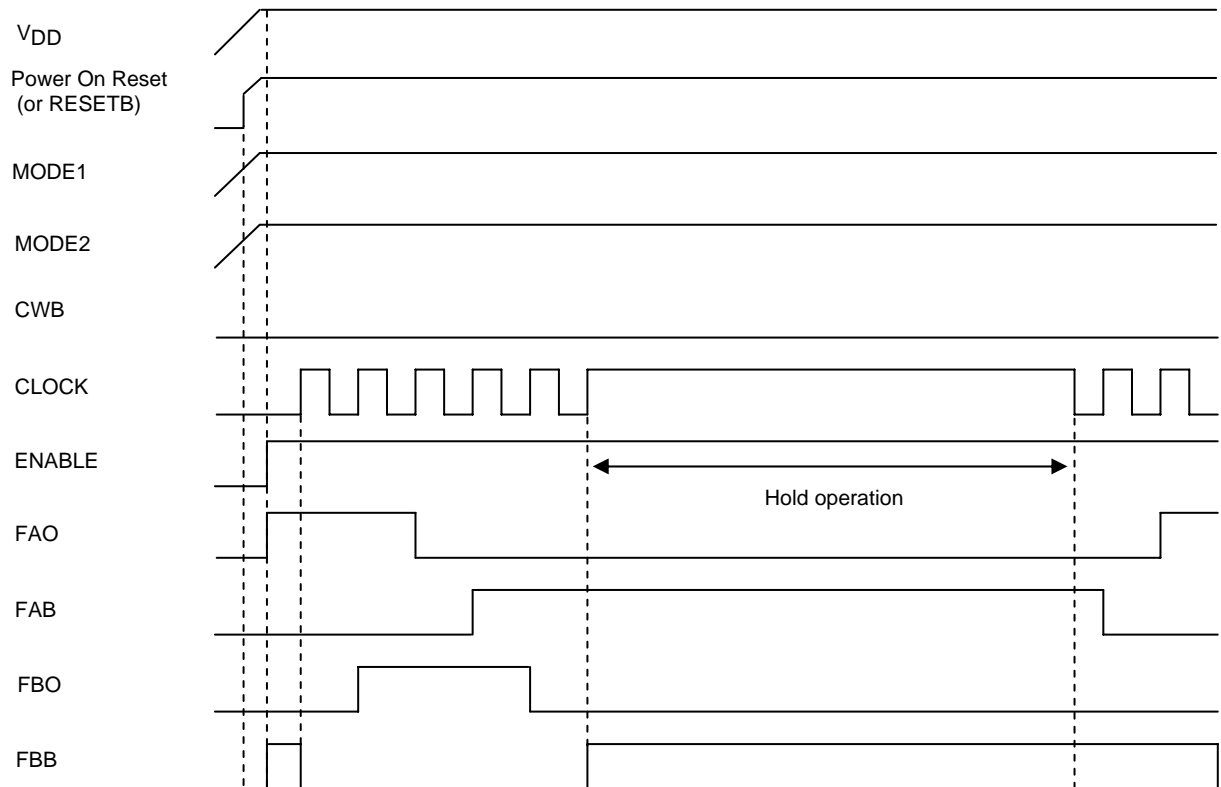
2 phase excitation (MODE 2)
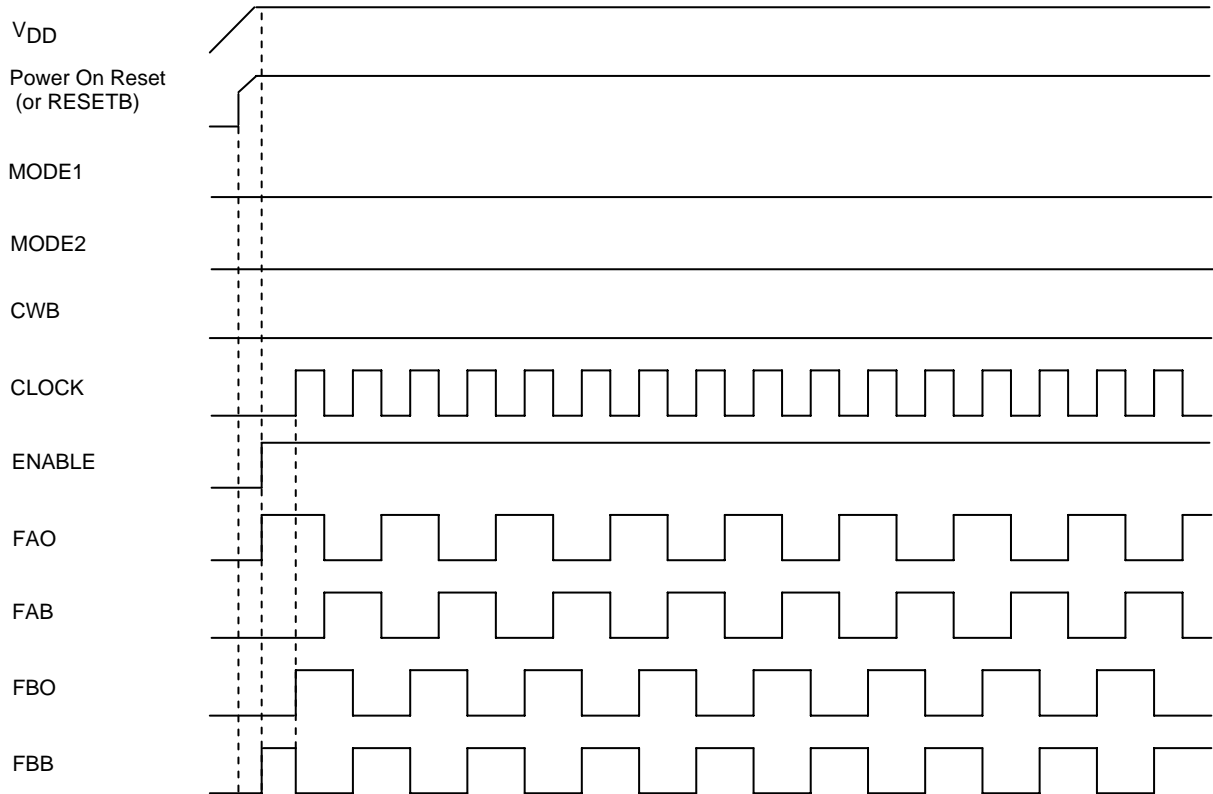
1-2 phase excitation (MODE 2)
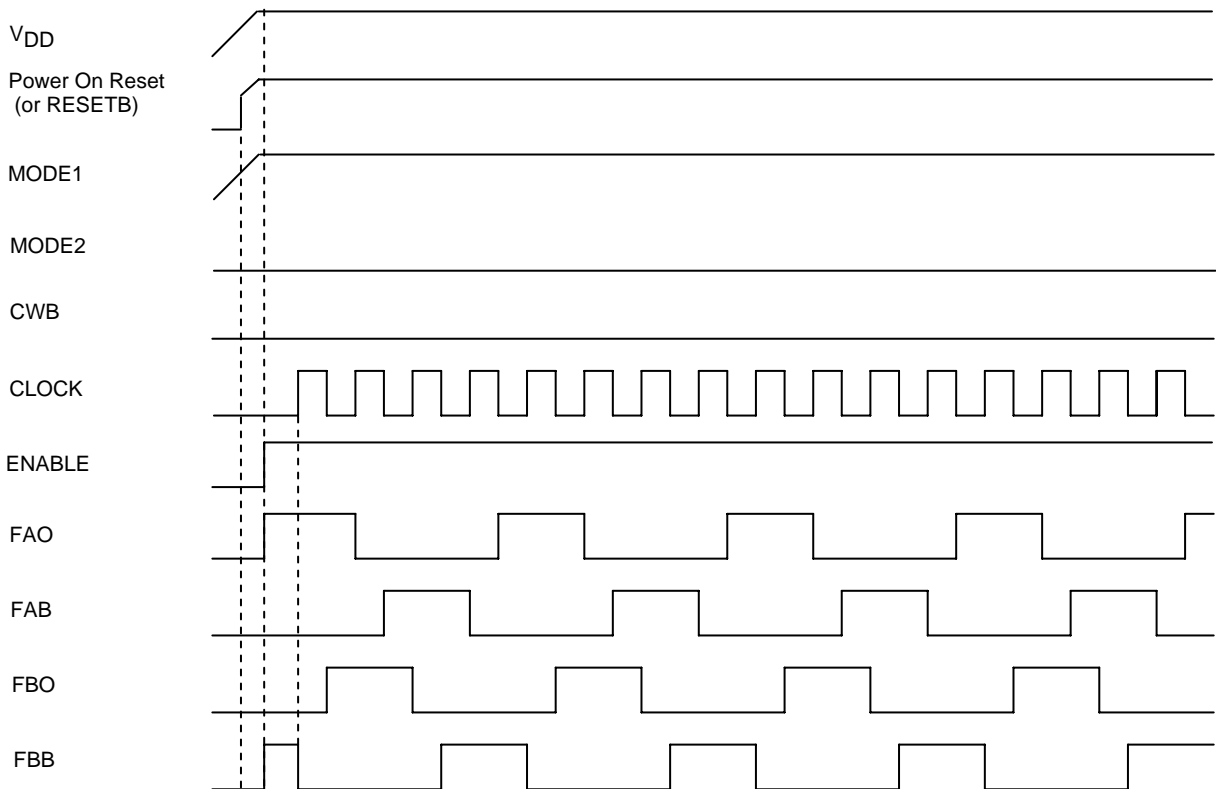
Usage Notes

1. Input signal functions and timing

[ENABLE, CLOCK and power on reset, RESETB (Input signal timing when power is first applied)]
The control IC of the driver is equipped with a power on reset function capable of initializing internal IC operations when power is supplied. A 4V typ setting is used for power on reset. Because the specification for the MOSFET gate voltage is 5V±5%, conduction of current to output at the time of power on reset adds electromotive stress to the MOSFET due to lack of gate voltage. To prevent electromotive stress, be sure to set ENABLE=Low while V_{DD}, which is outside the operating supply voltage, is less than 4.75V.
 In addition, if the RESETB terminal is used to initialize output timing, be sure to allow at least 10μs until CLOCK input.
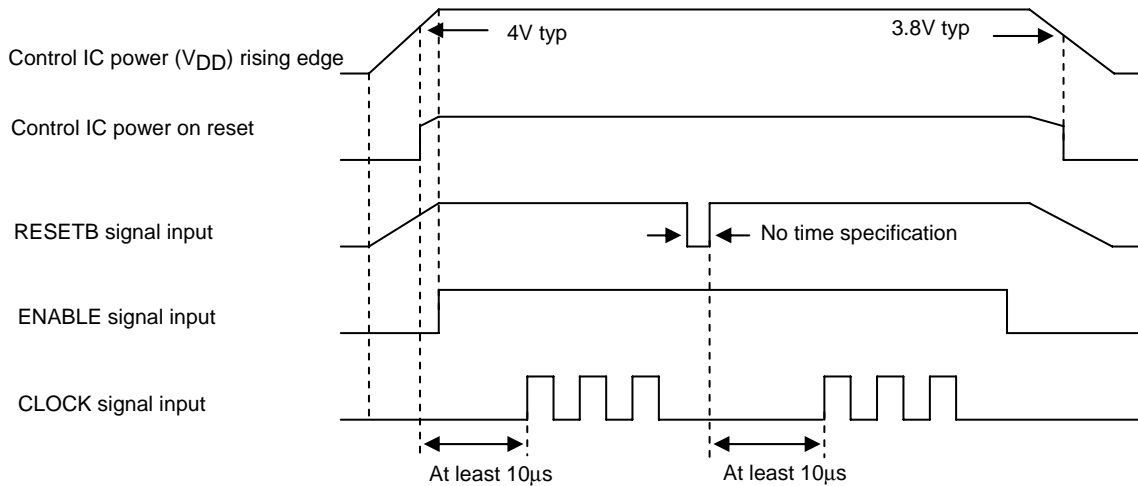
ENABLE, CLOCK, and RESETB Signals Input Timing

[CLOCK (Phase switching clock)]
• Input frequency: DC to 50kHz
• Minimum pulse width: 10μs
• MODE2=1(High) Signals are read on the rising edge.
• MODE2=0(Low) Signals are read on the rising and falling edges.

[CWB (Motor direction setting)]
 The direction of rotation is switched by setting CWB to 1 (high) or 0 (low).
 See the timing charts for details on the operation of the outputs.
 Note: The state of the CWB input must not be changed during the 6.25μs period before and after the rising edge of the CLOCK input.

[ENABLE (Forcible on/off control of the A, AB, B, and BB outputs, and hybrid IC internal operation)]
 ENABLE=1: Normal operation
 ENABLE=0: Outputs A, AB, B, and BB forced to the off state.
        If, during the state where CLOCK signal input is provided, the ENABLE pin is set to 0 and then is later restored to the 1 state, the IC will resume operation with the excitation timing continued from before the point ENABLE was set to 0.
 If sudden stop is applied to the CLOCK signal used for motor rotation, the motor axis may advance beyond the theoretical position due to inertia. To stop at the theoretical position, the SLOW DOWN setting for gradually slowing the CLOCK cycle is required.

[MODE1 and MODE2 (Excitation mode selection)]
 MODE1=0: 2-phase excitation
 MODE2=1: Rising edge of CLOCK
 MODE1=1: 1-2 phase excitation
 MODE2=0: Rising and falling edges of CLOCK
 See the timing charts for details on output operation in these modes.

 Note: The state of the MODE input must not be changed during the 5μs period before and after the rising edge of the
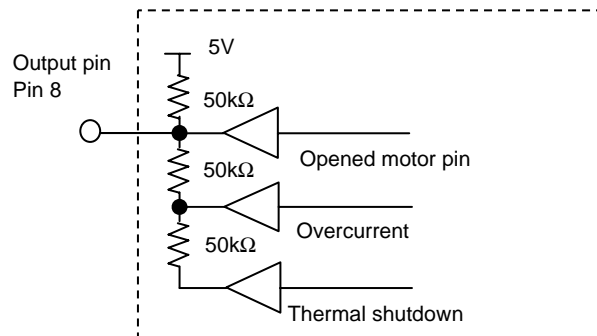   CLOCK input.
       The CLOCK input must not be changed during the period from when the signal changes from high to low or low
       to high in MODE1 or MODE2, till when the signal changes from high to low or low to high in CWB.

[Configuration of Each Input Pin]
<Configuration of the MODE1, MODE2, CLOCK,   <Configuration of the FAULT2 pin>
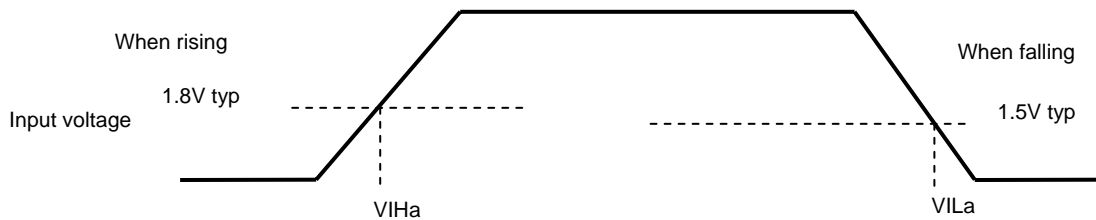 CWB, ENABLE, and RESETB input pins>
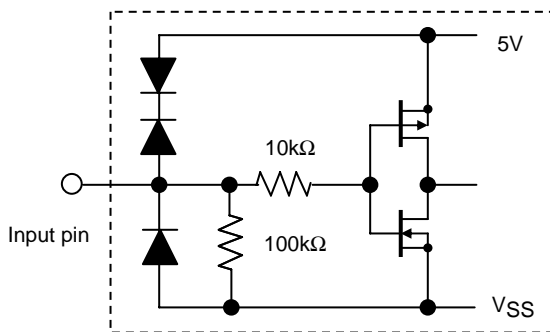
(Configuration of the buffer is open drain.)

All input pins of this driver support schmitt input. Typ specifications at Tc = 25°C are given below. Hysteresis voltage
is 0.3V (VIHa-VILa).

 Input voltage specifications are as follows.
 V_{IH}=2.5V min
 V_{IL}=0.8V max
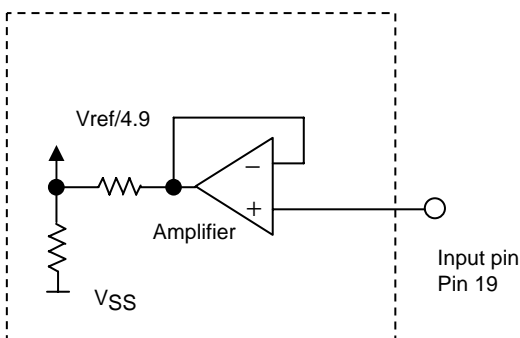
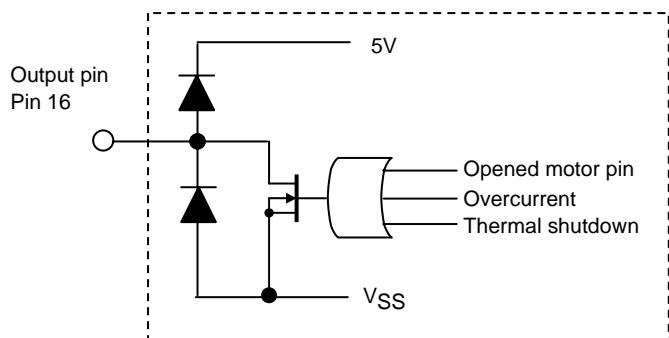<Configuration of the Vref input pin>   <Configuration of the FAULT1 output pin>

<FAULT1, FAULT2 output>

FAULT1 Output

FAULT1 is an open drain output. Low is output if either overcurrent or overheating is detected.

FAULT2 output

Output is resistance divided (3 levels) and the type of abnormality detected is converted to the corresponding output voltage.

- Opened motor pin: 10mV (typ)
- Overcurrent: 2.5V (typ)
- Overheat: 3.3V (typ)

Abnormality detection can be released by a RESETB operation or turning V_{DD} voltage on/off.

<VrefOP output pin configuration>

<VrefOP output>
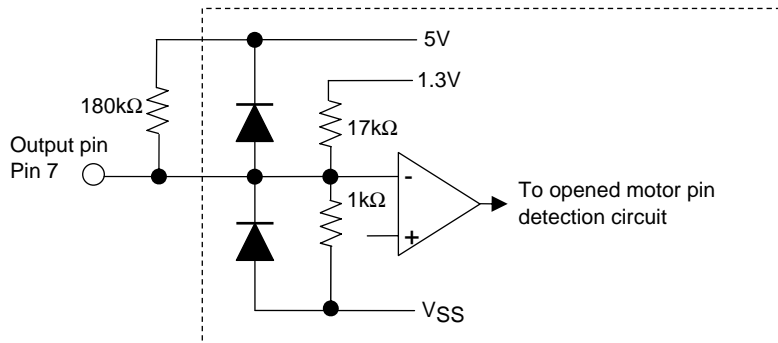
To set the motor current detection circuit operates when pin is open, to monitor the reference voltage VrefOP terminal. It is also possible to set any detectable current by connecting an external pull-up resistor to 5V supply.

<I_{OH}d by setting pull-up resistor current sensing pin 7 open>

When 7 pins open, VrefOP (typ) is 98mV. In this case, detection current I_{OH}d is expressed as follows.

VefOP = I_{OH}d × Rs (Rs: Current detection resistor)

Detection current is 1.1A.

Now, detection current greater than 1.1A is I_{OH}dX. Reference voltage VrefOPX is calculated as above.

Pull-up resistor Rdx by pin 7 is calculated as follows.

RdX = (180 × RTX) ÷ (180 - RTX)

RTX = (5.0V - VrefOPX) ÷ ((1.0588 × VrefOPX) - 0.0765)   (RdX and RTX unit is kΩ)

*To disable pin open detection, please connect a 5V pull-up resistor of 10k to 15kΩ.

2. STK672-630C-E overcurrent detection, overheat detection, and motor terminal open detection functions

Each detection function operates using a latch system and turns output off. Because a RESET signal is required to restore output operations, once the power supply, V_{DD}, is turned off, you must either again apply power on reset with $V_{DD}ON$ or apply a RESETB=High→Low→High signal.

[Motor terminal open detection]
This hybrid IC is equipped with a function for detecting open output terminals to prevent thermal destruction of the MOSFET due to repeated avalanche operation that occurs when an output terminal connected to the motor is open. The open condition is determined by checking the presence or absence of the flyback current that flows in the motor inductance during the off period of the PWM cycle.
Detection is performed by using the fact that the flyback current does not flow when a motor terminal is open.
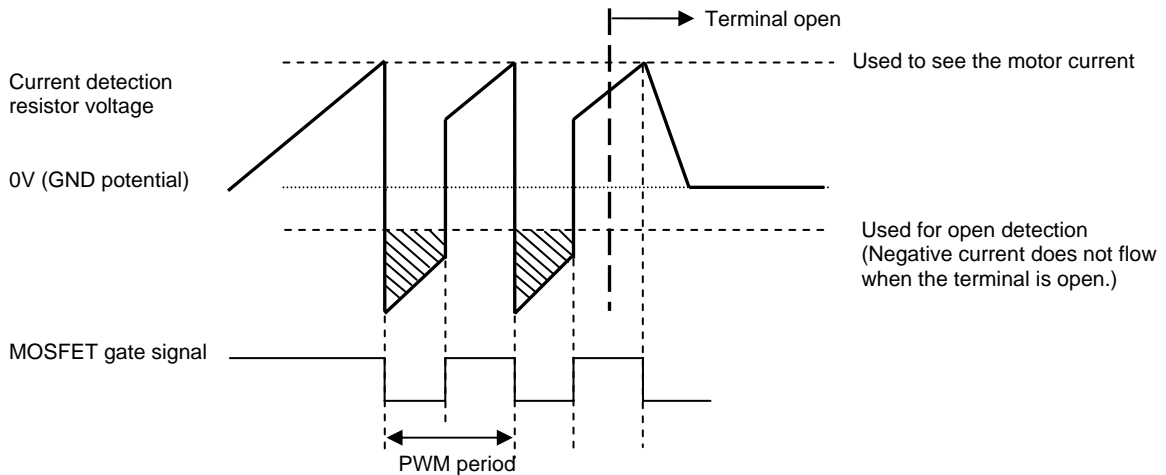
When the current level drops, the difference with the GND potential decreases, making detection difficult. The motor current that can be detected by motor terminal open detection is 0.7A or more with the STK672-630C-E.

<Notes on the ENABLE high edge>
When ENABLE changes from low to high and the STK672-6XXB-E performs constant-current PWM operation that flows a negative current during the 30μs period after the high edge, open detection may activate and stop the driver. The motor current setting voltage Vref must be set so that PWM operation is not performed within a period of 30μs after the high edge.
If the motor current setup voltage is set for the rated motor current, PWM operation is not performed during this 30μs period after the high edge, so this is not a problem.
In addition, there is no problem with operation that lowers the current setting Vref after the motor rated current is reached as shown in the diagram on the following page.
Whether constant-current PWM operation is performed during the 30μs period after the high edge can be judged by substituting the motor L and R values into the formula on the following page.

$Vref = (R02 ÷ (R01+R02)) × 5V$ (or 3.3V)
$I_{OH}1 = (Vref ÷ 4.9) ÷ Rs$ $I_{OH}1$: Motor current value to be set
$I_{OH}2 = (V_{CC} ÷ R) × (1-e^{-tR/L})$ $I_{OH}2$: Current value 30μs after the ENABLE high edge
⇒ Judgment standard: $I_{OH}1 > I_{OH}2$

R01, R02, 5V (or 3.3V): See the Sample Application Circuit documents.
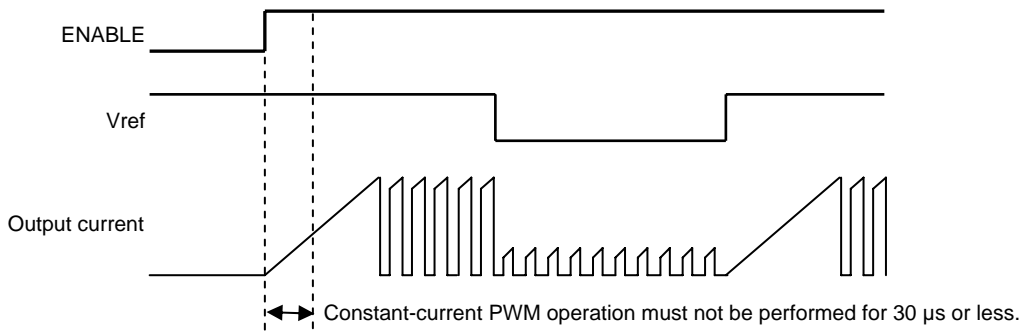Rs: Current detection resistance value (Ω)
V_{CC}: Motor supply voltage (V)
R: Motor winding resistance (Ω)
L: Motor winding inductance (H)
⇒ There is no problem if the $I_{OH}2$ obtained by substituting t = 30μs and the motor L and R values is smaller than the current setting value $I_{OH}1$.

Constant-current PWM operation must not be performed for 30 μs or less.

<Connection of capacitors between output pins and GND prohibited>

Capacitors must not be connected between the phase A (pin 4), phase AB (pin 5), phase B (pin 3) and phase BB (pin 1) outputs and GND. What happens if capacitors are connected is that open-circuit detection may be triggered by the discharge current of the capacitors when the internal MOSFET is set ON. This current is not an inductance current generated by the motor winding but a capacitor current so a negative current will not flow to the other phase in each pair of phases, possibly causing the driver to shut down.

<Excessive external noise>

If, when the motor current rises prior to the PWM operation, a spike-shaped current exceeding the Vref-setting current is generated by excessive external noise, for instance, before the current level (0.7A for the STK672-632C-E and 630C-E, 1.1A for the STK672-642C-E and 640C-E motor drivers) at which motor pin open-circuiting can be detected is reached, the internal MOSFET is set OFF. Since the MOSFET has been set OFF before the actual motor current reaches 0.5A (or 0.8A), the level of the negative current subsequently flowing to the other phase in each pair of phases is low, and it may be judged that no negative current is flowing, possibly causing open-circuit detection to be triggered.

During normal constant-current PWM operation, the duration of 5.5μs, which is equivalent to 25% of the initial operation in the PWM period, corresponds to the section where the current is not detected, and this ensures that no current is detected for the linking part of the current that is generated in this section. The no-current detection section is not synchronized at the current rise prior to the PWM operation so when a spike-shaped current exceeding the Vref-setting current is generated, the MOSFET is set OFF at the stage where the level of the actual motor current is low. As a result, the level of the negative current subsequently flowing to the other phase in each pair of phases is low, and it may be judged that no negative current is flowing, possibly causing open-circuit detection to be triggered.
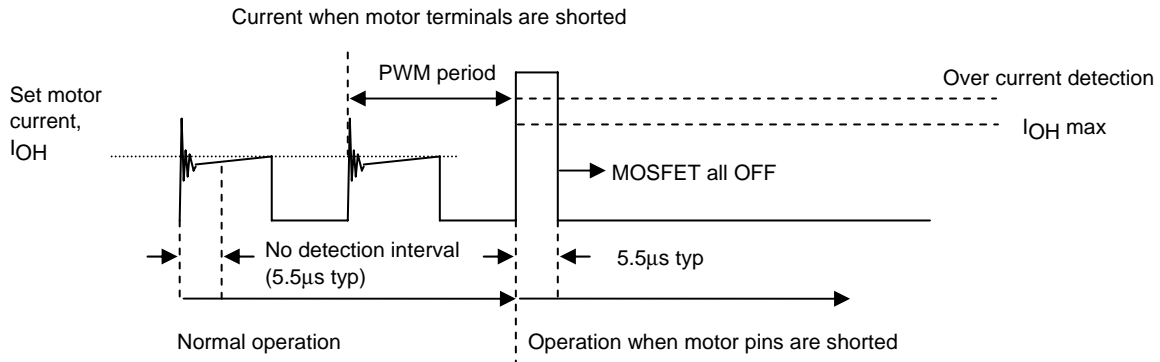

No-current detection time (5.5μs typ)   PWM period
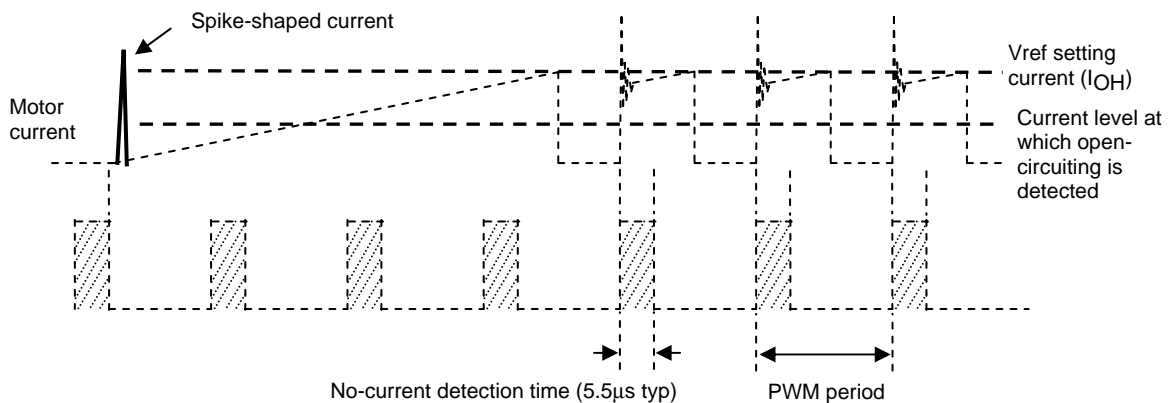
[Over current detection]

This hybrid IC is equipped with a function for detecting overcurrent that arises when the motor burns out or when there is a short between the motor terminals.

Over current detection occurs at 3.5A typ with the STK672-630C-E. and -632C-E.

Current when motor terminals are shorted

PWM period

Over current detection

Set motor current, I_{OH}

I_{OH} max

MOSFET all OFF

No detection interval (5.5µs typ)

5.5µs typ

Normal operation

Operation when motor pins are shorted

Over current detection begins after an interval of no detection (a dead time of 5.5µs typ) during the initial ringing part during PWM operations. The no detection interval is a period of time where over current is not detected even if the current exceeds I_{OH}.

[Overheat detection]

Rather than directly detecting the temperature of the semiconductor device, overheat detection detects the temperature of the aluminum substrate (144°C typ).

Within the allowed operating range recommended in the specification manual, if a heat sink attached for the purpose of reducing the operating substrate temperature, Tc, comes loose, the semiconductor can operate without breaking. However, we cannot guarantee operations without breaking in the case of operations other than those recommended, such as operations at a current exceeding I_{OH} max that occurs before over current detection is activated.

3. Calculating STK672-630C-E HIC Internal Power Loss

The average internal power loss in each excitation mode of the STK672-630C-E can be calculated from the following formulas.

Each excitation mode
2-phase excitation mode
$2PdAVex = 2 \times Vsat \times 0.5 \times CLOCK \times I_{OH} \times t2 + 0.5 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$

1-2 Phase excitation mode
$1\text{-}2PdAVex = 2 \times Vsat \times 0.25 \times CLOCK \times I_{OH} \times t2 + 0.25 \times CLOCK \times I_{OH} \times (Vsat \times t1 + Vdf \times t3)$

Motor hold mode
$HoldPdAVex = (Vsat + Vdf) \times I_{OH}$

        Vsat: Combined voltage of Ron voltage drop + current detection resistance
   Vdf: Combined voltage of the FET body diode + current detection resistance
        CLOCK: Input CLOCK (CLOCK pin signal frequency)
t1, t2, and t3 represent the waveforms shown in the figure below.
        t1: Time required for the winding current to reach the set current (I_{OH})
        t2: Time in the constant current control (PWM) region
        t3: Time from end of phase input signal until inverse current regeneration is complete
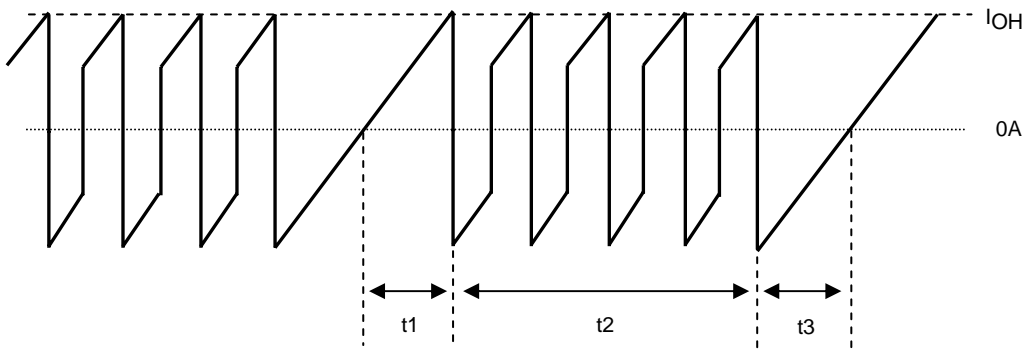
Motor COM Current Waveform Model

    $t1 = (-L/(R+0.33)) \ln (1-((R+0.33)/V_{CC}) \times I_{OH})$
    $t3 = (-L/R) \ln ((V_{CC}+0.33)/(I_{OH} \times R + V_{CC}+0.33))$
    V_{CC}: Motor supply voltage (V)
    L: Motor inductance (H)
    R: Motor winding resistance (Ω)
    I_{OH}: Motor set output current crest value (A)

Relationship of CLOCK, t1, t2, and t3 in each excitation mode
   2-phase excitation mode: $t2 = (2/CLOCK) - (t1+t3)$
   1-2 phase excitation mode: $t2 = (3/CLOCK) - t1$
For Vsat and Vdf, be sure to substitute values from the graphs of Vsat vs. I_{OH} and Vdf vs. I_{OH} while the set current value is I_{OH}.
Then, determine whether a heat sink is required by comparing with the graph of ΔTc vs. Pd based on the average HIC power loss calculated.
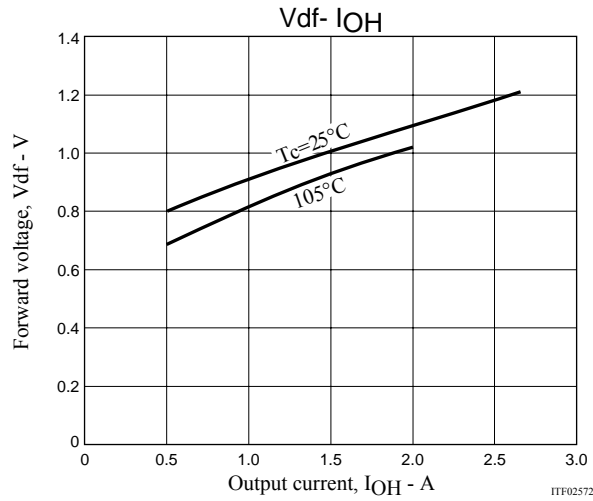When designing a heat sink, refer to the section "Thermal design" found on the next page. The average HIC power loss, PdAV, described above does not have the avalanche's loss. To include the avalanche's loss, be sure to add Equation (2), "STK672-6** Allowable Avalanche Energy Value" to PdAV above. When using this IC without a fin always check for temperature increases in the set, because the HIC substrate temperature, Tc, varies due to effects of convection around the HIC.

STK672-630C-E Output saturation voltage, Vsat - Output current, I_{OH}

Vsat - I_{OH}

Output saturation voltage, Vsat - V vs *Output current, I_{OH} - A*

Curves labeled Tc=105°C and 25°C

ITF02571
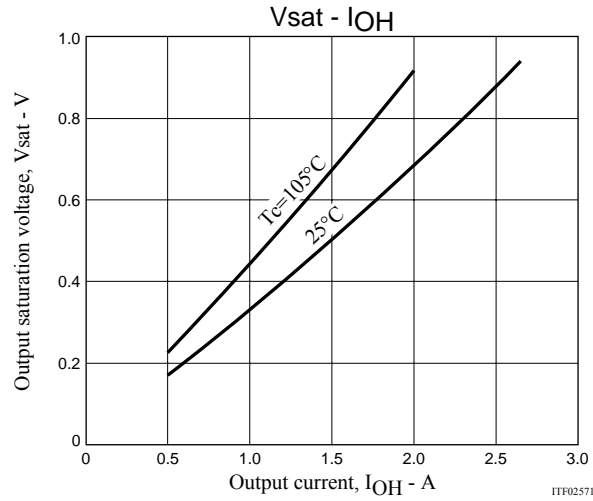
STK672-630C-E Forward voltage, Vdf -Output current, I_{OH}

Vdf - I_{OH}

Forward voltage, Vdf - V vs *Output current, I_{OH} - A*

Curves labeled Tc=25°C and 105°C

ITF02572

Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV

ΔTc - PdAV

Substrate temperature rise, ΔTc - °C vs *Hybrid IC internal average power dissipation, PdAV - W*

ITF02551
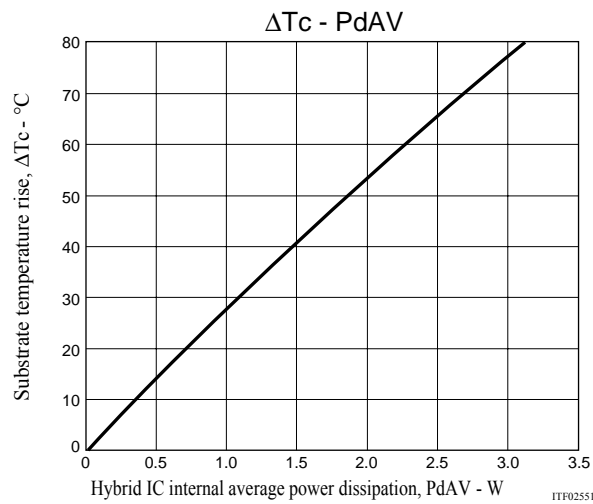
4. STK672-630C-E Allowable Avalanche Energy Value

(1) Allowable Range in Avalanche Mode

When driving a 2-phase stepping motor with constant current chopping using an STK672-6** Series hybrid IC, the waveforms shown in Figure 1 below result for the output current, I_D, and voltage, V_{DS}.
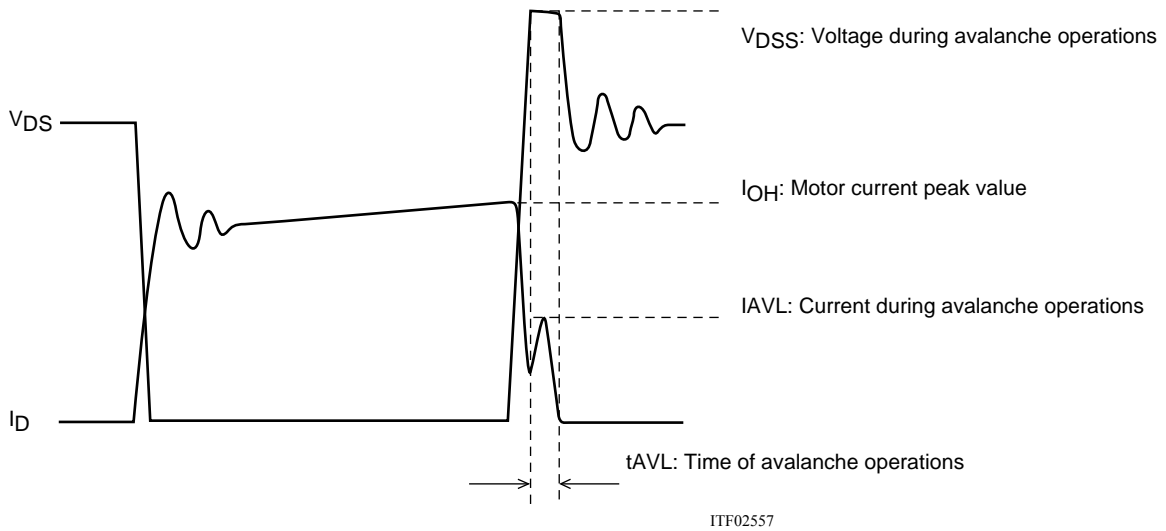

V_{DSS}: Voltage during avalanche operations

I_{OH}: Motor current peak value

IAVL: Current during avalanche operations

tAVL: Time of avalanche operations

ITF02557

Figure 1 Output Current, I_D, and Voltage, V_{DS}, Waveforms 1 of the STK672-6** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

When operations of the MOSFET built into STK672-6** Series ICs is turned off for constant current chopping, the I_D signal falls like the waveform shown in the figure above. At this time, the output voltage, V_{DS}, suddenly rises due to electromagnetic induction generated by the motor coil.

In the case of voltage that rises suddenly, voltage is restricted by the MOSFET V_{DSS}. Voltage restriction by V_{DSS} results in a MOSFET avalanche. During avalanche operations, I_D flows and the instantaneous energy at this time, EAVL1, is represented by Equation (1).

$$EAVL1 = V_{DSS} \times IAVL \times 0.5 \times tAVL \text{ --- (1)}$$

V_{DSS}: V units, IAVL: A units, tAVL: sec units

The coefficient 0.5 in Equation (1) is a constant required to convert the IAVL triangle wave to a square wave.

During STK672-6** Series operations, the waveforms in the figure above repeat due to the constant current chopping operation. The allowable avalanche energy, EAVL, is therefore represented by Equation (2) used to find the average power loss, PAVL, during avalanche mode multiplied by the chopping frequency in Equation (1).

$$PAVL = V_{DSS} \times IAVL \times 0.5 \times tAVL \times fc \text{ -- (2)}$$

fc: Hz units (fc is set to the PWM frequency of 50kHz.)

For V_{DSS}, IAVL, and tAVL, be sure to actually operate the STK672-6** Series and substitute values when operations are observed using an oscilloscope.

Ex. If V_{DSS}=110V, IAVL=1A, tAVL=0.2μs when using a STK672-630C-E driver, the result is:

$PAVL = 110 \times 0.5 \times 0.5 \times 0.2 \times 10^{-6} \times 50 \times 10^{3} = 0.28W$

V_{DSS}=110V is a value actually measured using an oscilloscope.

The allowable loss range for the allowable avalanche energy value, PAVL, is shown in the graph in Figure 3. When examining the avalanche energy, be sure to actually drive a motor and observe the I_D, V_{DSS}, and tAVL waveforms during operation, and then check that the result of calculating Equation (2) falls within the allowable range for avalanche operations.

(2) I_D and V_{DSS} Operating Waveforms in Non-avalanche Mode

Although the waveforms during avalanche mode are given in Figure 1, sometimes an avalanche does not result during actual operations.

Factors causing avalanche are listed below.

• Poor coupling of the motor's phase coils (electromagnetic coupling of A phase and AB phase, B phase and BB phase).

• Increase in the lead inductance of the harness caused by the circuit pattern of the P.C. board and motor.

• Increases in V_{DSS}, tAVL, and IAVL in Figure 1 due to an increase in the supply voltage from 24V to 36V.

If the factors above are negligible, the waveforms shown in Figure 1 become waveforms without avalanche as shown in Figure 2.

Under operations shown in Figure 2, avalanche does not occur and there is no need to consider the allowable loss range of PAVL shown in Figure 3.
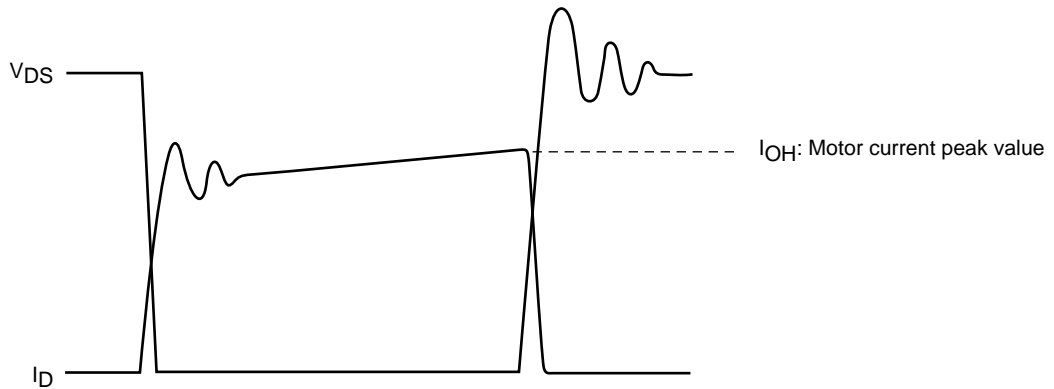
ITF02558

Figure 2 Output Current, I_D, and Voltage, V_{DS}, Waveforms 2 of the STK672-6** Series when Driving a 2-Phase Stepping Motor with Constant Current Chopping

Figure 3 Allowable Loss Range, PAVL-I_{OH} During STK672-630C-E Avalanche Operations
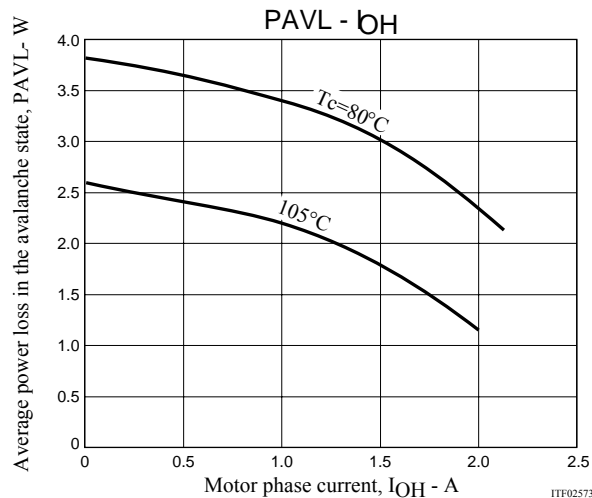
ITF02573

Note:

The operating conditions given above represent a loss when driving a 2-phase stepping motor with constant current chopping.

Because it is possible to apply 2.6W or more at I_{OH}=0A, be sure to avoid using the MOSFET body diode that is used to drive the motor as a zener diode.

5. Thermal design

[Operating range in which a heat sink is not used]
Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.
The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to "Calculating Internal HIC Loss for the STK672-630C-E in the specification document.
Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,
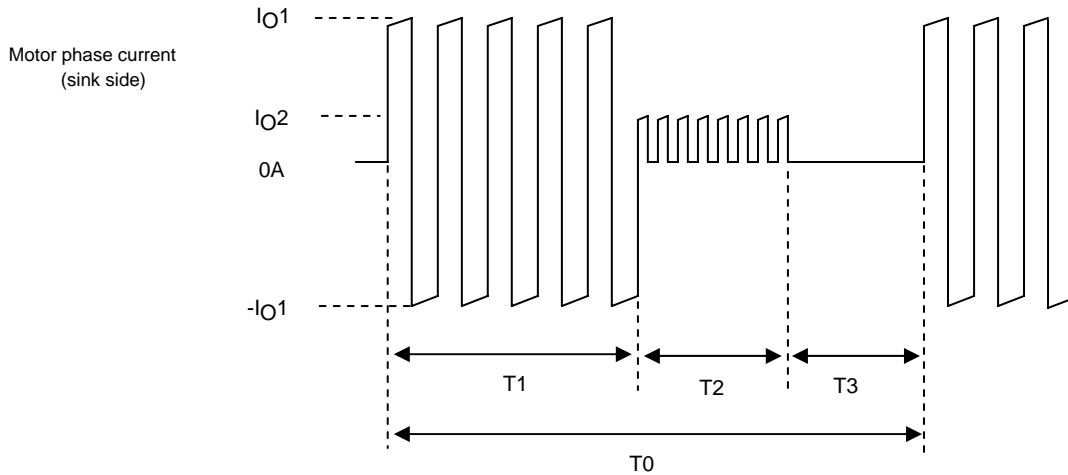
Figure 1 Motor Current Timing

T1: Motor rotation operation time
T2: Motor hold operation time
T3: Motor current off time
T2 may be reduced, depending on the application.
T0: Single repeated motor operating cycle
I_O1 and I_O2: Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.
The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

$$\text{PdAV}= (T1{\times}P1+T2{\times}P2+T3{\times}0) \div TO \text{ ---------------------------- (I)}$$
$$\text{(Here, P1 is the PdAV for } I_O1 \text{ and P2 is the PdAV for } I_O2\text{)}$$

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]
Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of θc-a in Equation (II) below and the graph depicted in Figure 3.

$$\theta\text{c-a}= (\text{Tc max-Ta}) \div \text{PdAV} \text{ --------------------------- (II)}$$
$$\text{Tc max: Maximum operating substrate temperature} =105°C$$
$$\text{Ta: HIC ambient temperature}$$

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.
The average HIC power loss, PdAV, described above represents the power loss when there is no avalanche operation. To add the loss during avalanche operations, be sure to add Equation (2), "Allowable STK672-6** Avalanche Energy Value", to PdAV.

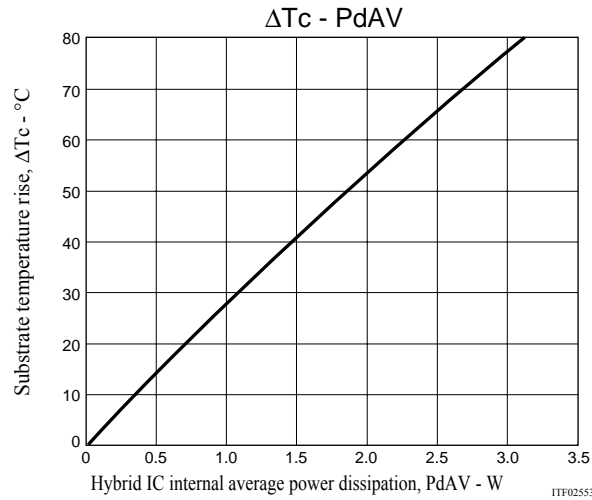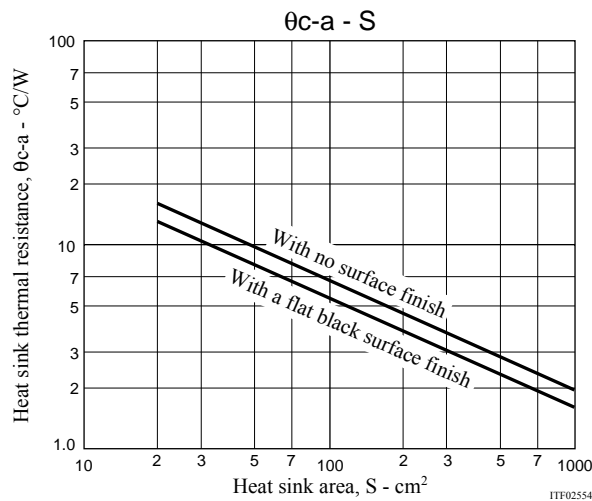Figure 2 Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV

ΔTc - PdAV

Substrate temperature rise, ΔTc - °C (y-axis)
Hybrid IC internal average power dissipation, PdAV - W (x-axis)

ITF02553

Figure 3 Heat sink area (Board thickness: 2mm) - θc-a

θc-a - S

Heat sink thermal resistance, θc-a - °C/W (y-axis)
With no surface finish
With a flat black surface finish
Heat sink area, S - cm^2 (x-axis)

ITF02554

6. Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta
   Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink.
   The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta.
   Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

Allowable power dissipation, PdPK(no heat sink) - Ambient temperature, Ta

PdPK - Ta

Allowable power dissipation, PdPK - W (y-axis)
Ambient temperature, Ta - °C (x-axis)

ITF02511
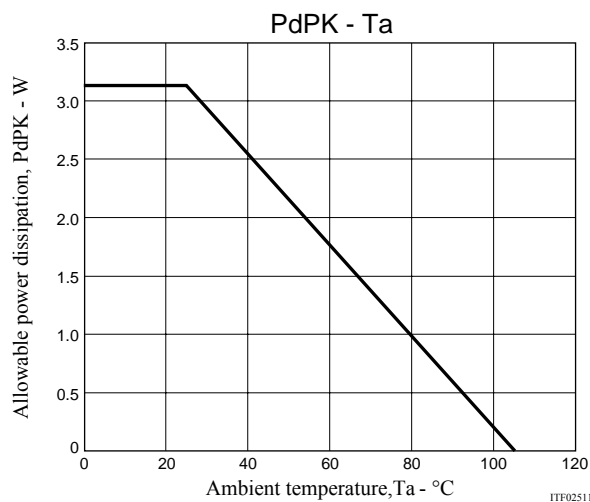
7. Example of Stepping Motor Driver Output Current Path (1-2 phase excitation)

2-phase stepping motor

I_OA I_OAB

FAULT2 VrefOP A   AB   B   BB
   8   7   4   5   3   1

V_{DD}=5V 9 V_{DD}

                              F1   F2   F3   F4
MODE1 10   Excitatin mode setting
N.C   11
MODE2 17   Phase advnce counter   Phase excitation signal generation   FAO / FAB / FBO / FBB
CLOCK 12
CWB   13

RESETB 14   Power on reset   Latch   Opened motor pin detection
ENABLE 15   Latch   Over current detection

FAULT1 16   FAULT1, FAULT2 signal   Chopper circuit   AI / BI

             Over heat detection   Latch   Vref/4.9
                                              Amp V_{SS} Vref

N.C   18
Vref   19 V_{SS}

R1   R2

V_{CC} 24V

C02 at least 100μF

P.G2 (2)
P.G1 (6)   P.GND

CLOCK

Phase A output current I_OA

PWM operations

When PWM operations of I_OA are OFF, for I_OAB, negative current flows through the parasitic diode, F2.

Phase AB output current I_OAB

When PWM operations of I_OAB are OFF, for I_OA, negative current flows through the parasitic diode, F1.

8. Other Notes on Use

In addition to the "Notes" indicated in the Sample Application Circuit, care should also be given to the following contents during use.

(1) Allowable operating range

Operation of this product assumes use within the allowable operating range. If a supply voltage or an input voltage outside the allowable operating range is applied, an overvoltage may damage the internal control IC or the MOSFET.

If a voltage application mode that exceeds the allowable operating range is anticipated, connect a fuse or take other measures to cut off power supply to the product.

(2) Input pins

If the input pins are connected directly to the PC board connectors, electrostatic discharge or other overvoltage outside the specified range may be applied from the connectors and may damage the product. Current generated by this overvoltage can be suppressed to effectively prevent damage by inserting 100Ω to $1k\Omega$ resistors in lines connected to the input pins.

Take measures such as inserting resistors in lines connected to the input pins.

(3) Power connectors

If the motor power supply V_{CC} is applied by mistake without connecting the GND part of the power connector when the product is operated, such as for test purposes, an overcurrent flows through the V_{CC} decoupling capacitor, C1, to the parasitic diode between the V_{DD} of the internal control IC and GND, and may damage the power supply pin block of the internal control IC.

To prevent destruction in this case, connect a 10Ω resistor to the V_{DD} pin, or insert a diode between the V_{CC} decoupling capacitor C1 GND and the V_{DD} pin.
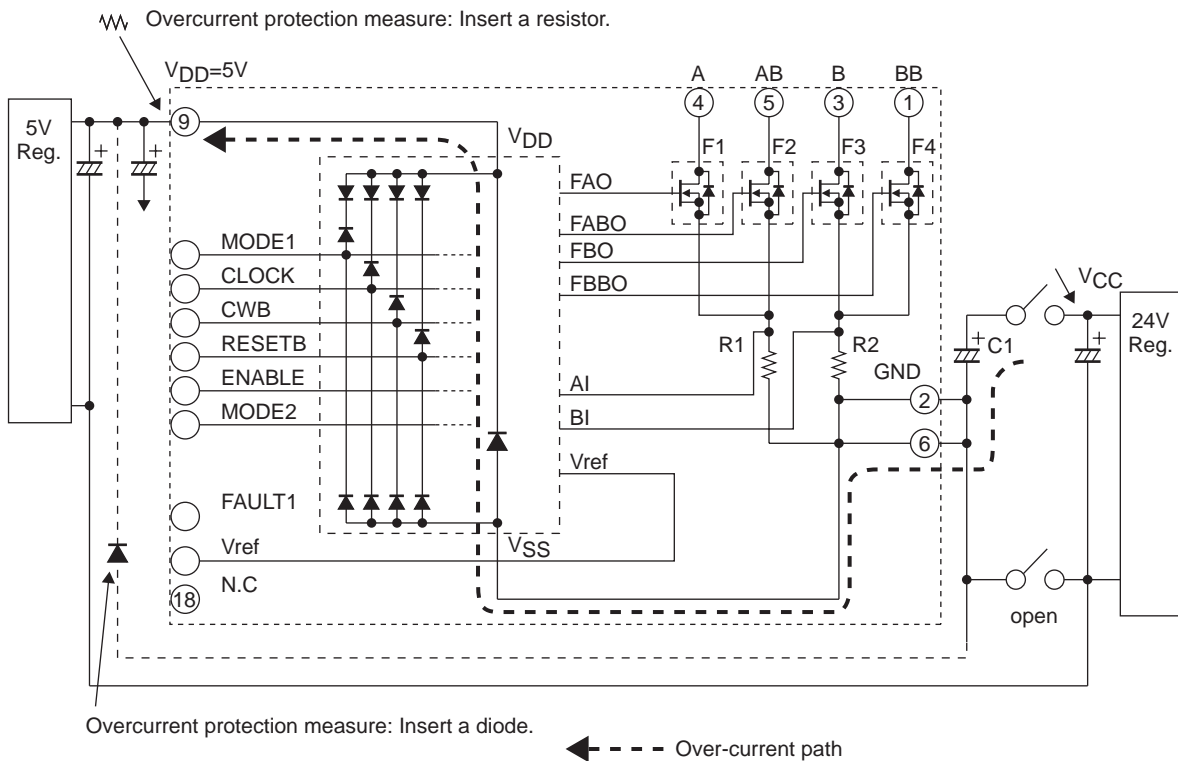
(4) Input Signal Lines

1) Do not use an IC socket to mount the driver, and instead solder the driver directly to the PC board to minimize fluctuations in the GND potential due to the influence of the resistance component and inductance component of the GND pattern wiring.

2) To reduce noise caused by electromagnetic induction to small signal lines, do not design small signal lines (sensor signal lines, and 5V or 3.3V power supply signal lines) that run parallel in close proximity to the motor output line A (Pin 4), AB (Pin 5), B (Pin 3), or BB (Pin 1) phases.

3) Pin 11 of this product are N.C pins. Do not connect any wiring to these pins.

(5) When mounting multiple drivers on a single PC board

When mounting multiple drivers on a single PC board, the GND design should mount a V_{CC} decoupling capacitor, C1, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.
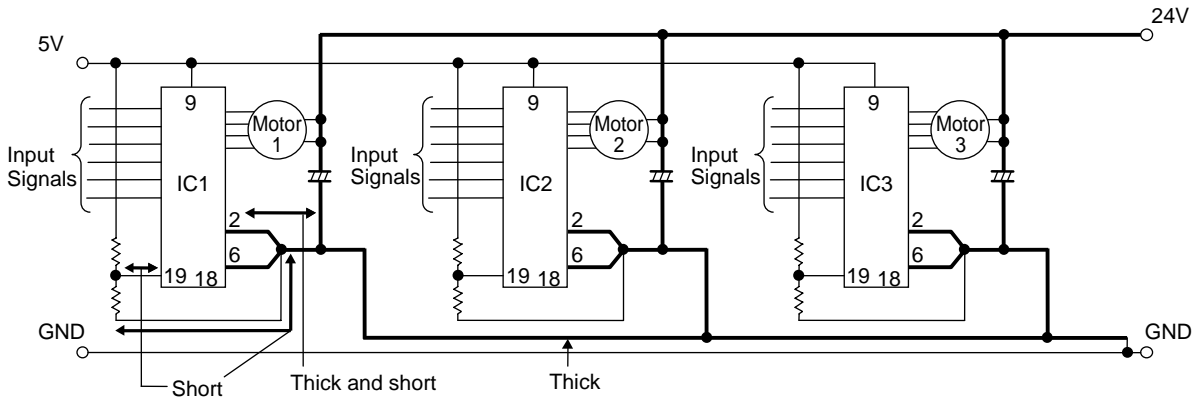
(6) V_{CC} operating limit

When the output (for example F1) of a 2-phase stepping motor driver is turned OFF, the AB phase back electromotive force eab produced by current flowing to the paired F2 parasitic diode is induced in the F1 side, causing the output voltage VFB to become twice or more the V_{CC} voltage. This is expressed by the following formula.

$$VFB = V_{CC} + eab$$
$$= V_{CC} + V_{CC} + I_{OH} \times RM + Vdf\,(1.5\,V)$$

V_{CC}: Motor supply voltage, I_{OH}: Motor current set by Vref

Vdf: Voltage drop due to F2 parasitic diode and current detection resistor R1, RM: Motor winding resistance value

Using the above formula, make sure that VFB is always less than the MOSFET withstand voltage of 100V. This is because there is a possibility that operating limit of V_{CC} falls below the allowable operating range of 46V, due to the RM and I_{OH} specifications.
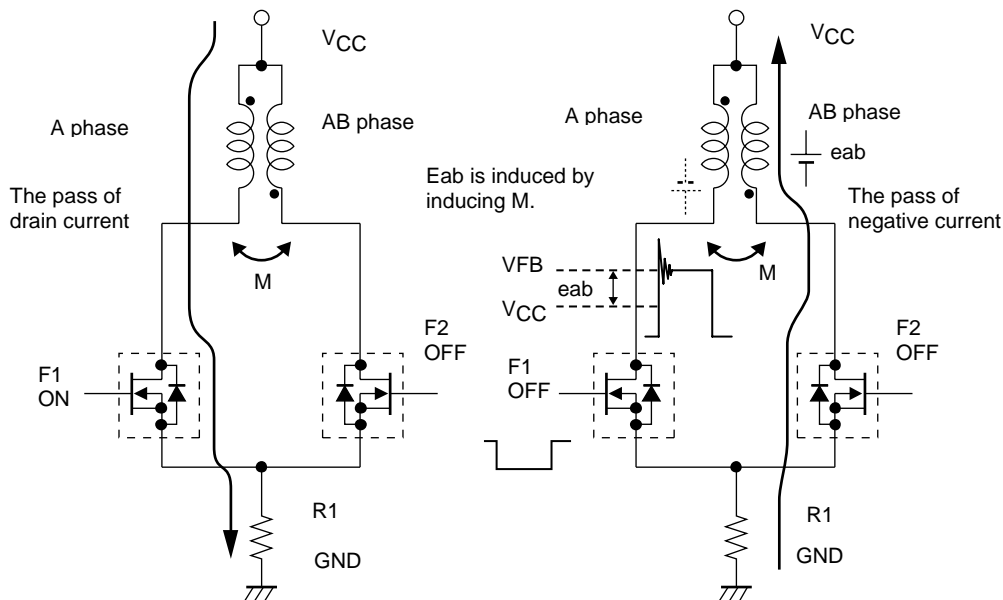
The oscillating voltage in excess of VFB is caused by LCRM (inductance, capacitor, resistor, mutual inductance) oscillation that includes micro capacitors C, not present in the circuit. Since M is affected by the motor characteristics, there is some difference in oscillating voltage according to the motor specifications. In addition, constant voltage drive without constant current drive enables motor rotation at $V_{CC} \geq 0V$.