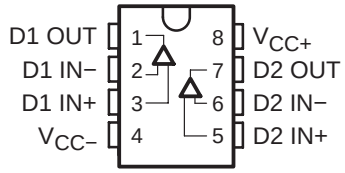
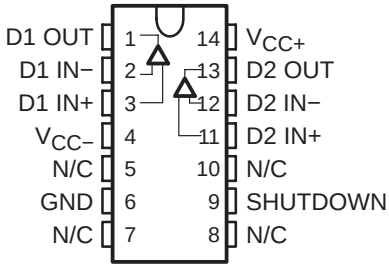
- **Remote Terminal ADSL Line Driver**
  - **Ideal for Both Full Rate ADSL and G.Lite**
  - **Compatible With 1:1 Transformer Ratio**
- **Low 2.1 pA/√Hz Noninverting Current Noise**
  - **Reduces Noise Feedback Through Hybrid Into Downstream Channel**
- **Wide Supply Voltage Range ±5 V to ±15 V**
  - **Ideal for ±12-V Operation**
- **Wide Output Swing**
  - **43-Vpp Differential Output Voltage, R_L = 200 Ω, ±12-V Supply**
- **High Output Current**
  - **350 mA (typ)**
- **High Speed**
  - **120 MHz (−3 dB, G=1, ±12 V, R_L = 25 Ω)**
  - **1200 V/μs Slew Rate (G = 4, ±12 V)**
- **Low Distortion, Single-Ended, G = 4**
  - **−79 dBc (250 kHz, 2 V_{pp}, 100-Ω load)**
- **Low Power Shutdown (THS6043)**
  - **300-μA Total Standby Current**
- **Thermal Shutdown and Short-Circuit Protection**
- **Standard SOIC, SOIC PowerPAD™ and TSSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6042
SOIC (D) AND
SOIC PowerPAD™ (DDA) PACKAGE
(TOP VIEW)

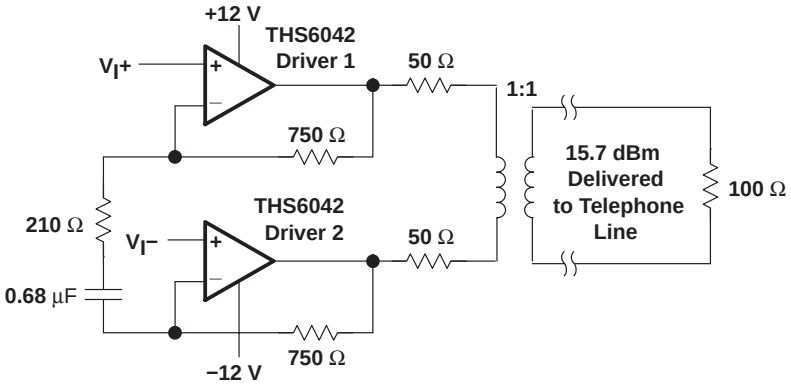


THS6043
SOIC (D) AND
TSSOP PowerPAD™ (PWP) PACKAGE
(TOP VIEW)



description

The THS6042/3 is a high-speed line driver ideal for driving signals from the remote terminal to the central office in asymmetrical digital subscriber line (ADSL) applications. It can operate from a ±12-V supply voltage while drawing only 8.2 mA of supply current per channel. It offers low –79 dBc total harmonic distortion driving a 100-Ω load (2 Vpp). The THS6042/3 offers a high 43-Vpp differential output swing across a 200-Ω load from a ±12-V supply. The THS6043 features a low-power shutdown mode, consuming only 300 μA quiescent current per channel. The THS6042/3 is packaged in standard SOIC, SOIC PowerPAD, and TSSOP PowerPAD packages.



RELATED PRODUCTS

DEVICE	DESCRIPTION
THS6052/3	175-mA, ±12 ADSL CPE line driver
THS6092/3	275-mA, +12 V ADSL CPE line driver
OPA2677	380-mA, +12 V ADSL CPE line driver
THS6062	±15 V to ± 5 V Low noise ADSL receiver
OPA2822	±6 V to 5 V Low noise ADSL receiver

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS6042CD	THS6042CDDA	THS6043CD	THS6043CPWP	THS6042EVM THS6043EVM
−40°C to 85°C	THS6042ID	THS6042IDDA	THS6043ID	THS6043IPWP	—

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage . . . . . $\pm V_{CC}$
Output current (see Note 1) . . . . . 450 mA
Differential input voltage . . . . . ± 4 V
Maximum junction temperature . . . . . 150°C
Total power dissipation at (or below) 25°C free-air temperature . . . . . See Dissipation Ratings Table
Operating free-air temperature, T_A: Commercial . . . . . 0°C to 70°C
Industrial . . . . . −40°C to 85°C
Storage temperature, T_{stg} : Commercial . . . . . −65°C to 125°C
Industrial . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6042 and THS6043 may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}	θ_{JC}	T_A = 25°C T_J = 150°C POWER RATING
D-8	95°C/W‡	38.3°C/W‡	1.32 W
DDA	45.8°C/W‡	9.2°C/W‡	2.73 W
D-14	66.6°C/W‡	26.9°C/W‡	1.88 W
PWP	37.5°C/W	1.4°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the Θ_{JA} is168°C/W for the D−8 package and 122.3°C/W for the D−14 package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, $R_{(FEEDBACK)}$ = 750 Ω, R_L = 100 Ω (unless otherwise noted)

dynamic performance

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (−3 dB)	R_L = 25 Ω	G = 1, R_F = 560 Ω	V_{CC} = ±6 V, ±12 V		120		MHz
			G = 2, R_F = 500 Ω			95		
			G = 4, R_F = 390 Ω			75		
		R_L = 100 Ω	G = 4, R_F = 390 Ω	V_{CC} = ±6 V, ±12 V		100		
			G = 8, R_F = 280 Ω			65		
SR	Slew rate (see Note 2)	R_L = 25 Ω	G = 2, R_F = 390 Ω, V_O = 5 V_{pp}	V_{CC} = ±15 V		1000		V/µs
				V_{CC} = ±12 V		900		
				V_{CC} = ±6 V		600		
		R_L = 100 Ω	G = 4, R_F = 750 Ω, V_O = 12 V_{pp}	V_{CC} = ±15 V		1400		
				V_{CC} = ±12 V		1200		
			G = 4, R_F = 750 Ω, V_O = 5 V_{pp}	V_{CC} = ±6 V		600		

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion (single-ended configuration) (R_F = 390 Ω)		G = 4, R_L = 100 Ω, V_{CC} = ±12 V, f = 250 kHz	$V_{O(pp)}$ = 2 V		−79		dBc
				$V_{O(pp)}$ = 16 V		−75		
			G = 4, R_L = 25 Ω, V_{CC} = ±6 V, f = 250 kHz	$V_{O(pp)}$ = 2 V		−72		
				$V_{O(pp)}$ = 7 V		−68		
V_n	Input voltage noise		V_{CC} = ±6 V, ±12 V	f = 10 kHz		2.2		nV/√Hz
I_n	Input current noise	+Input	V_{CC} = ±6 V, ±12 V, ±15 V	f = 10 kHz		2.1		pA/√Hz
		−Input				11		
	Crosstalk		f = 250 kHz, V_{CC} = ±6 V, ±12 V, R_F = 430 Ω, R_L = 100 Ω	V_O = 2 Vpp, G = 4		−71		dBc
			f = 250 kHz, V_{CC} = ±6 V, ±12 V, R_F = 390 Ω, R_L = 25 Ω			−65		

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, $R_{(FEEDBACK)}$ = 750 Ω, R_L = 100 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_{CC} = ±6 V, ±12 V	T_A = 25°C		9.5	16	mV
			T_A = full range			21	
	Differential offset voltage		T_A = 25°C		1	5	
			T_A = full range			7	
	Offset drift		T_A = full range		20		µV/°C
I_{IB}	− Input bias current	V_{CC} = ±6 V, ±12 V	T_A = 25°C		3.5	10	µA
			T_A = full range			12	
	+ Input bias current		T_A = 25°C		1	5	
			T_A = full range			6	
	Differential input bias current		T_A = 25°C		3.5	10	
			T_A = full range			12	
Z_{OL}	Open-loop transimpedance	R_L = 1 kΩ	V_{CC} = ±6 V, ±12 V		1		MΩ

input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range	V_{CC} = ±12 V	T_A = 25°C	±9.6	±10.1		V
			T_A = full range	±9.5			
		V_{CC} = ±6V	T_A = 25°C	±3.7	±4.2		
			T_A = full range	±3.6			
CMRR	Common-mode rejection ratio	V_{CC} = ±6 V, ±12 V	T_A = 25°C	59	68		V
			T_A = full range	55			
R_I	Input resistance	+ Input			1.5		MΩ
		− Input			15		Ω
C_i	Input capacitance				2		pF

output characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	Single ended 100-mV overdrive	R_L = 25 Ω	V_{CC} = ±12 V	±7.5	±9.1		V
				V_{CC} = ±6 V	±4.1	±4.6		
			R_L = 100 Ω	V_{CC} = ±12 V	±10.3	±10.8		
				V_{CC} = ±6 V	±4.5	±4.9		
I_O	Output current		R_L = 25 Ω,	V_{CC} = ± 12 V	300	350		mA
			R_L = 10 Ω,	V_{CC} = ±6 V	230	260		
I_{OS}	Short-circuit current		R_L = 0 Ω,	V_{CC} = ±12 V		400		mA
r_o	Output resistance		Open loop			15		Ω

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±12 V, $R_{(FEEDBACK)}$ = 750 Ω, R_L = 100 Ω (unless otherwise noted) (continued)

power supply

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply			±4.5		±16.5	V
		Single supply			9		33	
I_{CC}	Quiescent current (each driver)		V_{CC} = ±12 V	T_A = 25°C		8.2	10.5	mA
				T_A = full range			11.5	
			V_{CC} = ±6 V	T_A = 25°C		7.4	9.5	
				T_A = full range			10.5	
PSRR	Power supply rejection ratio		V_{CC} = ±12 V	T_A = 25°C	−65	−72		dB
				T_A = full range	−62			
			V_{CC} = ±6 V	T_A = 25°C	−62	−69		
				T_A = full range	−60			

shutdown characteristics (THS6043 only)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(SHDN)}$	Shutdown pin voltage for power up	V_{CC} = ±6 V, ±12 V, GND = 0 V (GND Pin as Reference)			0.8	V
$V_{IH(SHDN)}$	Shutdown pin voltage for power down	V_{CC} = ±6 V, ±12 V, GND = 0 V (GND pin as reference)	2			V
$I_{CC(SHDN)}$	Total quiescent current when in shutdown state	V_{CC} = ±6 V, ±12 V		0.3	0.7	mA
t_{DIS}	Disable time (see Note 3)	V_{CC} = ±12 V		0.5		µs
t_{EN}	Enable time (see Note 3)	V_{CC} = ±12 V		0.2		µs
$I_{IL(SHDN)}$	Shutdown pin input bias current for power up	V_{CC} = ±6 V, ±12 V		40	100	µA
$I_{IH(SHDN)}$	Shutdown pin input bias current for power down	V_{CC} = ±6 V, ±12 V $V_{(SHDN)}$ = 3.3 V		50	100	µA

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small and large signal output	vs Frequency	1 − 6
	Harmonic distortion	vs Output voltage	7, 8, 9 13, 14, 15
		vs Frequency	10, 11, 12, 16, 17, 18
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V	Negative output voltage headroom	vs Free-air temperature	22
V_O	Output voltage headroom	vs Output current	23
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I_{IB}	Input bias current	vs Free-air temperature	27
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	Overdrive recovery		33, 34
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TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

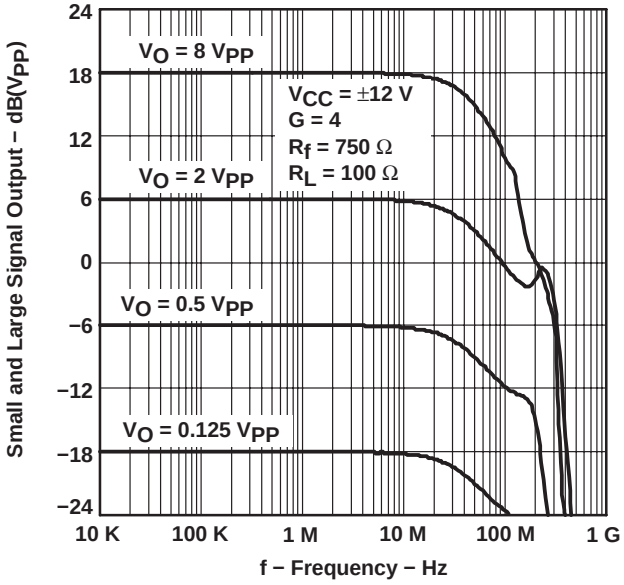


Figure 1

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

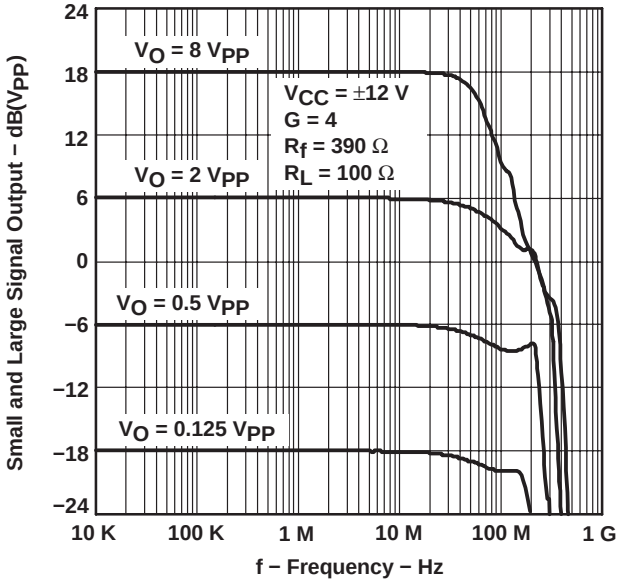


Figure 2

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

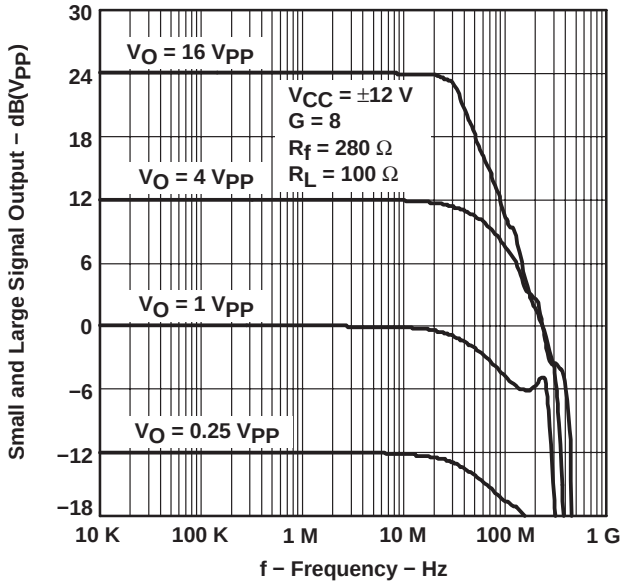


Figure 3

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

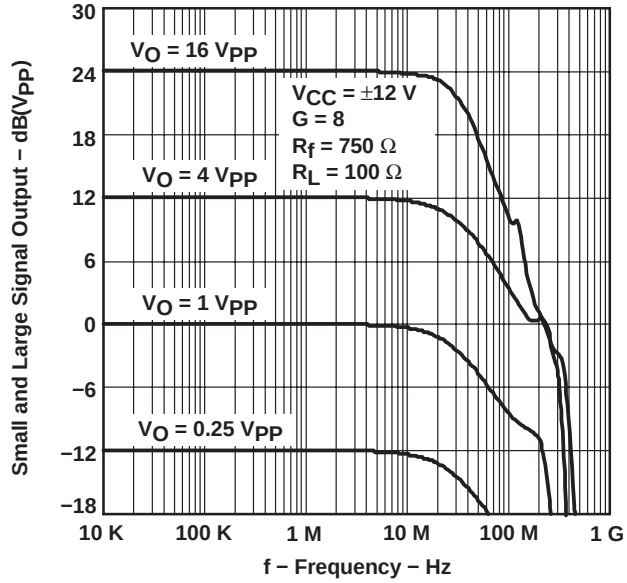


Figure 4

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL OUTPUT
vs
FREQUENCY

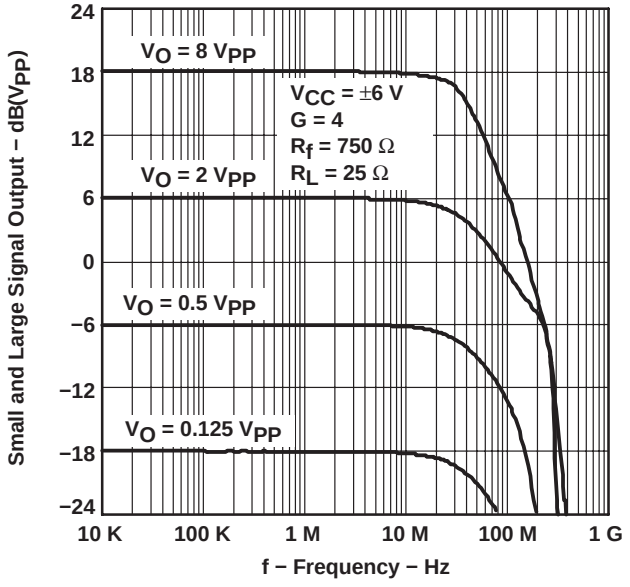


Figure 5

SMALL AND LARGE SIGNAL OUTPUT
vs
FREQUENCY

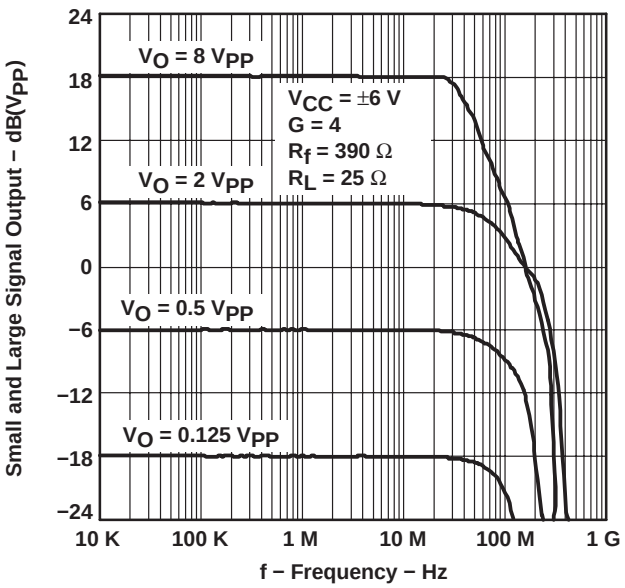


Figure 6

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

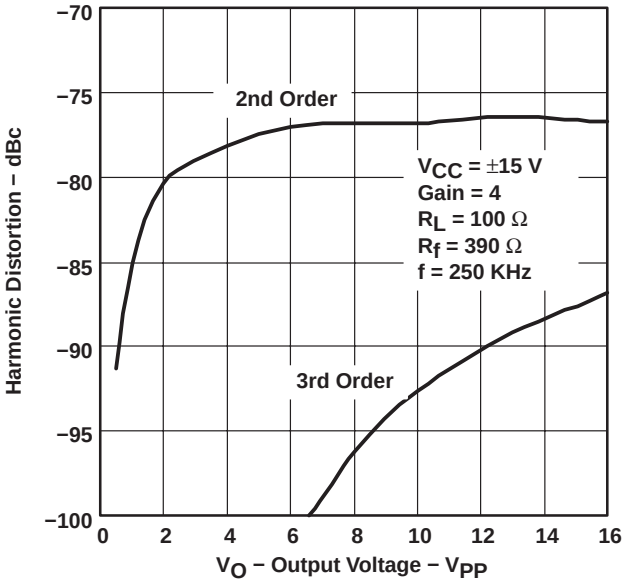


Figure 7

HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

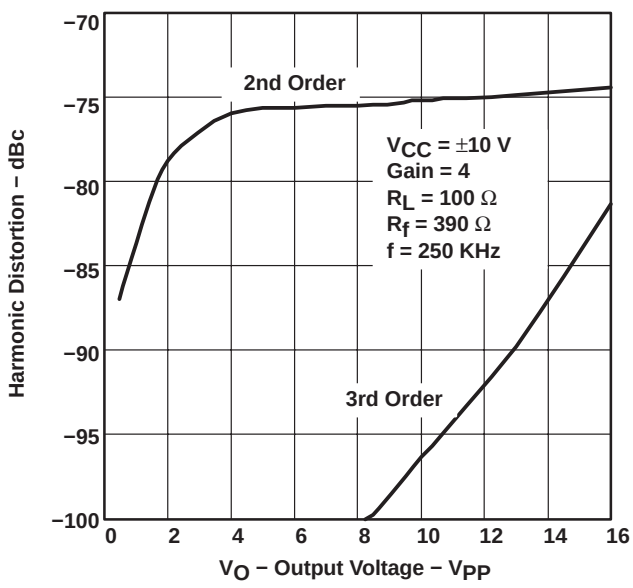


Figure 8

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION vs OUTPUT VOLTAGE

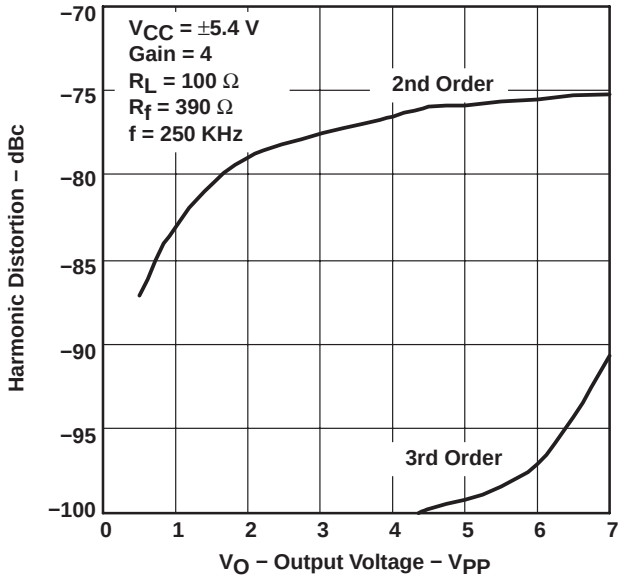


Figure 9

HARMONIC DISTORTION vs FREQUENCY

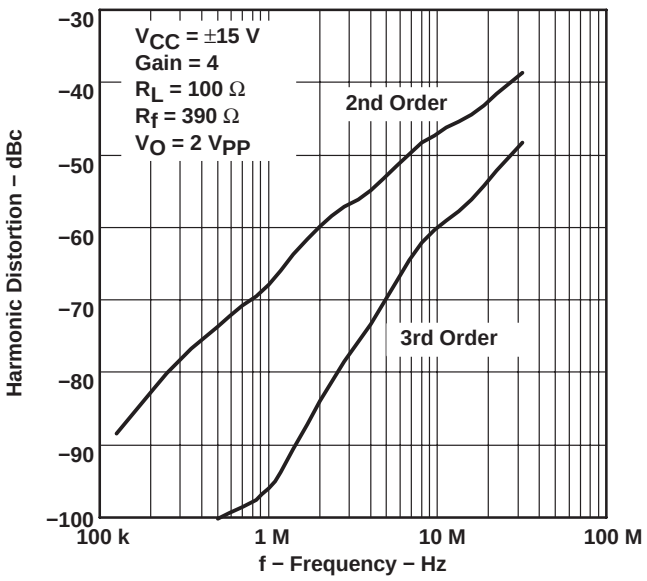


Figure 10

HARMONIC DISTORTION vs FREQUENCY

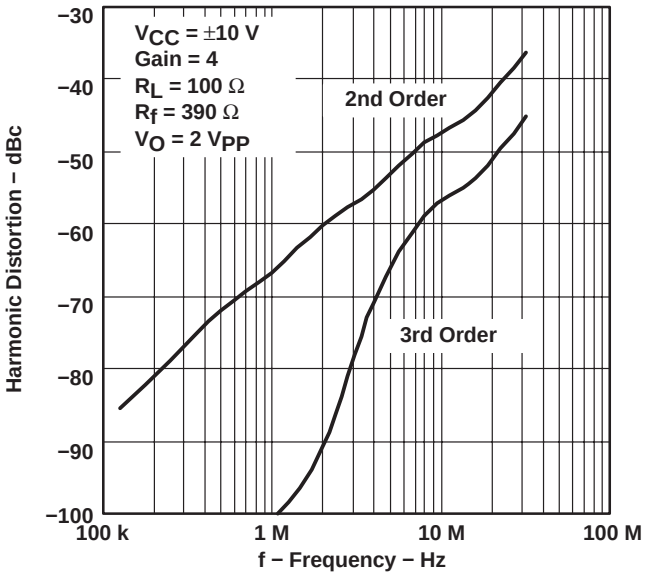


Figure 11

HARMONIC DISTORTION vs FREQUENCY

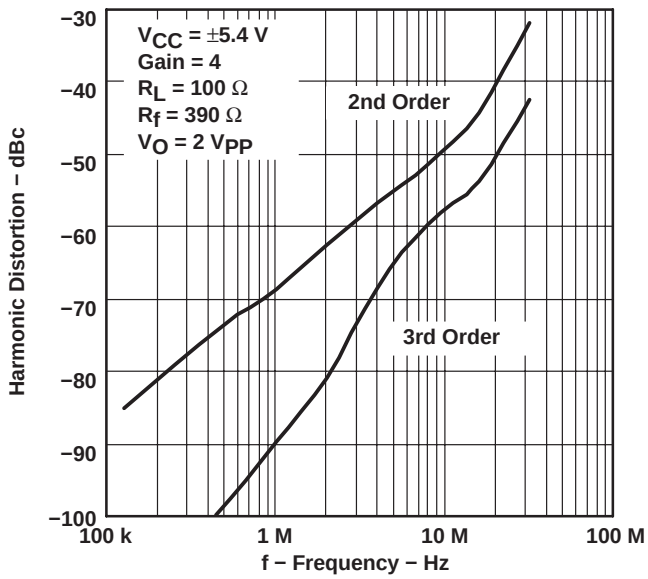


Figure 12

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION vs OUTPUT VOLTAGE

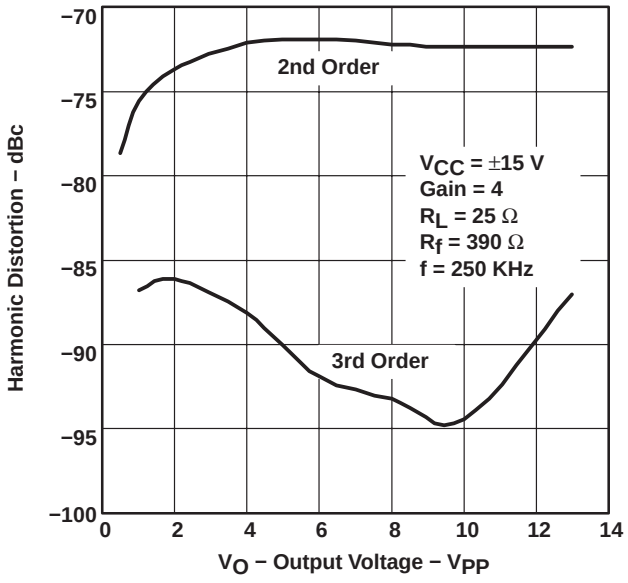


Figure 13

HARMONIC DISTORTION vs OUTPUT VOLTAGE

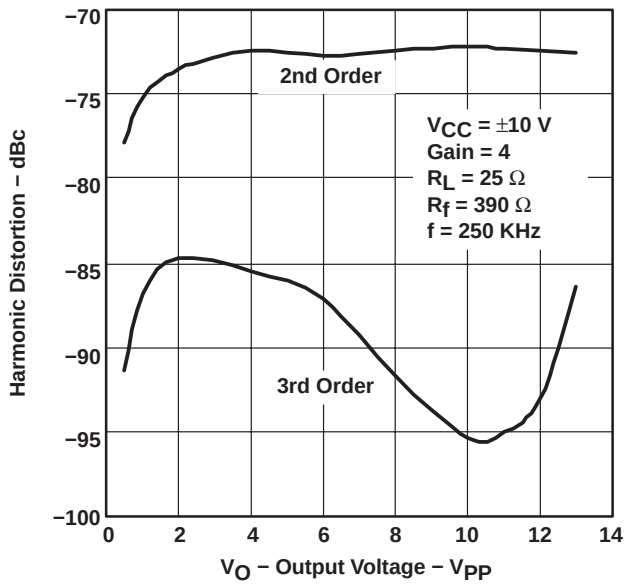


Figure 14

HARMONIC DISTORTION vs OUTPUT VOLTAGE

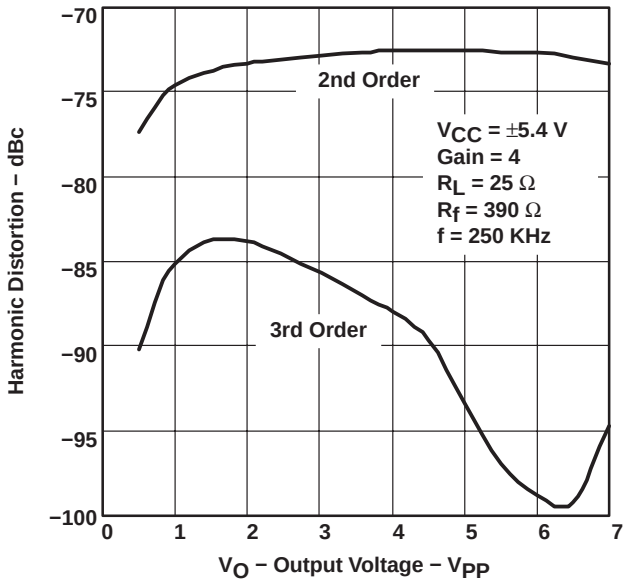


Figure 15

HARMONIC DISTORTION vs FREQUENCY

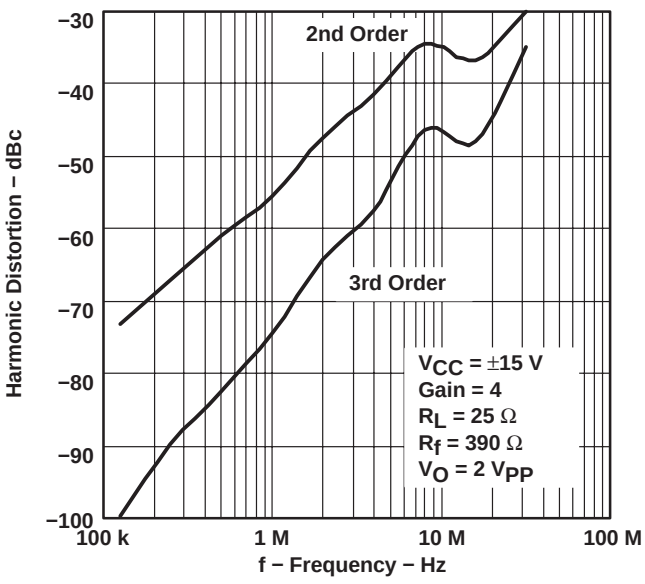


Figure 16

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION vs FREQUENCY

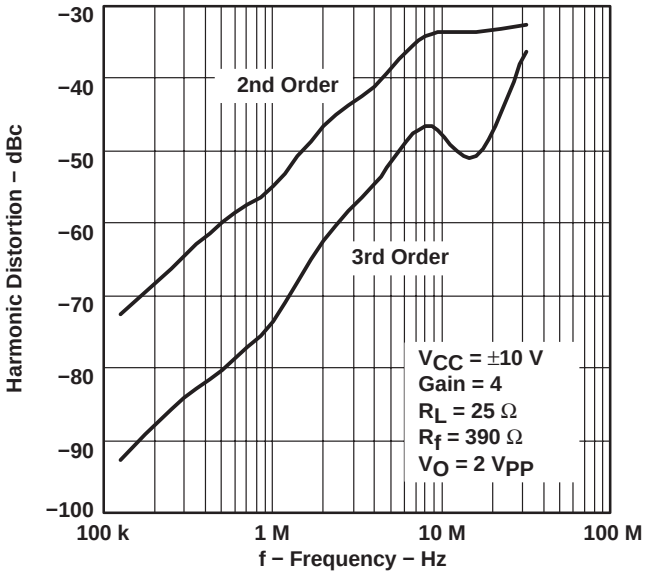


Figure 17

HARMONIC DISTORTION vs FREQUENCY

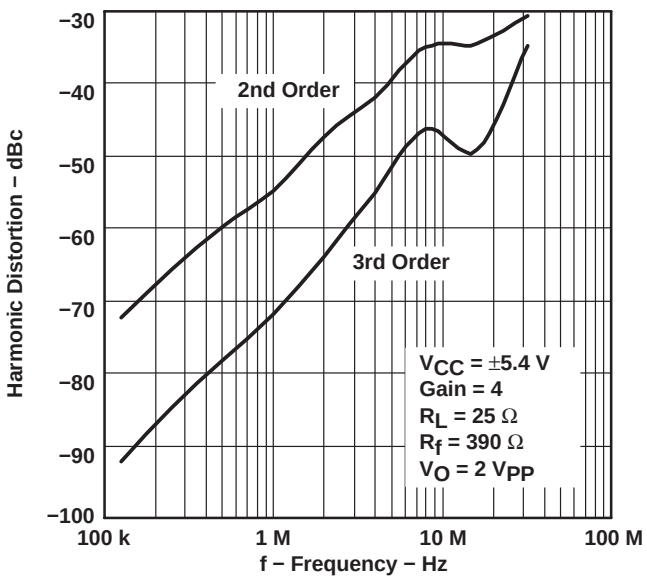


Figure 18

VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

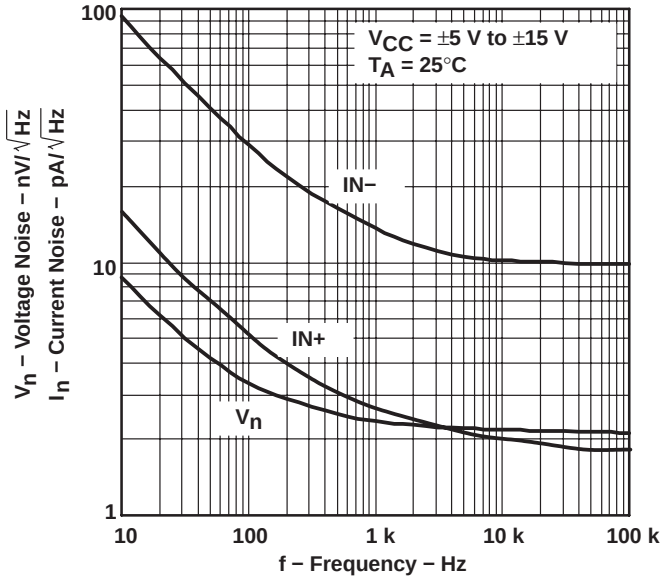


Figure 19

QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

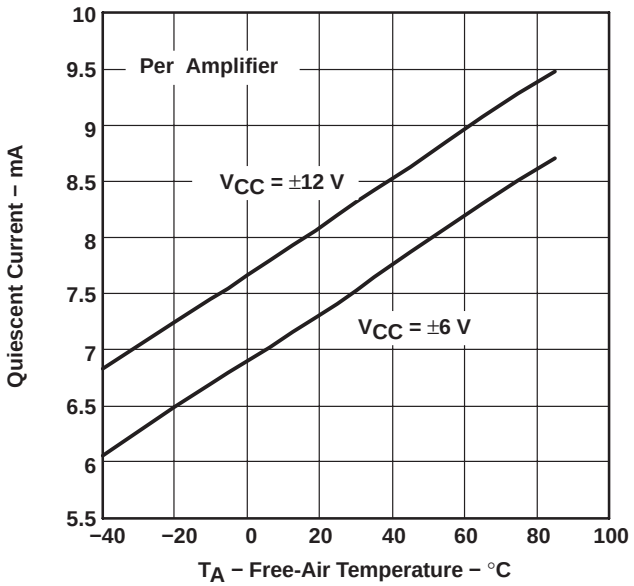


Figure 20

TYPICAL CHARACTERISTICS

POSITIVE OUTPUT VOLTAGE HEADROOM vs FREE-AIR TEMPERATURE

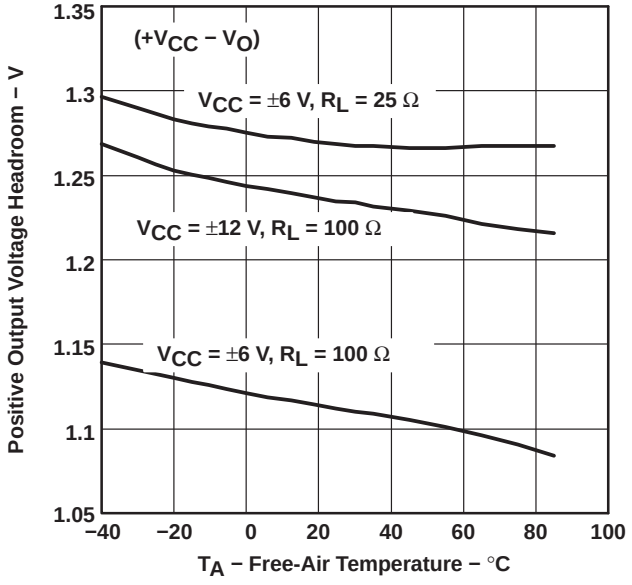


Figure 21

NEGATIVE OUTPUT VOLTAGE HEADROOM vs FREE-AIR TEMPERATURE

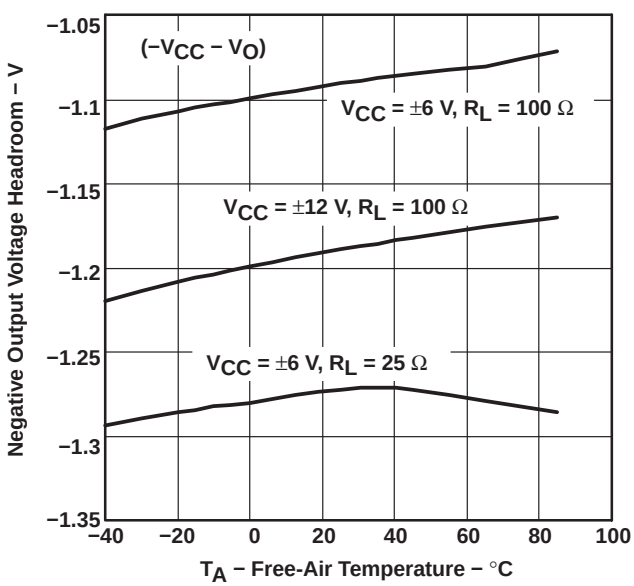


Figure 22

OUTPUT VOLTAGE HEADROOM vs OUTPUT CURRENT

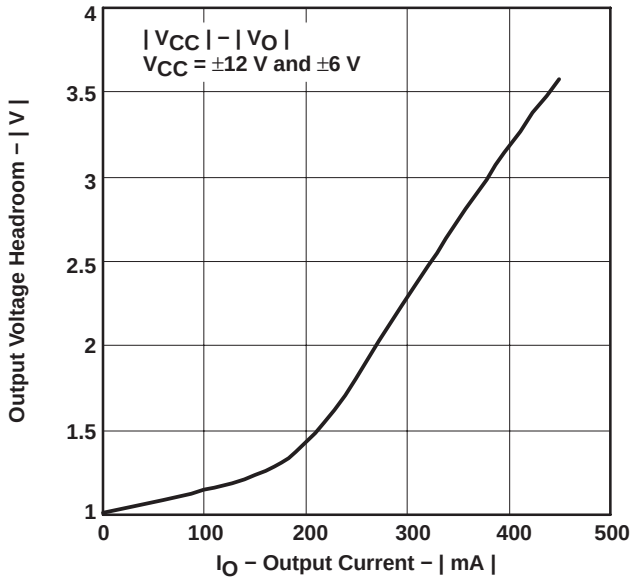


Figure 23

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

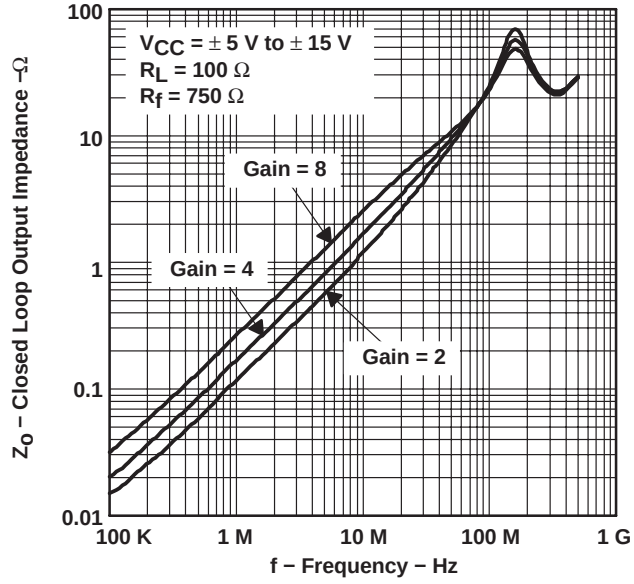


Figure 24

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT IN SHUTDOWN MODE vs FREE-AIR TEMPERATURE

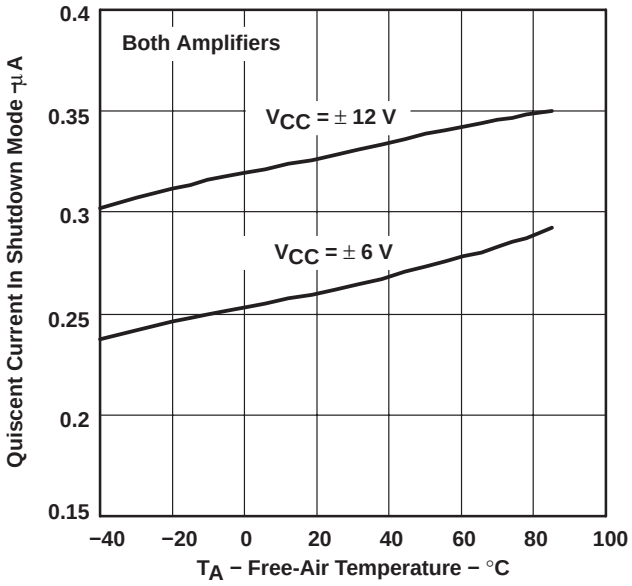


Figure 25

INPUT OFFSET VOLTAGE AND DIFFERENTIAL INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

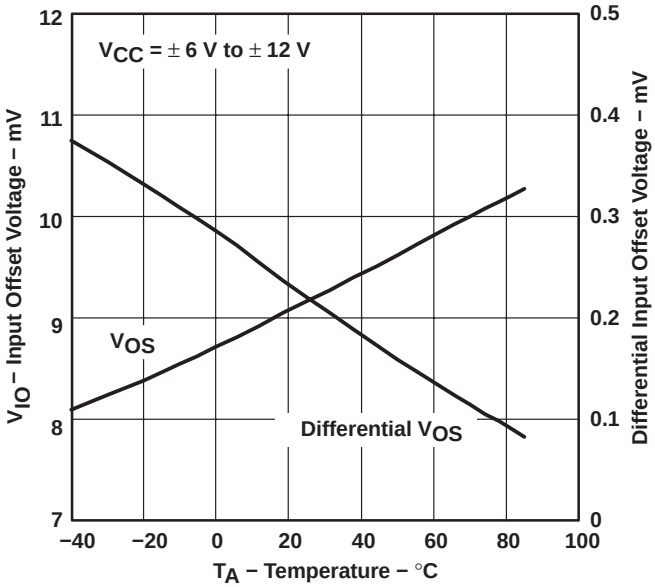


Figure 26

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

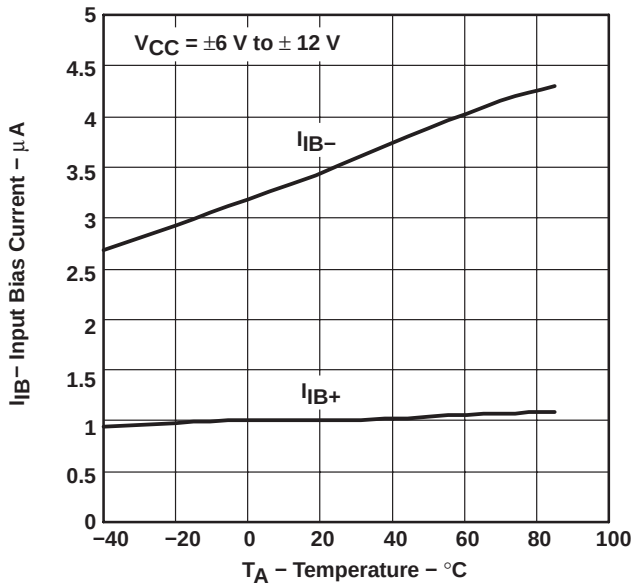


Figure 27

COMMON-MODE REJECTION RATIO vs FREQUENCY

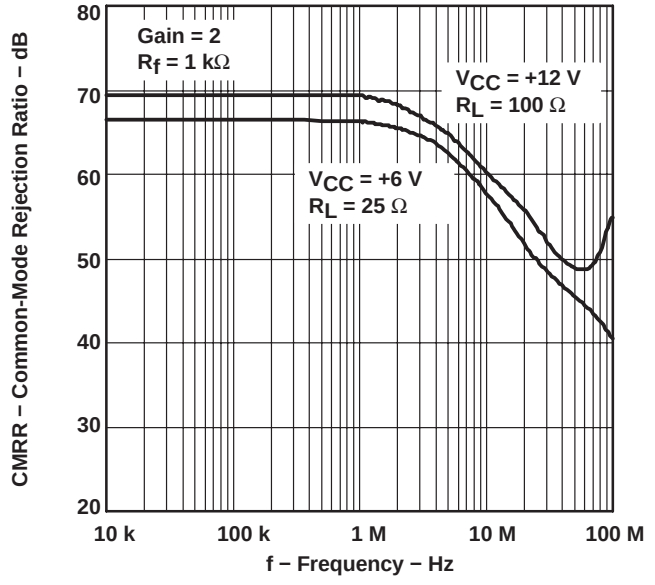


Figure 28

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

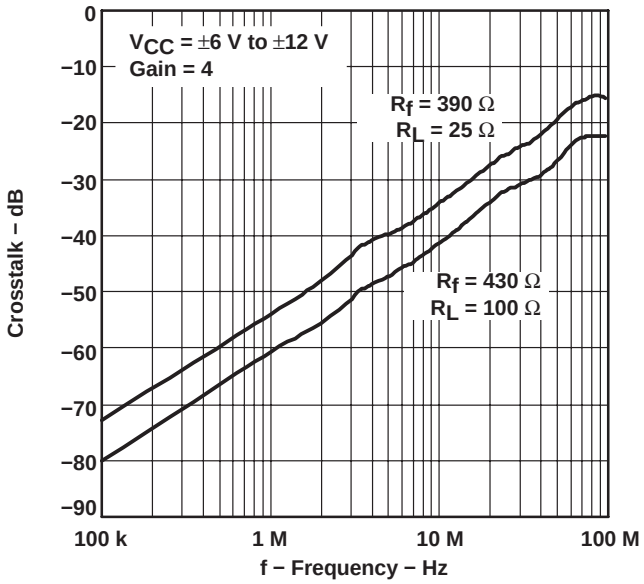


Figure 29

SLEW RATE vs OUTPUT VOLTAGE STEP

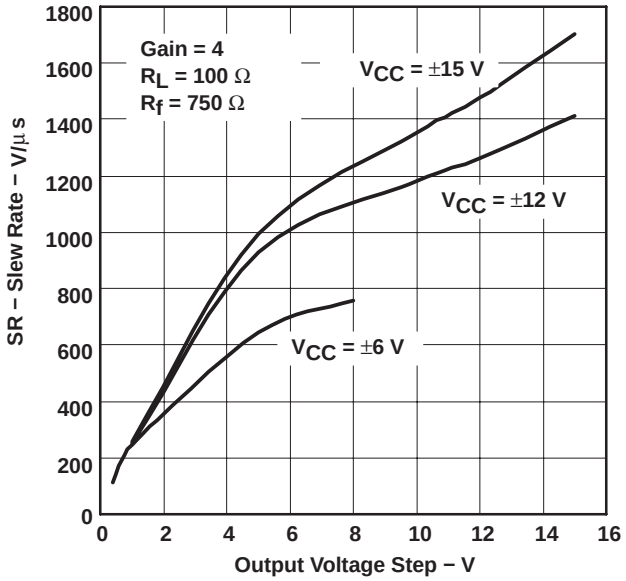


Figure 30

SHUTDOWN RESPONSE

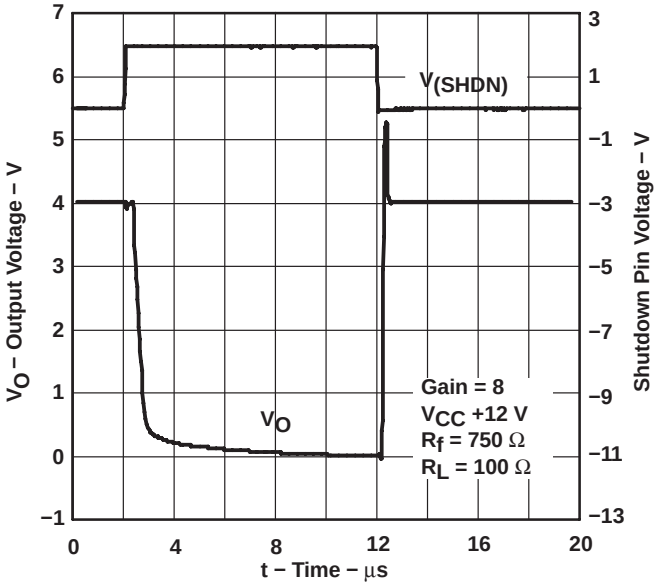


Figure 31

TRANSIMPEDANCE AND PHASE vs FREQUENCY

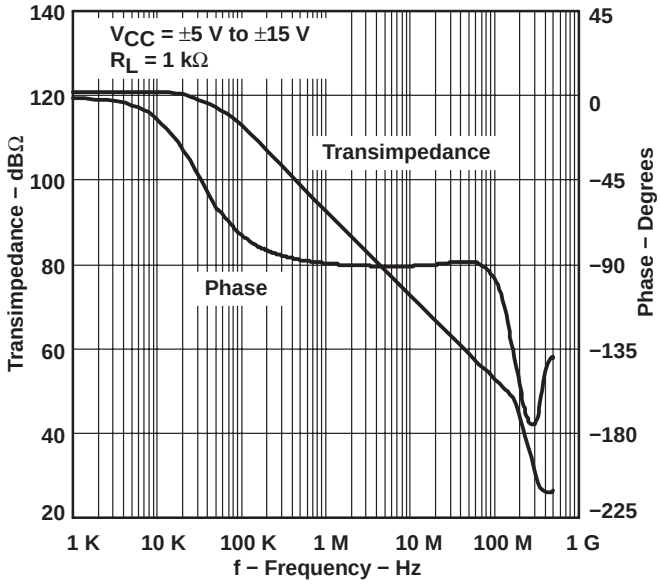


Figure 32

TYPICAL CHARACTERISTICS

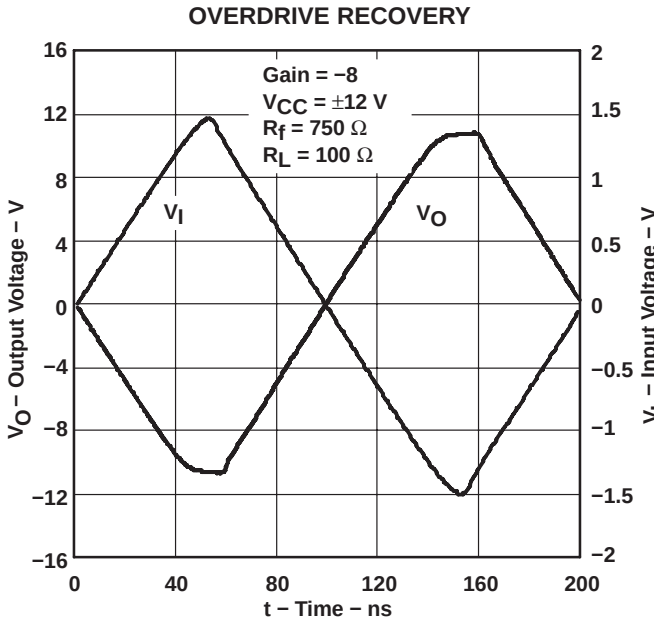


Figure 33

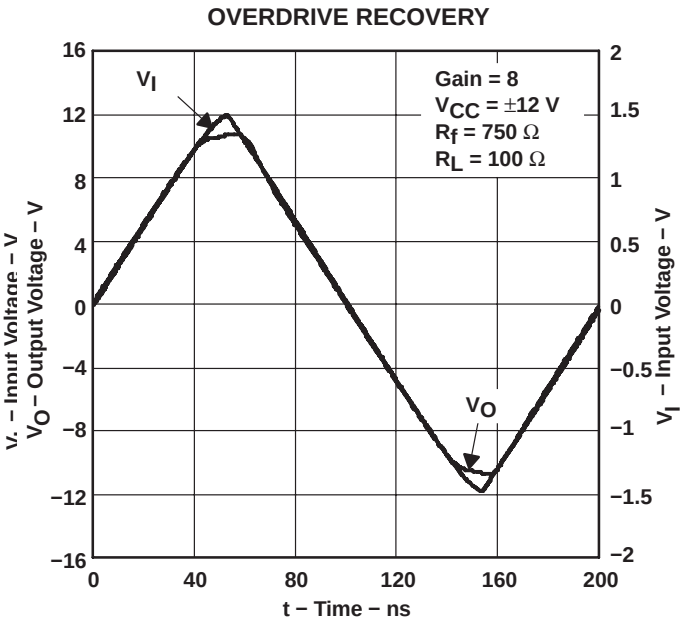


Figure 34

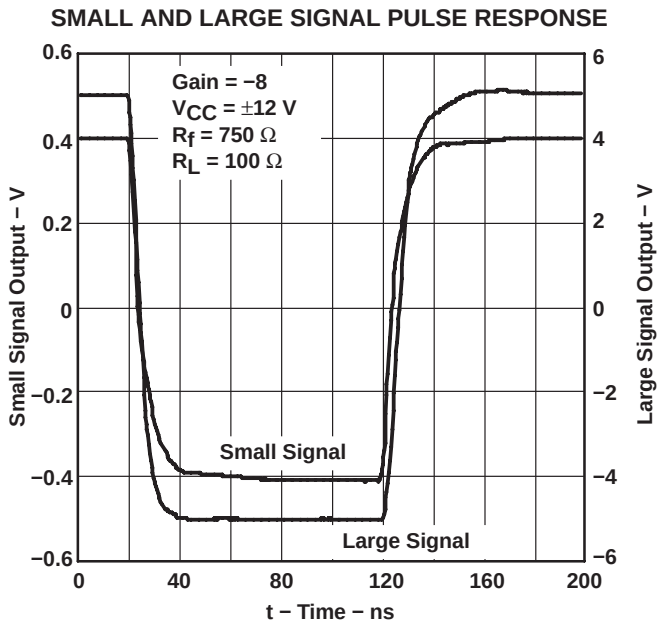


Figure 35

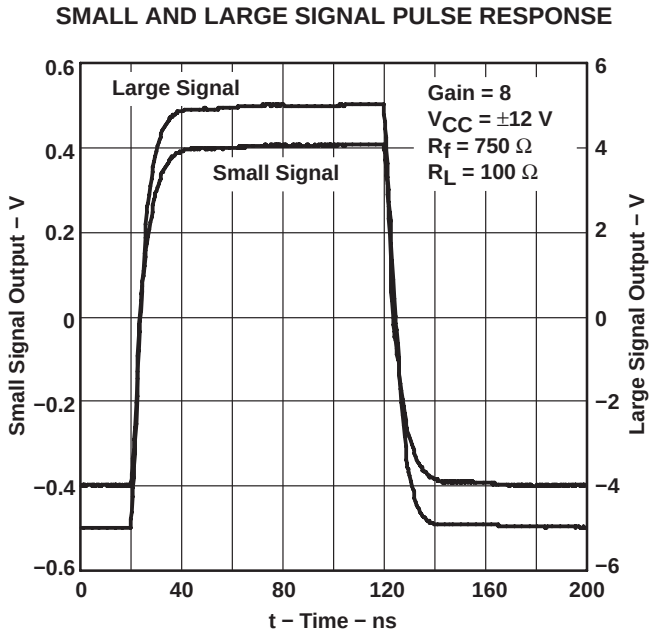


Figure 36

APPLICATION INFORMATION

The THS6042/3 contain two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 230 mA at full output voltage.

The THS6042/3 are fabricated using the Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

ADSL

The THS6042/3 were primarily designed as line drivers for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 13 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6042/3 are specified for a minimum full output current of 230 mA at ±6 V and 300 mA at the full output voltage of ±12 V. This performance meets the demanding needs of ADSL at the client side end of the telephone line. A typical ADSL schematic is shown in Figure 37.

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or creates intermodulation products that interfere with other ADSL carrier frequencies.

The THS6042/3 have been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figures 7 − 15. In the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) is primarily due to the third order harmonics. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system. Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

Even though the THS6042/3 are designed to drive ADSL signals that have a maximum bandwidth of 1.1 MHz, reactive loading from the transformer can cause some serious issues. Most transformers have a resonance peak typically occurring from 20 MHz up to 150 MHz depending on the manufacturer and construction technique. This resonance peak can cause some serious issues with the line driver amplifier such as small high-frequency oscillations, increased current consumption, and/or ringing. Although the series termination resistor helps isolate the transformer's resonance from the line-driver amplifier, additional means may be necessary to eliminate the effects of a reactive load. The simplest way is to add a snubber network, also known as a zoebel network, in parallel with the transformer as shown by $R_{(SNUB)}$ and $C_{(SNUB)}$ in Figure 36. At high frequencies, where the transformer's impedance becomes very high at its resonance frequency (ex: 1 kΩ @ 100 MHz), the snubber provides a resistive load to the circuit. The value for $R_{(SNUB)}$ should initially be set to the impedance presented by the transformer within its pass-band. An example of this would be to use a 100-Ω resistor for a 1:1 transformer or a 25-Ω resistor for a 1:2 transformer. The value for $C_{(SNUB)}$ should be chosen such that the –3 dB frequency is about 5 times less than the resonance frequency. For example,if the resonance frequency is at 100 MHz, the impedance of $C_{(SNUB)}$ should be equal to $R_{(SNUB)}$ at 20 MHz. This leads to a value of $C_{(SNUB)} = 1 / (2 \pi f R_{(SNUB)})$, or approximately 82 pF. This should only be used as a starting point. The final values will be dictated by actual circuit testing.

APPLICATION INFORMATION

ADSL (continued)

One problem in the ADSL CPE area is noise. It is imperative that signals received off the telephone line have as high a signal-to-noise ratio (SNR) as possible. This is because of the numerous sources of interference on the line. The best way to accomplish this high SNR is to have a low-noise receiver such as the THS6062 or OPA2822 on the front-end. Even if the receiver has very low noise characteristics, noise could be dominated by the line driver amplifier. The THS6042/3 were primarily designed to circumvent this issue.

The ADSL standard, ANSI T1.413, stipulates a noise power spectral density of –140 dBm/Hz, which is equivalent to 31.6 nV/$\sqrt{\text{Hz}}$ for a 100-Ω system. Although many amplifiers can reach this level of performance, actual ADSL system testing has indicated that the noise power spectral density may be required to have ≤ –150 dBm/Hz, or ≤ 10 nV/$\sqrt{\text{Hz}}$. With a transformer ratio of 1:2, this number reduces to less than 5 nV/$\sqrt{\text{Hz}}$. The THS6042/3, with an equivalent input noise of 2.2 nV/$\sqrt{\text{Hz}}$, is an excellent choice for this application. Coupled with a low 2.1 pA/$\sqrt{\text{Hz}}$ noninverting current noise, a very low 11 pA/$\sqrt{\text{Hz}}$ inverting current noise, and low value resistors, the THS6042/3 ensures that the received signal SNR is as high as possible.

APPLICATION INFORMATION

ADSL (continued)

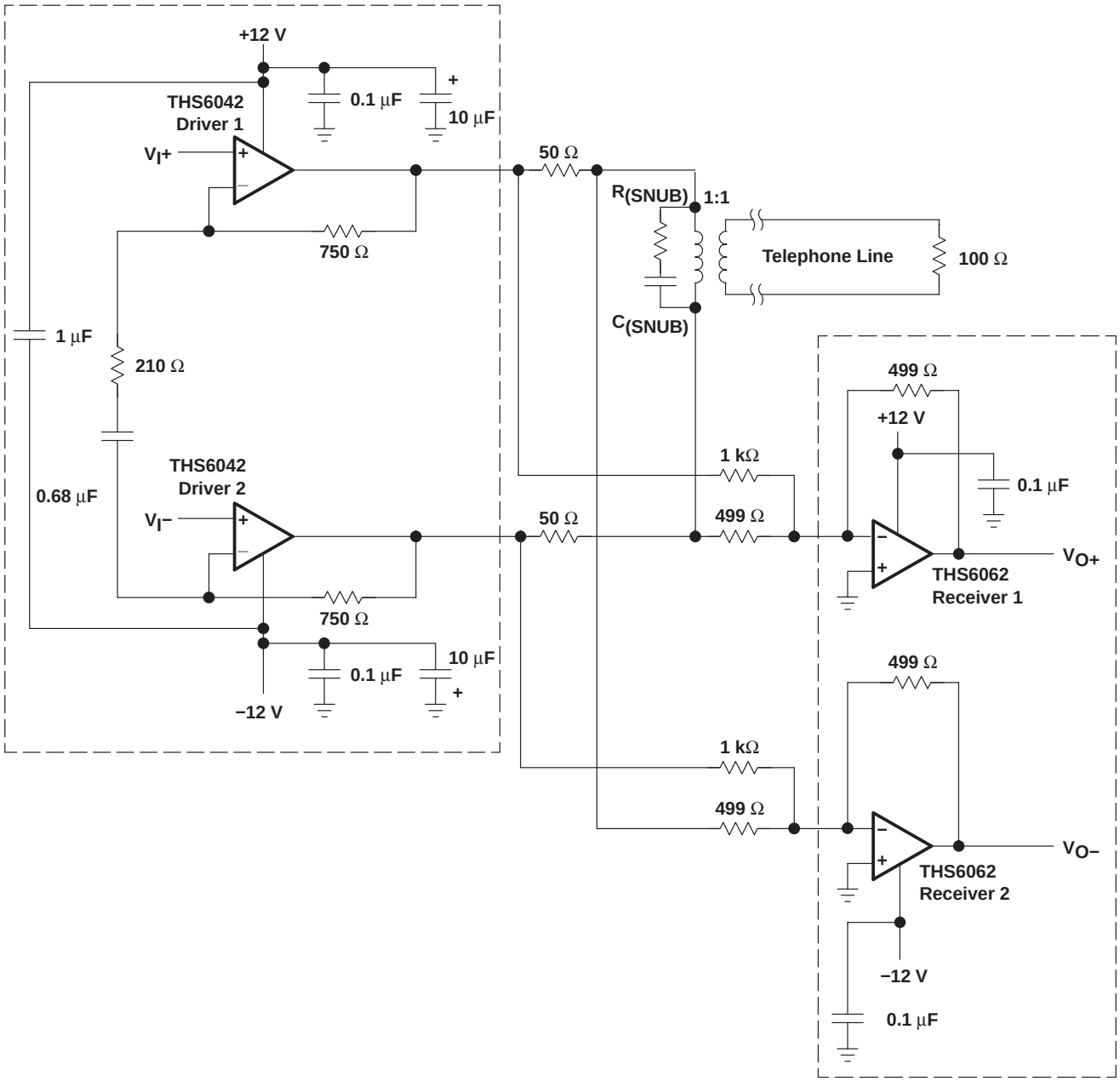


Figure 37. THS6042 ADSL Application With 1:1 Transformer Ratio

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 38. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN− = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

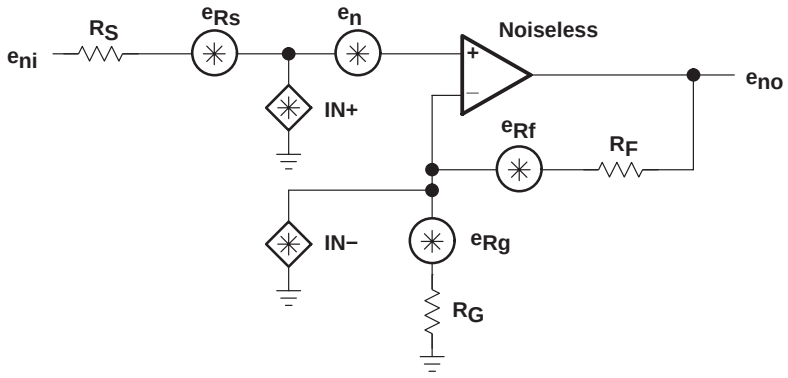


Figure 38. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\, A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{\ 2}}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 39 shows the noise figure graph for the THS6042/3.

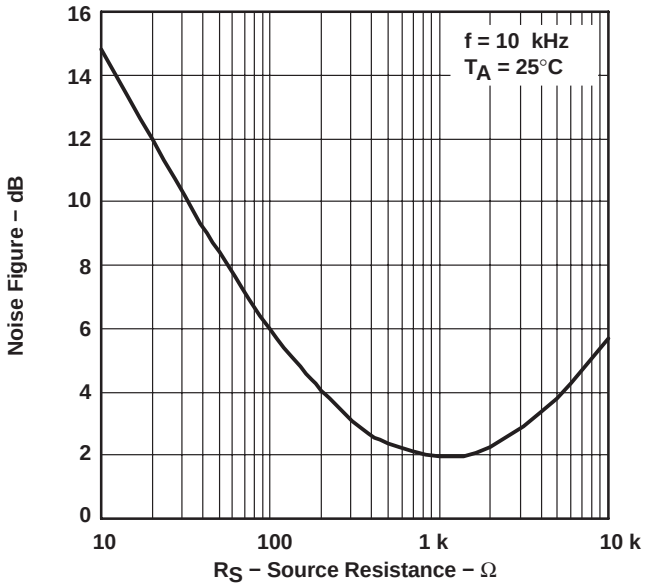


Figure 39. Noise Figure vs Source Resistance

APPLICATION INFORMATION

device protection features

The THS6042/3 have two built-in features that protect the devices against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device.

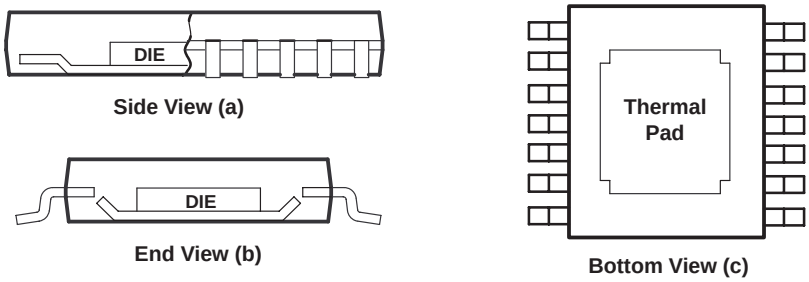
The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

thermal information − PowerPAD

The THS6042/3 are available packaged in thermally-enhanced PowerPAD packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 40(a) and Figure 40(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 40(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 40. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6042/3. These areas are high-speed layout techniques and thermal-management techniques. Because the devices are high-speed parts, the following guidelines are recommended.

- Ground plane − It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6042/3 is not necessarily required, it is highly recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance − To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 41, which shows what happens when a 2.2-pF capacitor is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. While the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a virtual ground and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 42, where a 22-pF capacitor adds only 0.9 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initally appear to be a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So, proper analysis of adding a capacitor to the inverting input node should always be performed for stable operation.

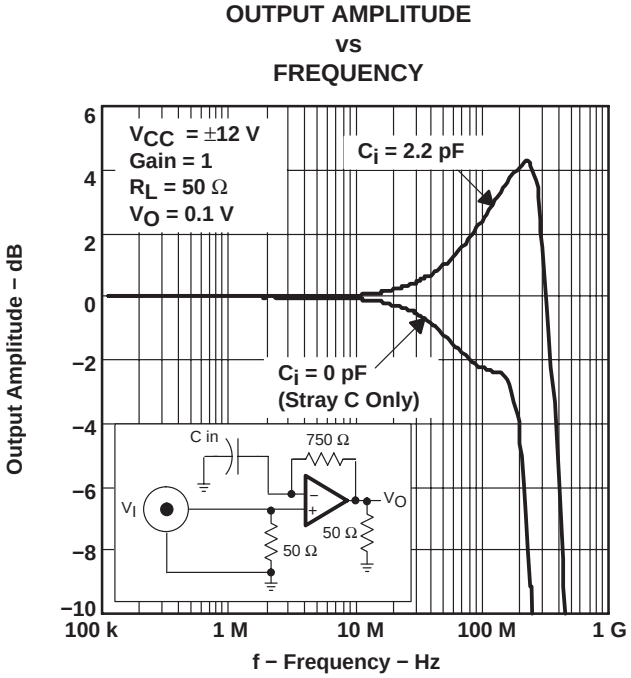


Figure 41

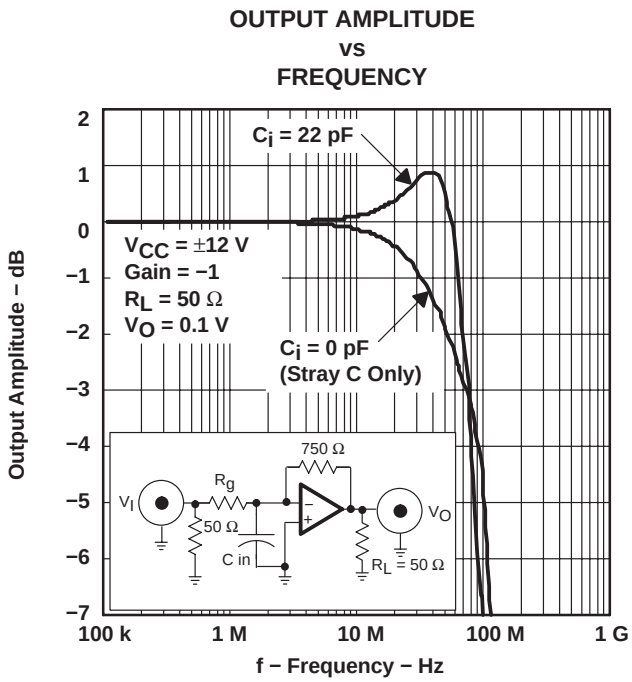


Figure 42

APPLICATION INFORMATION

PCB design considerations (continued)

- Proper power supply decoupling − Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- Differential power supply decoupling − The THS6042/3 were designed for driving low-impedance differential signals. The 50-Ω load which each amplifier drives causes large amounts of currents to flow from amplifier to amplifier. Power supply decoupling for differential current signals must be accounted for to ensure low distortion of the THS6042/3. By simply connecting a 0.1-μF to 1-μF ceramic capacitor from the $+V_{CC}$ pin to the $-V_{CC}$ pin, differential current loops will be minimized (see Figure 37). This will help keep the THS6042/3 operating at peak performance.

Because of its power dissipation, proper thermal management of the THS6042/3 is required. Even though the THS6042 and THS6043 PowerPADs are different, the general methodology is the same. Although there are many ways to properly heatsink these devices, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane. Refer to Figure 43 for the following steps.

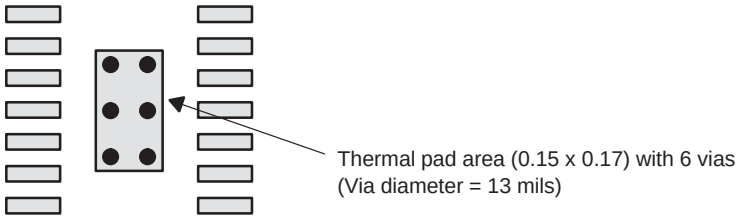


Figure 43. THS6043 PowerPAD PCB Etch and Via Pattern − Minimum Requirements

1. Place 6 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
2. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This will help dissipate the heat generated from the THS6042/3. These additional vias may be larger than the 13 mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, therefore, wicking is generally not a problem.
3. Connect all holes to the internal ground plane.
4. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6042/3 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
5. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its 6 holes. The bottom-side solder mask should cover the 6 holes of the thermal pad area. This eliminates the solder from being pulled away from the thermal pad area during the reflow process.

APPLICATION INFORMATION

PCB design considerations (continued)

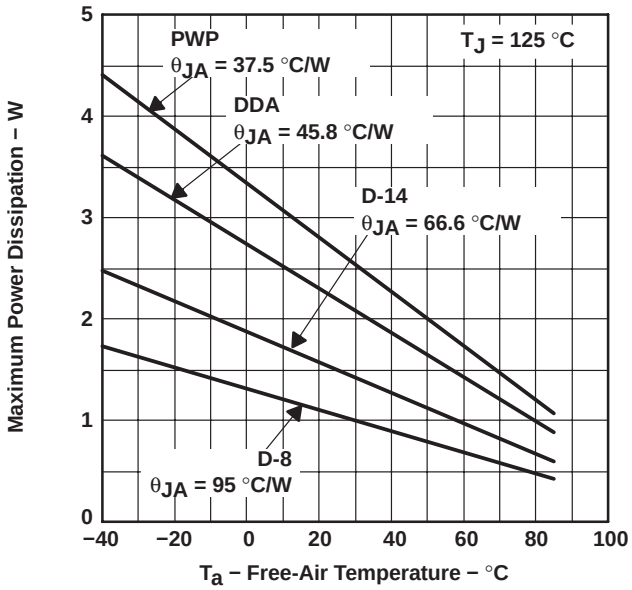
6. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
7. With these preparatory steps in place, the THS6042/3 is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6042/3 in their PowerPAD packages depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 95°C/W for the SOIC−8 (D) package, 45.8°C/W for the DDA package, 66.6°C/W for the SOIC−14 (D) package, and 37.5°C/W for the PWP package. Although the maximum recommended junction temperature (T_J) is listed as 150°C, performance at this elevated temperature will suffer. To ensure optimal performance, the junction temperature should be kept below 125°C. Above this temperature, distortion will tend to increase. Figure 44 shows the recommended power dissipation with a junction temperature of 125°C. If no solder is used to connect the PowerPAD to the PCB, the θ_{JA} will increase dramatically with a vast reduction in power dissipation capability. For a given θ_{JA} and a maximum junction temperature, the power dissipation is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Power dissipation of THS6042/3 (watts)
T_{MAX} = Maximum junction temperature allowed in the design (125°C recommended)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (D−8 =38.3°C/W, DDA = 9.2°C/W, D−14 = 26.9°C/W, PWP = 1.4°C/W)
θ_{CA} = Thermal coefficient from case to ambient



NOTE: Results are with no air flow and PCB size = 3”× 3”
2 oz. trace and copper pad with solder unless otherwise noted.

Figure 44. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

PCB design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class-AB), most of the heat dissipation is at low output voltages with high output currents. Figure 45 and Figure 46 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using V_{CC} = ±6 V, there is generally not a heat problem, even with SOIC packages.

However, when using V_{CC} = ±12 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The standard SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package.

MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE (DUE TO THERMAL LIMITS)

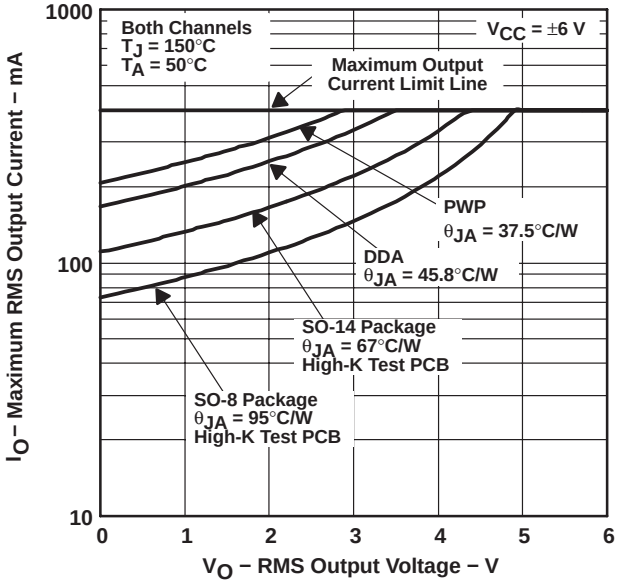


Figure 45

MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE (DUE TO THERMAL LIMITS)

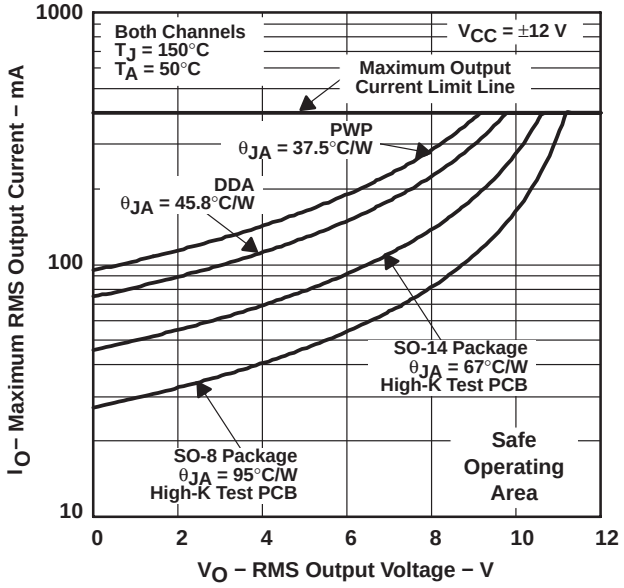


Figure 46

APPLICATION INFORMATION

recommended feedback and gain resistor values

As with all current feedback amplifiers, the bandwidth of the THS6042/3 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 1 to 6. The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with these drivers, which tend to drive low-impedance loads. This can be seen in Figures 1−6. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor may need to be changed. For most applications, a feedback resistor value of 750 Ω is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Table 1. Recommended Feedback (R_f) Values for Optimum Frequency Response

GAIN	R_L = 25 Ω		R_L = 100 Ω	
	V_{CC} = ±6 V	V_{CC} = ±12 V	V_{CC} = ±6 V	V_{CC} = ±12 V
1	680 Ω	560 Ω	620 Ω	510 Ω
2, −1	470 Ω	430 Ω	430 Ω	390 Ω
4	270 Ω	240 Ω	270 Ω	240 Ω
8	200 Ω	200 Ω	200 Ω	200 Ω

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and may increase the distortion. Decreasing the feedback resistance too low may increase the bandwidth, but an increase in the load on the output may cause distortion to increase instead of decreasing. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion. This is illustrated in Figure 10 to 12 and Figures 16 to 18.

APPLICATION INFORMATION

shutdown control

The THS6043 is essentially the same amplifier as the THS6042. The only difference is the added flexibility of a shutdown circuit. When the shutdown pin signal is low, the THS6043 is active. But, when a shutdown pin is high (≥2 V), the THS6043 is turned off. The shutdown logic is not latched and should always have a signal applied to it. To help ensure a fixed logic state, an internal 50 kΩ resistor to GND is utilized. An external resistor, such as a 3.3 kΩ, to GND may be added to help improve noise immunity within harsh environments. If no external resistor is utilized and SHDN pin is left unconnected, the THS6043 defaults to a power-on state. A simplified circuit can be seen in Figure 47.

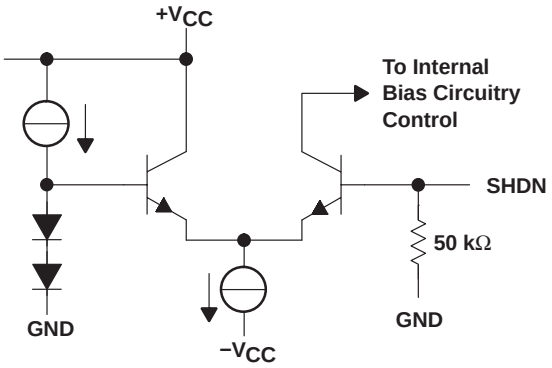


Figure 47. Simplified THS6043 Shutdown Control Circuit

One aspect of the shutdown feature, which is often over-looked, is that the amplifier does not have a large output impedance while in shutdown mode. This is due to the R_F and R_G resistors. This effect is true for any amplifier connected as an amplifier with gains >1. The internal circuitry may be powered down and in a high-impedance state, but the resistors are always there. This allows the signal to flow through these resistors and into the ground connection. Figure 48 shows the results of the output impedance with no feedback resistor and a typically configured amplifier.

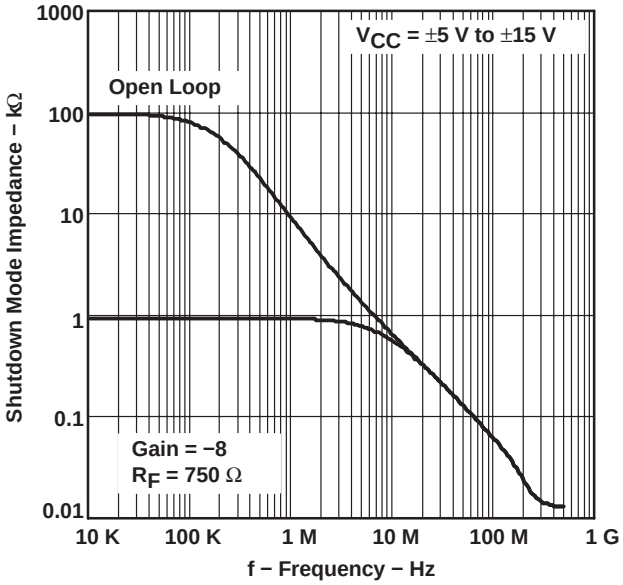


Figure 48. Output Impedance In Shutdown Mode

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6042/3 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 5 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 49. Keep in mind that stray capacitance on the output is also considered capacitive loading, whether or not it is there on purpose. A minimum value of 5 Ω should work well for most applications. In ADSL systems, setting the series resistor value to 12.4 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

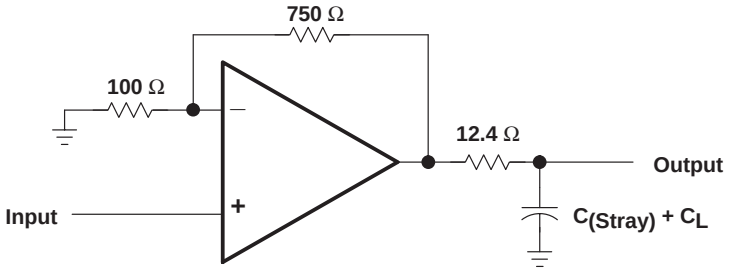
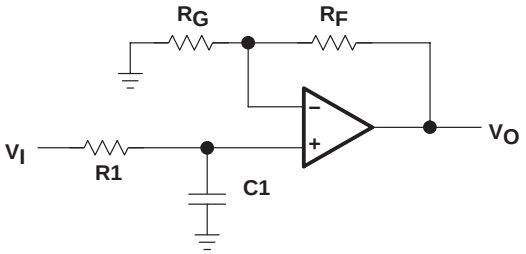


Figure 49. Driving a Capacitive Load

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is *not* recommended. The THS6042/3, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 50).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 50. Single-Pole Low-Pass Filter

APPLICATION INFORMATION

general configurations (continued)

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 51.

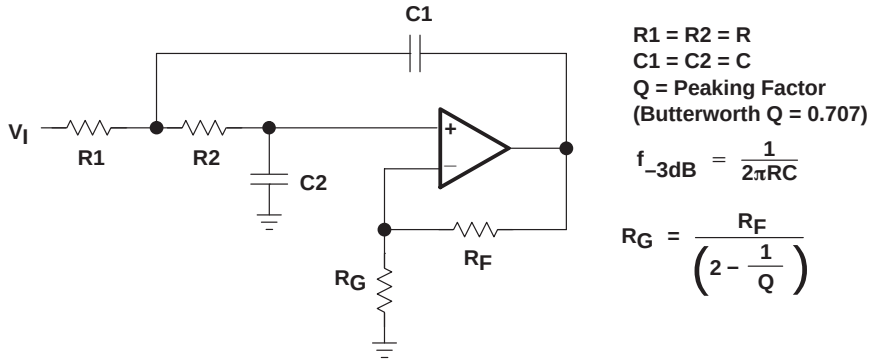


Figure 51. 2-Pole Low-Pass Sallen-Key Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6042CDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	6042C	Samples
THS6042ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6042I	Samples
THS6042IDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	6042I	Samples
THS6042IDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6042I	Samples
THS6043CPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6043C	Samples
THS6043ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS6043I	Samples
THS6043IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6043I	Samples
THS6043IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6043I	Samples
THS6043IPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6043I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

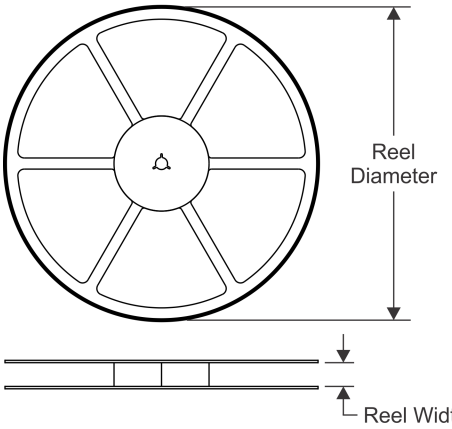
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

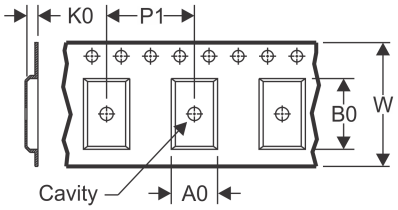
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

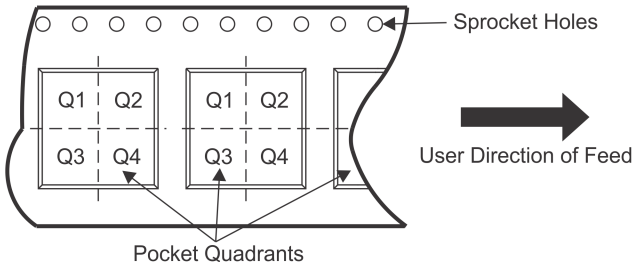


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

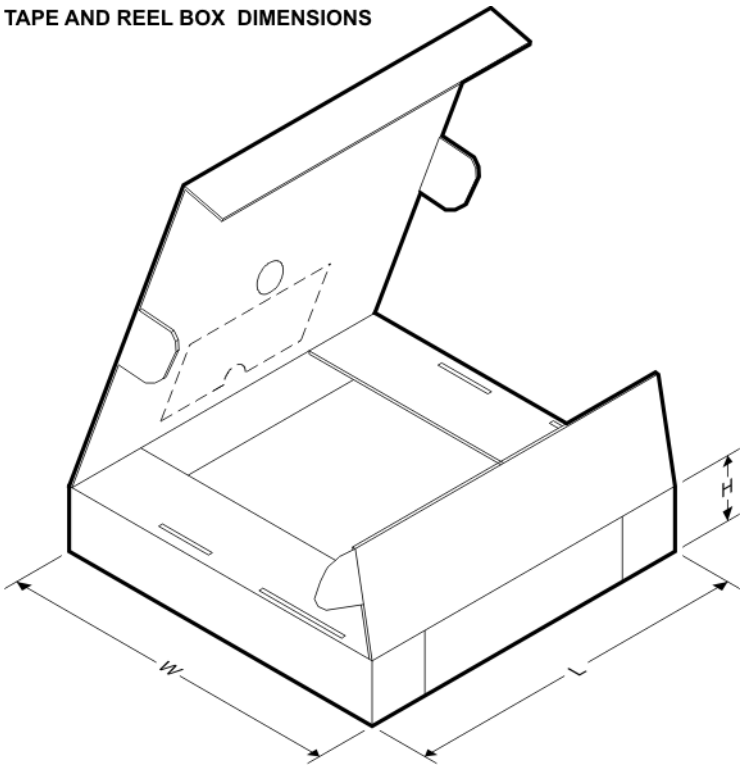
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6043IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

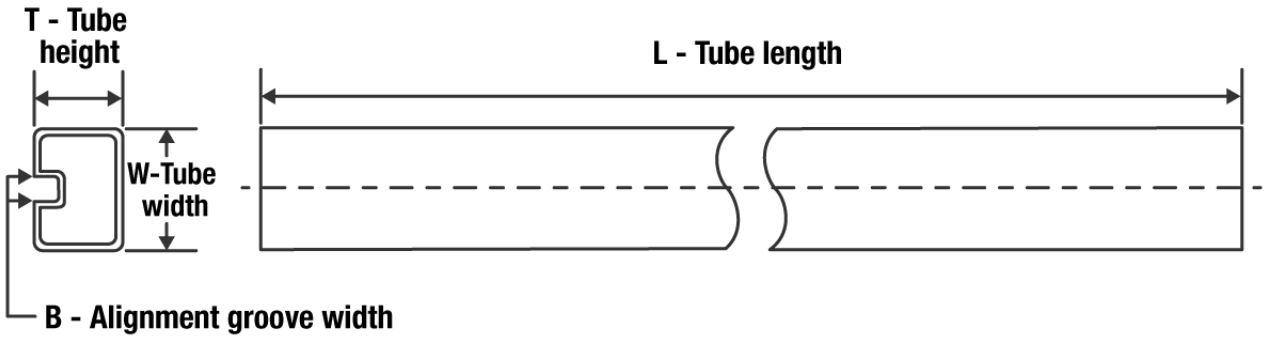
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6043IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE

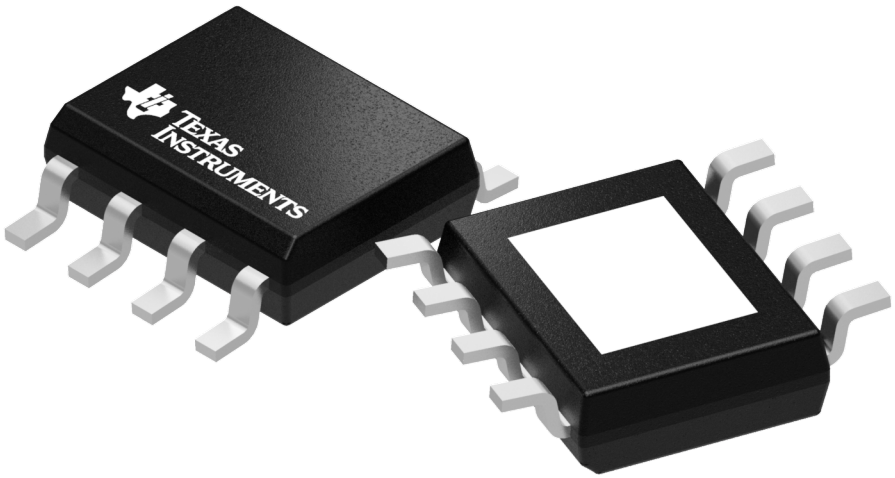


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS6042CDDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS6042ID	D	SOIC	8	75	505.46	6.76	3810	4
THS6042IDDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS6042IDG4	D	SOIC	8	75	505.46	6.76	3810	4
THS6043CPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
THS6043ID	D	SOIC	14	50	505.46	6.76	3810	4
THS6043IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



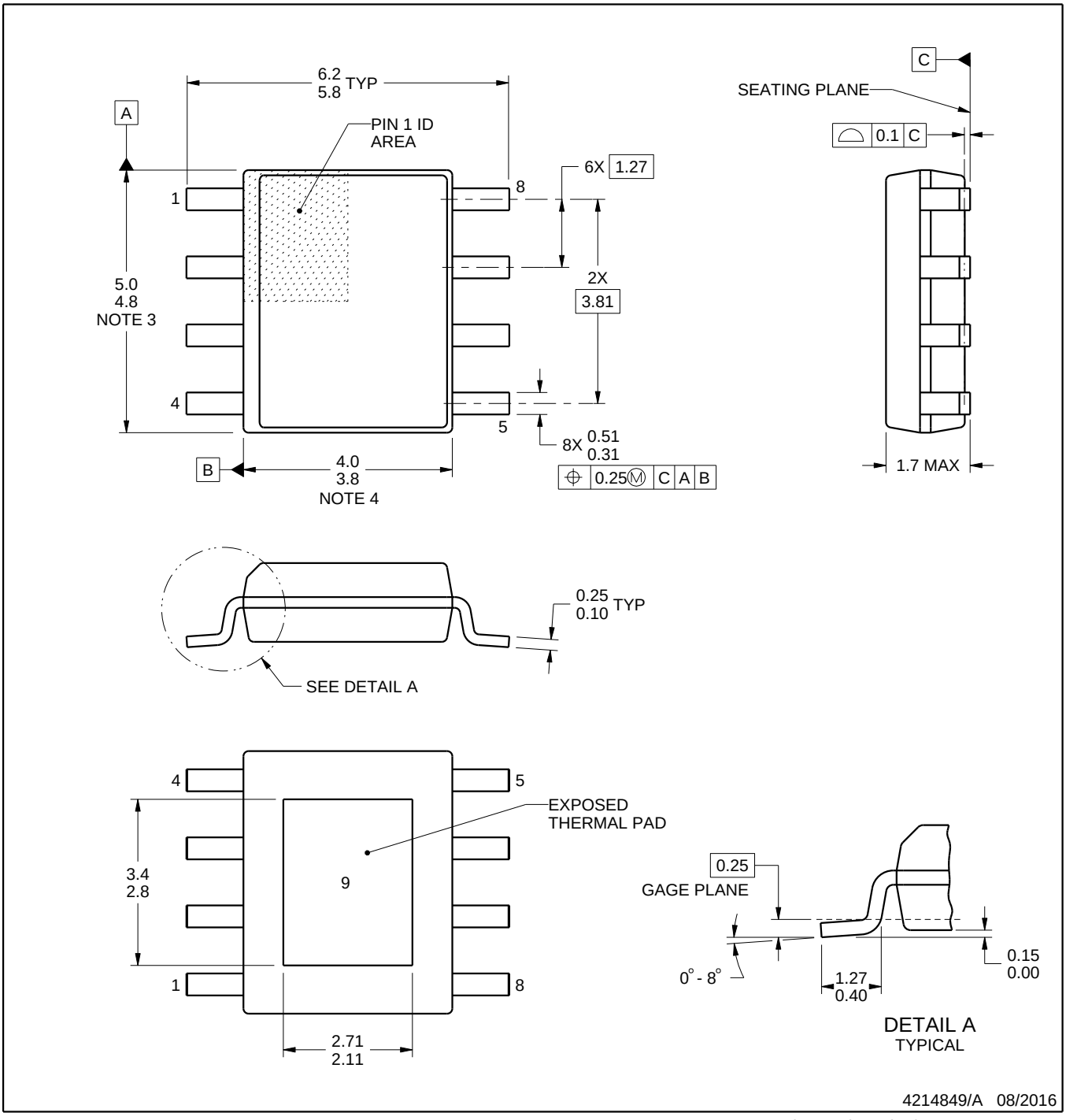
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

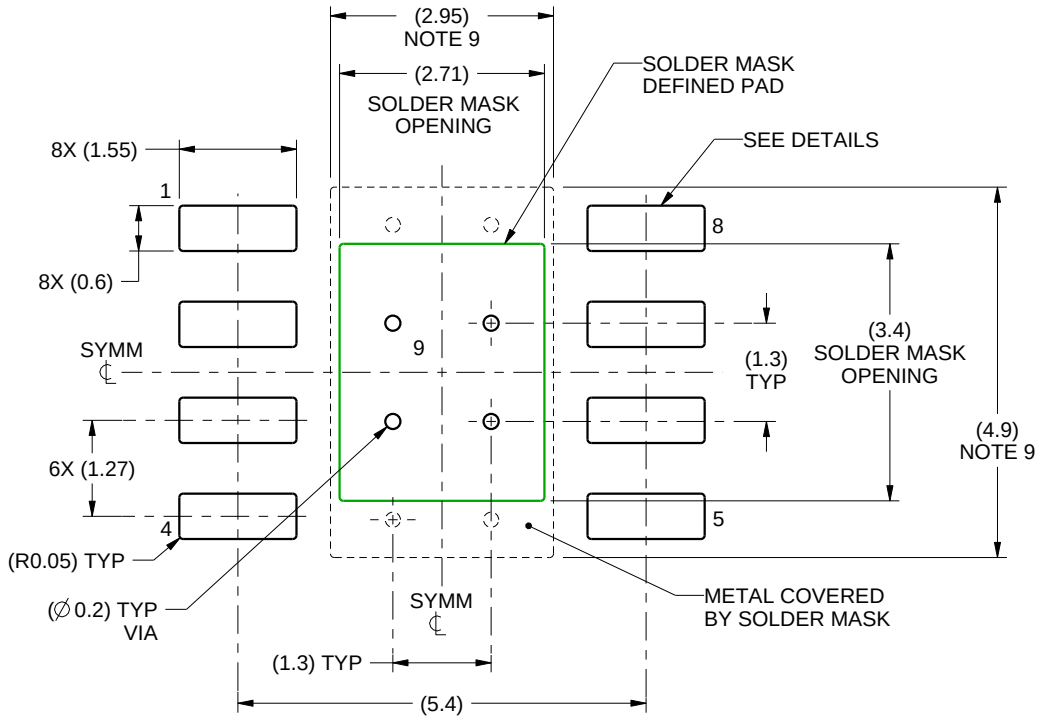
PLASTIC SMALL OUTLINE



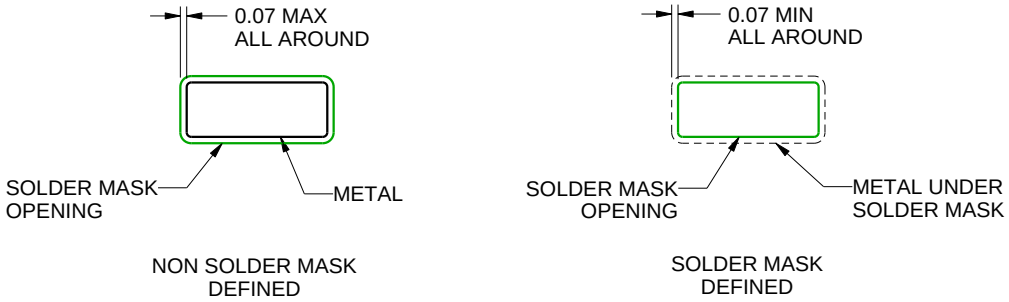
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

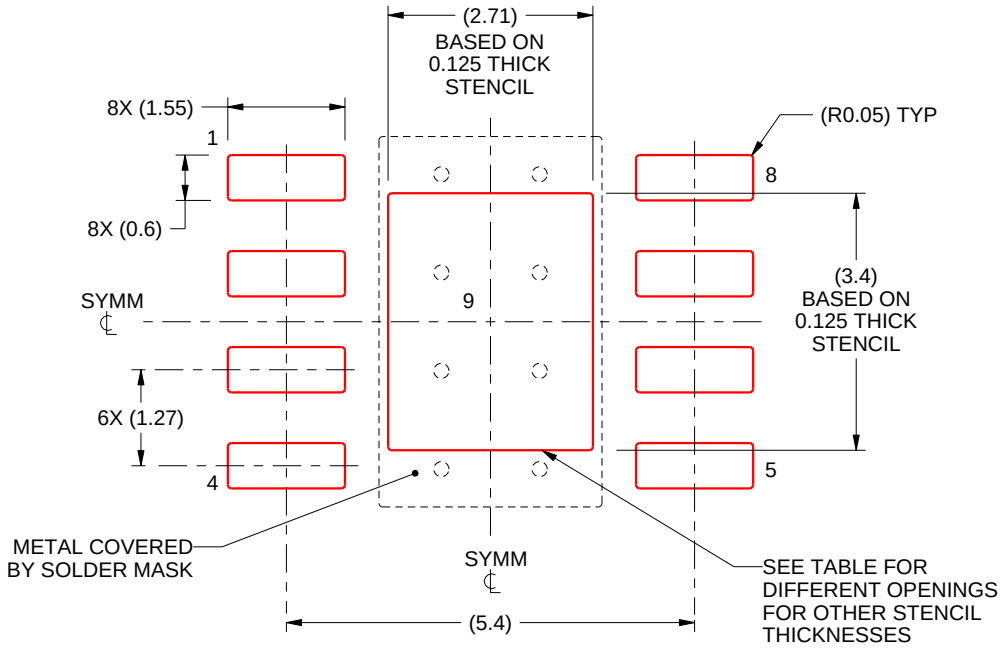
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

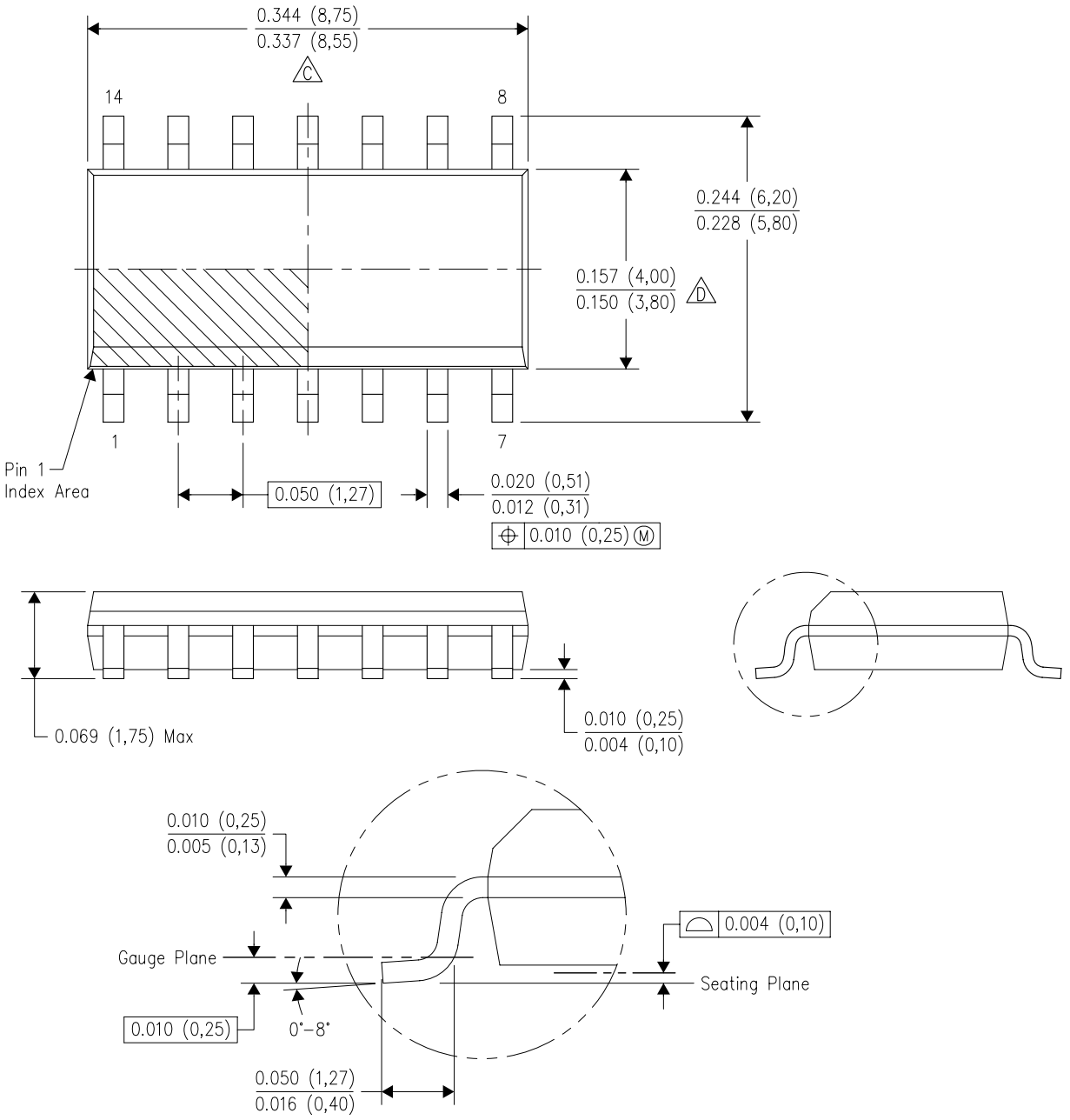
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

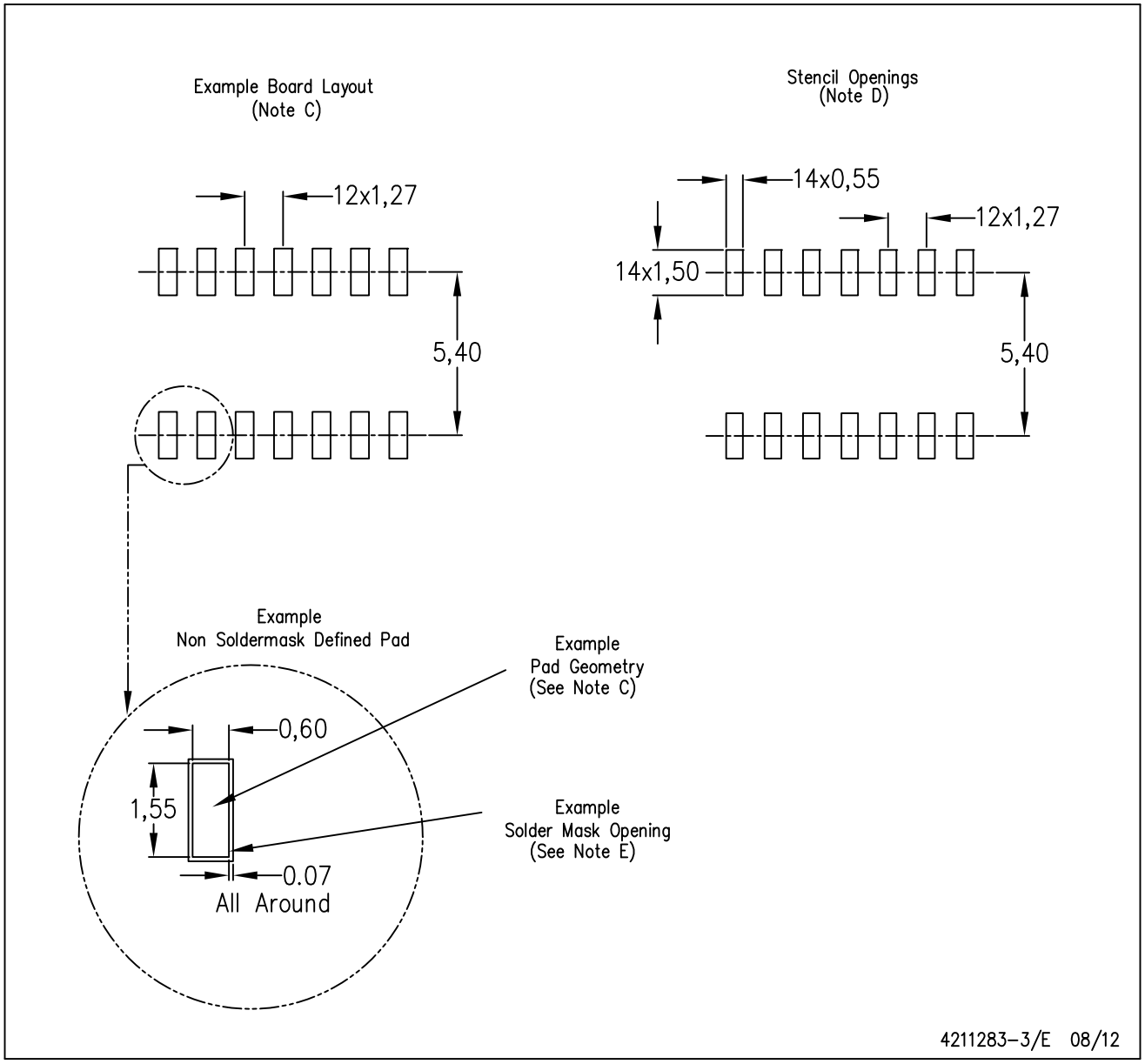
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

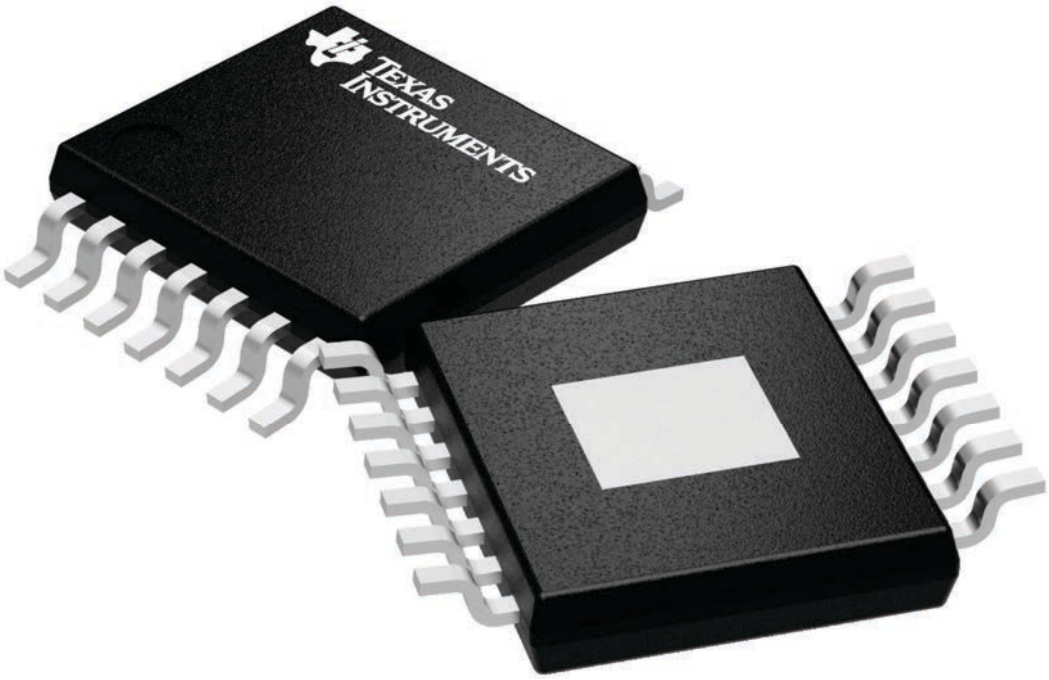
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

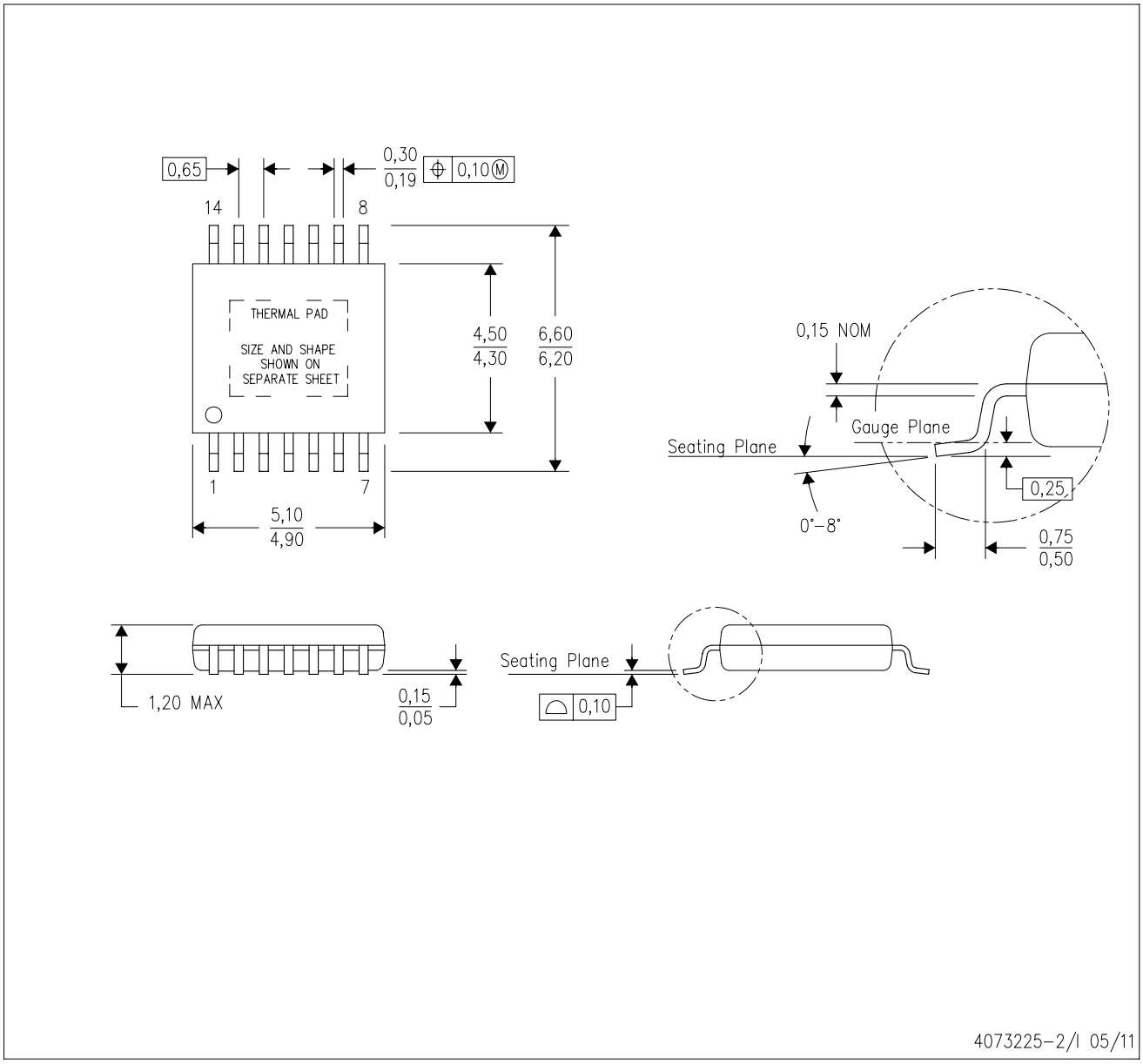
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

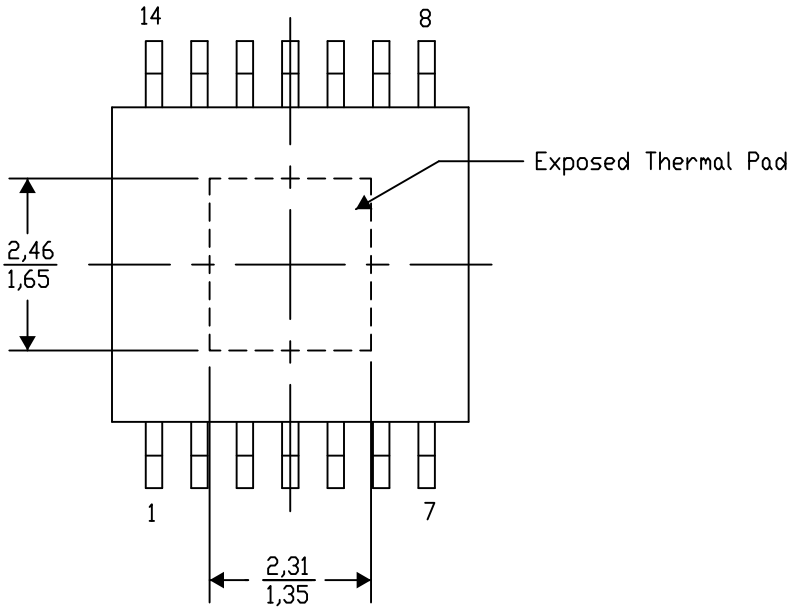
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

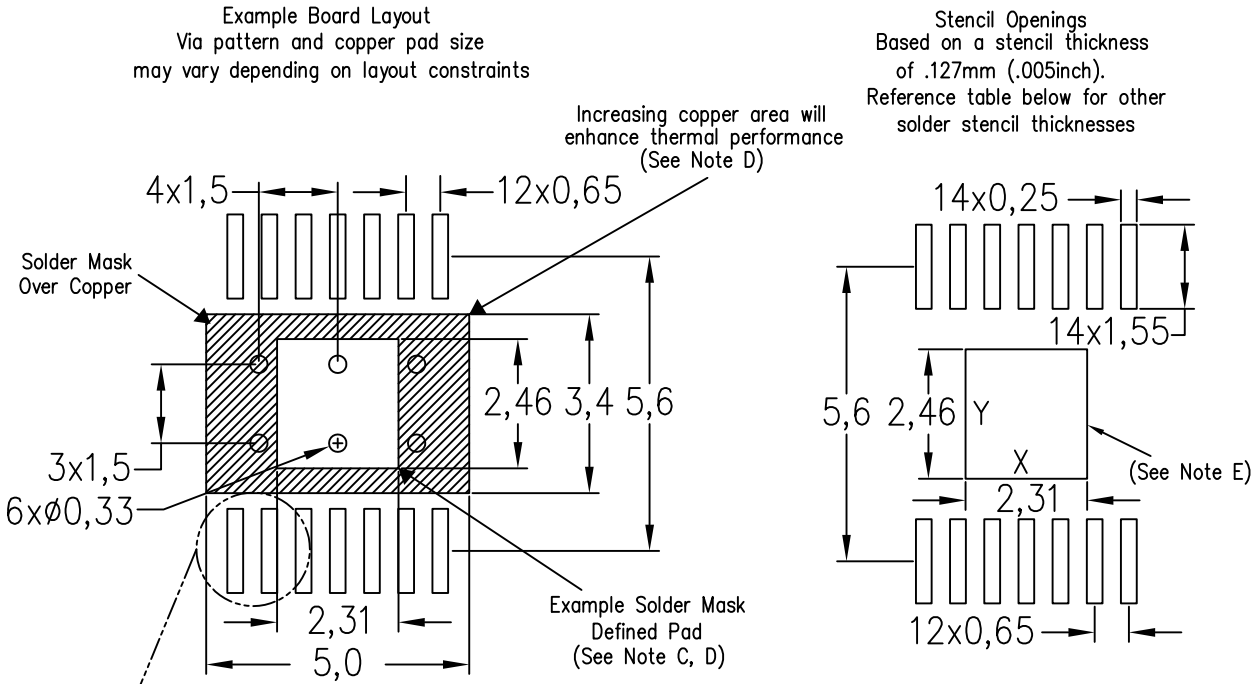
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

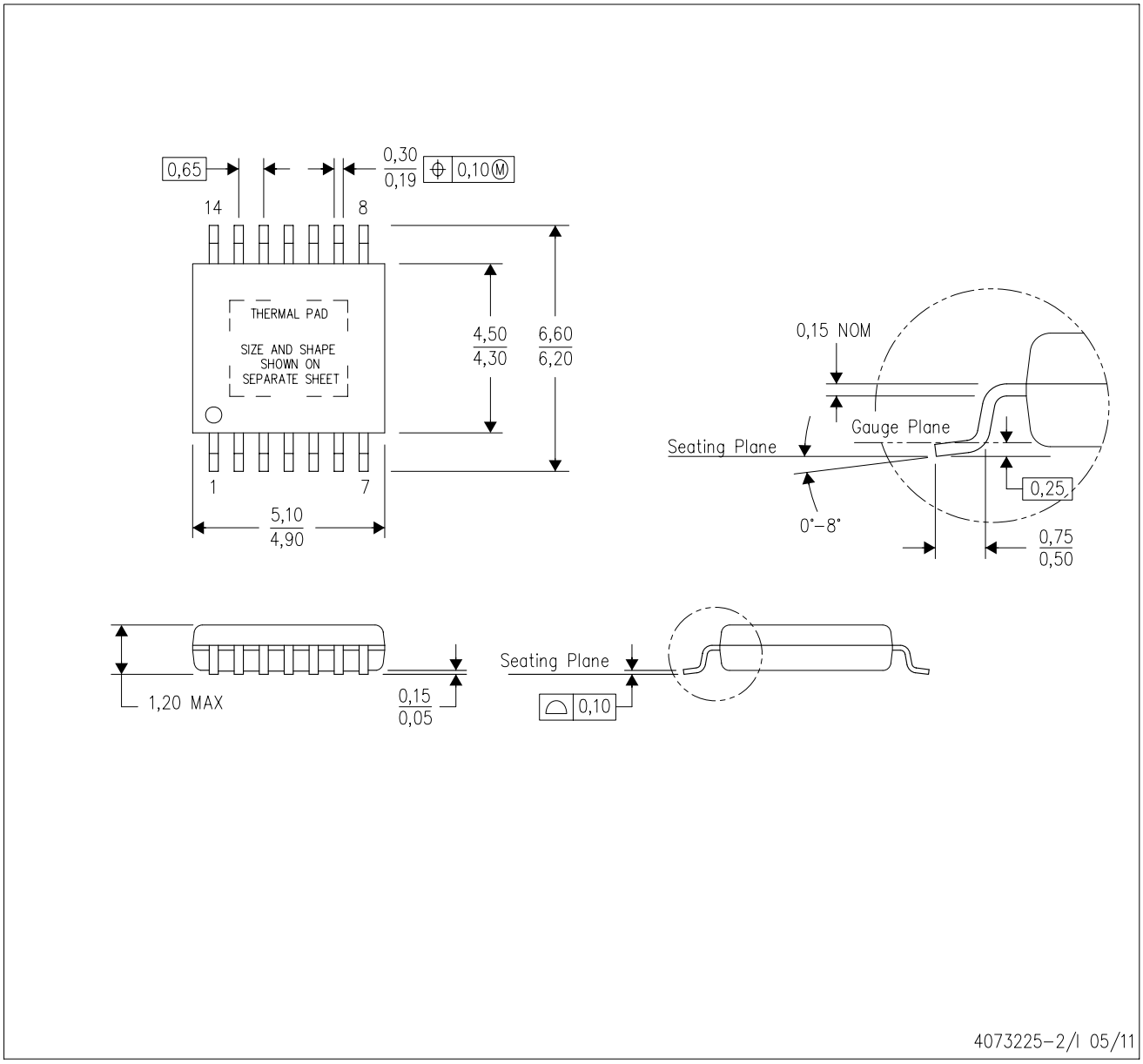


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

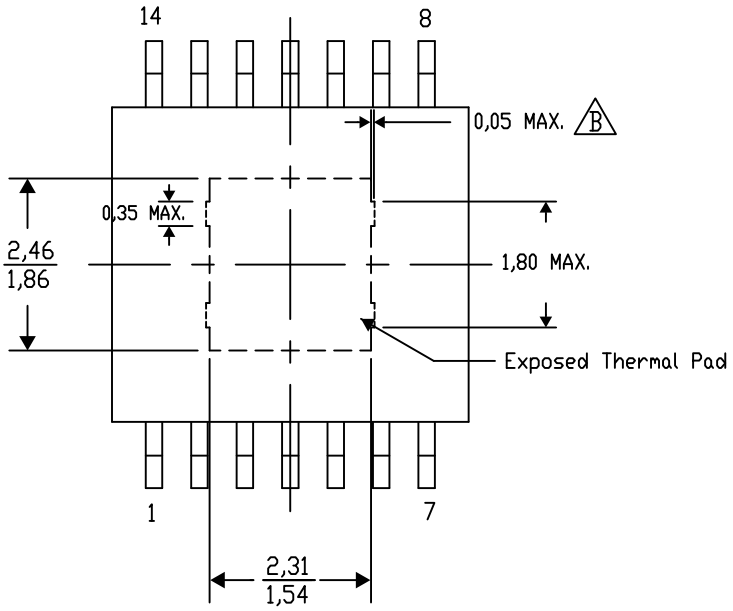
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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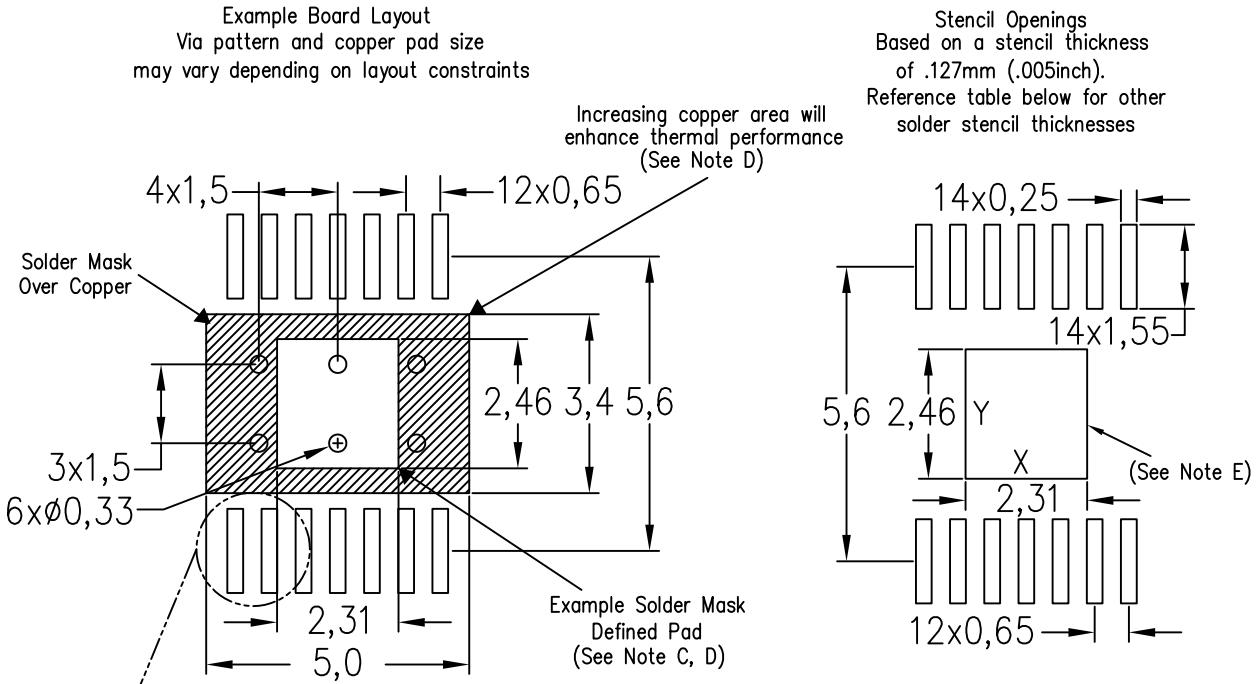

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

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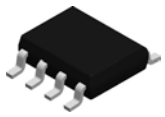
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

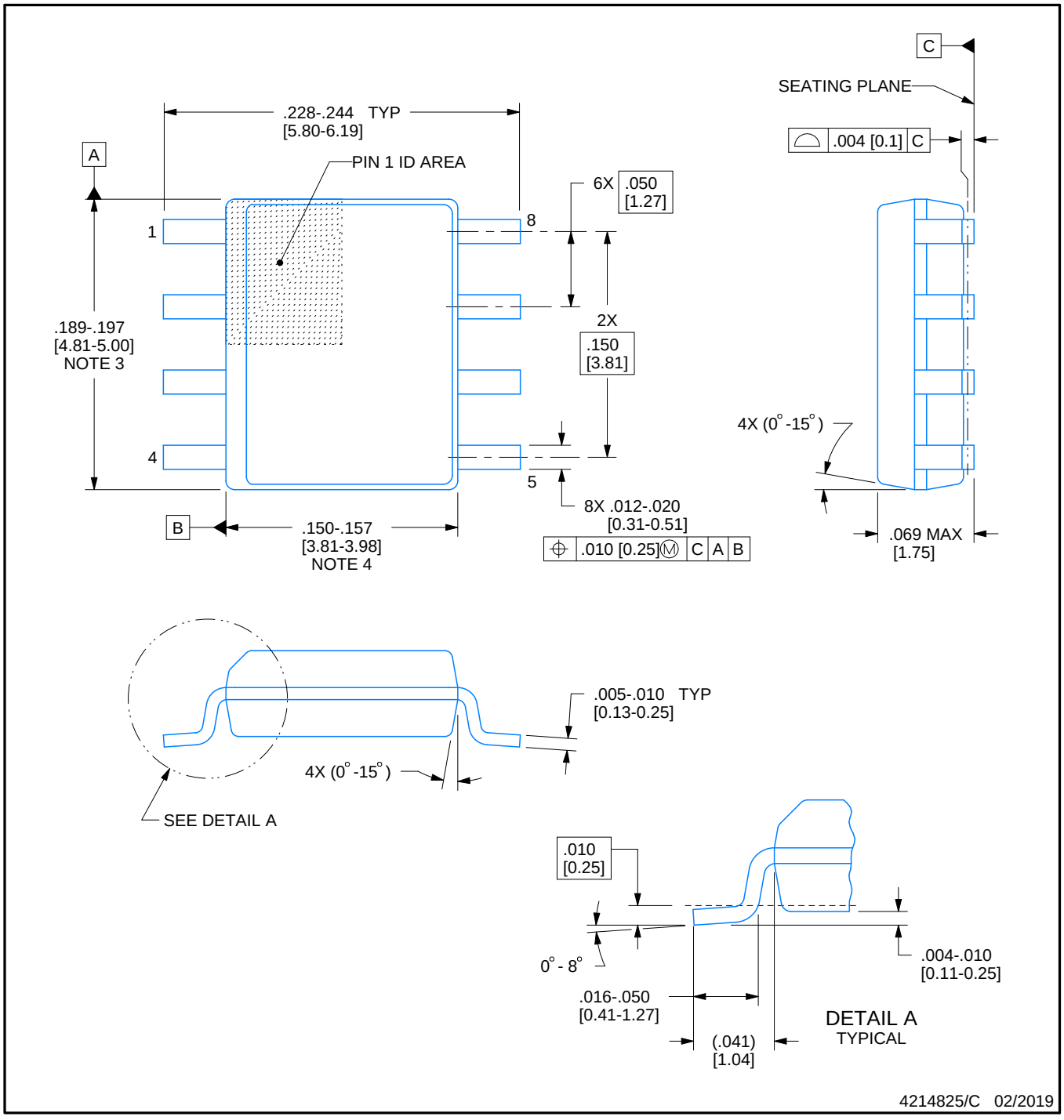


PACKAGE OUTLINE

D0008A

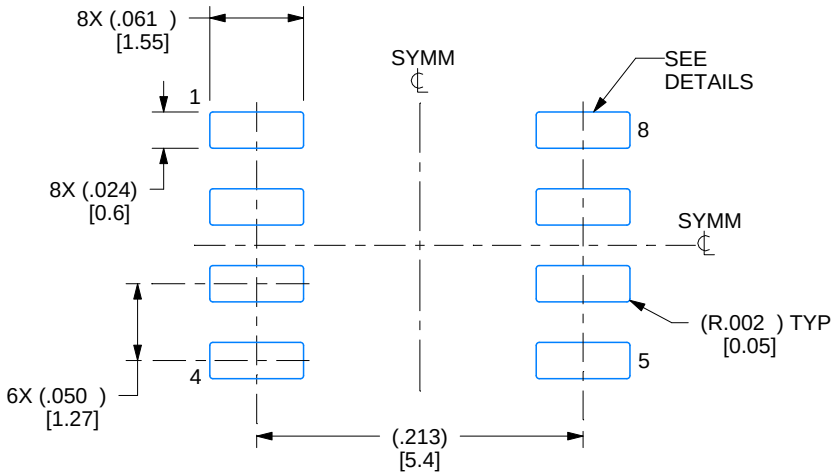
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

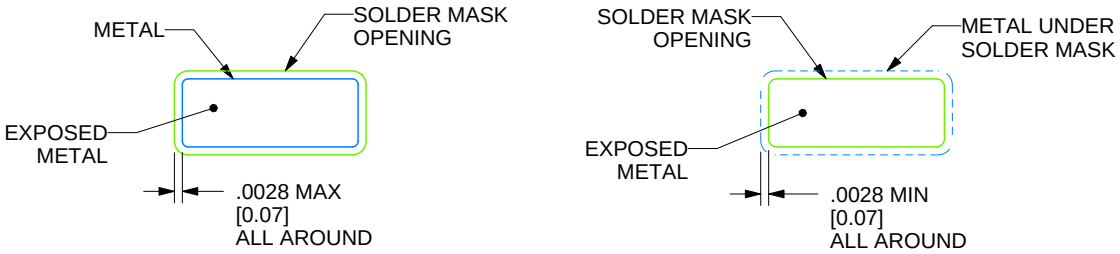


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

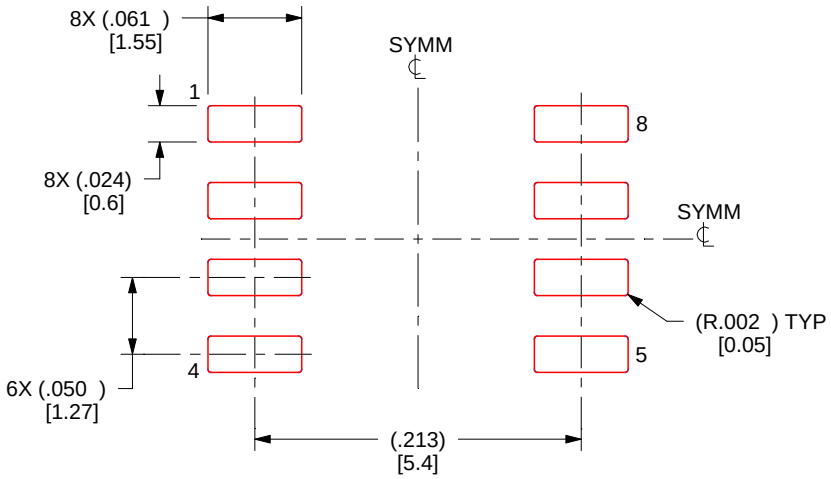
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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