eZ80F91 Modular Development Kit

User Manual

PRELIMINARY

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Document Disclaimer

Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

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ZILOG

Introduction

The eZ80F91 Modular Development Kit provides a general-purpose platform for creating a design based on ZiLOG's eZ80F91 microcontroller. The eZ80F91 is a member of ZiLOG's eZ80Acclaim!™ product family, which offers on-chip Flash capability. The eZ80F91 Modular Development Kit features an eZ80F91 Mini Enet Module and an eZ80Acclaim! MDS Adapter Board onto which the module mounts.

Kit Features

The key features of the eZ80F91 Modular Development Kit are:

- eZ80F91 Mini Enet Module:
  - eZ80F91 device operating at 50MHz, with 256KB of internal Flash memory and 8KB of internal SRAM memory.
  - 128KB of off-chip SRAM memory.
  - On-chip Ethernet Media Access Controller (EMAC).
  - Ethernet port and PHY.
  - Real-Time Clock with battery backup.
  - Footprint for an SIR IrDA transceiver.
  - Two 56-pin mini-module connectors for attachment to the eZ80Acclaim! MDS adapter board.
- eZ80Acclaim! MDS Adapter Board:
  - Footprint for 2M x 8 external Flash memory such as AM29LV160D.
  - Footprint for 10-bit bus switch such as 74CBTLV3384 to support external Flash.
  - RS232 connector with interface circuit for UART0.
  - ZDI and JTAG debug connectors.

  - Two 56-pin mini-module connectors.
  - Two 60-pin interface connectors for connection to an external application or development board (not supplied).
  - 32-pin header and footprint for a GPRS modem.
  - One green 3.3 OK LED.
  - One yellow Test LED and pushbutton.
  - 5VDC external power supply.
- Serial Smart Cable
- eZ80Acclaim!™ Software and Documentation CD-ROM
- ZiLOG ZTP TCP/IP stack CD-ROM
- Schematics for the eZ80F91 Mini Enet Module and eZ80Acclaim! MDS adapter board.

eZ80F91 Modular Development Kit Overview

The purpose of the eZ80F91 Modular Development Kit is to provide the design engineer with a set of tools for designing an application based on the eZ80F91 microcontroller.

A block diagram of the eZ80Acclaim! MDS adapter board is shown in Figure 1.

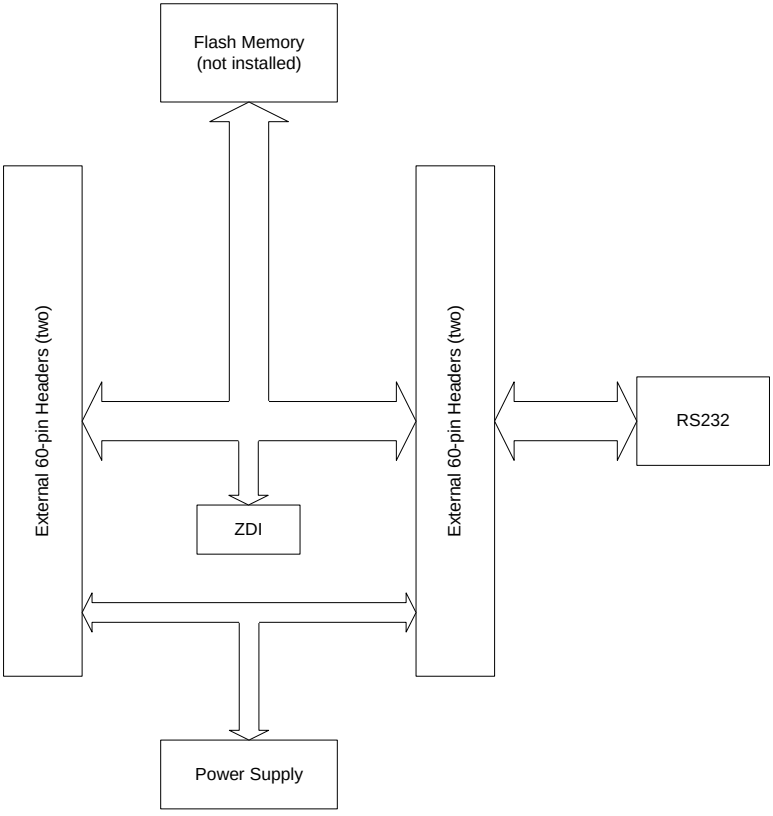

Figure 1. eZ80Acclaim! MDS Adapter Board Block Diagram

Figure 2 provides a block diagram of the eZ80F91 Mini Enet Module.

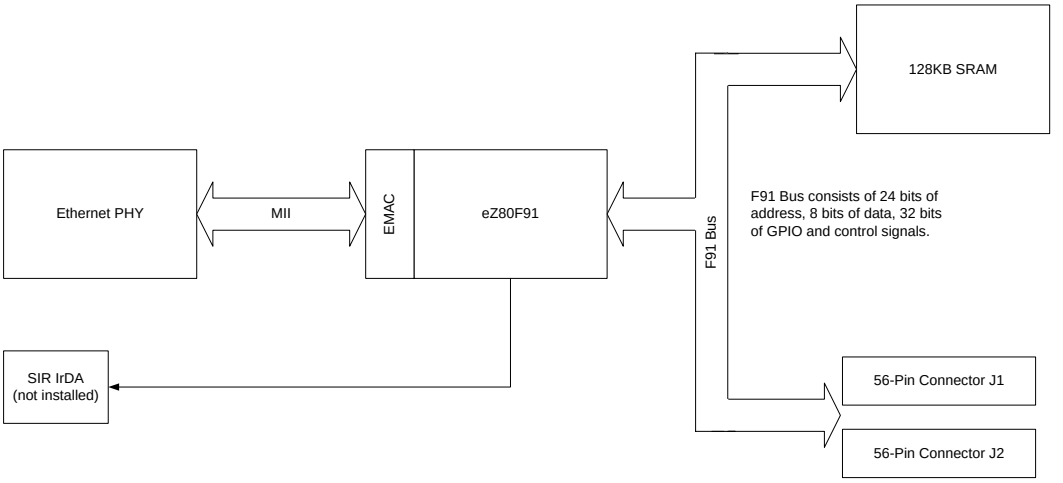

Figure 2. eZ80F91 Mini Enet Module Block Diagram

Schematics for the eZ80F91 Mini Enet Module and eZ80Acclaim! MDS adapter board are provided in the Schematics section starting on page 33.

eZ80Acclaim! MDS Adapter Board

This section describes functions of the eZ80Acclaim! MDS adapter board.

eZ80F91 Mini Enet Module Interface

The eZ80F91 Mini Enet Module interface on the eZ80Acclaim! MDS adapter board consists of two 56-pin mini-module receptacles.

Almost all of these receptacles' signals are connected directly to the CPU. Three input signals offer options to the application developer by disabling certain functions of the eZ80F91 Mini Enet Module.

These three input signals are:

- Disable IrDA ($\overline{\text{DIS\_IrDA}}$) (used only if you have installed an external SIR IrDA transceiver onto the eZ80F91 Mini Enet Module)
- $\overline{\text{F91\_WE}}$
- RTC_V_{DD}

A description of these three signals follows.

Disable IrDA. When the $\overline{\text{DIS\_IrDA}}$ input signal is pulled Low, the IrDA transceiver located on the eZ80F91 Mini Enet Module is disabled. As a result, UART0 can be used with the RS232 or the RS485 interfaces on the eZ80® Development Platform.

$\overline{\text{F91\_WE}}$. When the $\overline{\text{F91\_WE}}$ signal is active Low, internal Flash on the eZ80F91 chip is enabled for writing. This signal is inverted from the $\overline{\text{F91\_WP}}$ signal on the eZ80F91 chip.

RTC_V_{DD}. RTC_V_{DD} is a test point for the Real Time Clock power supply.

Peripheral Bus Mini-Module Connector, J1

Figure 3 illustrates the pin layout of the 56-pin Peripheral Bus Mini-Module Connector, J1, on the eZ80Acclaim! MDS adapter board. Table 1 identifies the pins and their functions.

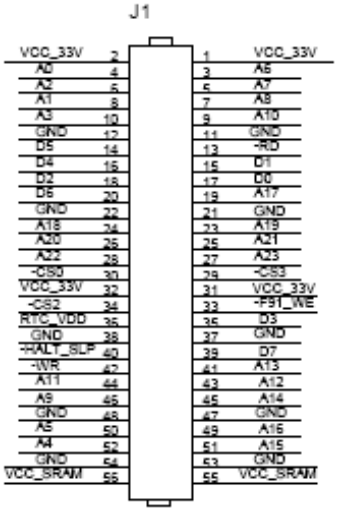

Figure 3. eZ80Acclaim! MDS Adapter Board
Peripheral Bus Mini-Module Connector J1 Pin Configuration

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
3	A6	Bidirectional	n/a	Yes	
4	A0	Bidirectional	n/a	Yes	
5	A7	Bidirectional	n/a	Yes	
6	A2	Bidirectional	n/a	Yes	
7	A8	Bidirectional	n/a	Yes	
8	A1	Bidirectional	n/a	Yes	
9	A102	Bidirectional	n/a	Yes	
10	A3	Bidirectional	n/a	Yes	
13	$\overline{RD}$	Output	Low	Yes	
14	D5	Bidirectional	n/a	Yes	
15	D1	Bidirectional	n/a	Yes	
16	D4	Bidirectional	n/a	Yes	
17	D0	Bidirectional	n/a	Yes	
18	D2	Bidirectional	n/a	Yes	
19	A17	Bidirectional	n/a	Yes	
20	D6	Bidirectional	n/a	Yes	

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
23	A19	Bidirectional	n/a	Yes	
24	A18	Bidirectional	n/a	Yes	
25	A21	Bidirectional	n/a	Yes	
26	A20	Bidirectional	n/a	Yes	
27	A23	Bidirectional	n/a	Yes	
28	$\overline{CS0}$	Output	Low	Yes	
29	$\overline{CS3}$	Output	Low	Yes	
33	$\overline{F91\_WE}$	Input	Low	No	Jumper on board
34	$\overline{CS0}$	Output	Low	Yes	
35	D3	Bidirectional	n/a	Yes	
36	RTC_V_{DD}	Input	n/a	Yes	
39	D7	Bidirectional	n/a	Yes	
40	$\overline{HALT\_SLP}$	Output	Low	Yes	
41	A13	Bidirectional	n/a	Yes	
42	$\overline{WR}$	Ouput	Low	Yes	
43	A12	Bidirectional	n/a	Yes	

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Table 1. eZ80Acclaim! MDS Adapter Board Peripheral Bus Connector J1 Identification[1,2] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal	Note
44	A11	Bidirectional	n/a	Yes	
45	A14	Bidirectional	n/a	Yes	
46	A9	Bidirectional	n/a	Yes	
49	A16	Bidirectional	n/a	Yes	
50	A5	Bidirectional	n/a	Yes	
51	A15	Bidirectional	n/a	Yes	
52	A4	Bidirectional	n/a	Yes	

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

I/O Mini-Module Connector, J2

Figure 4 illustrates the pin layout of the 56-pin Peripheral Bus Mini-Module Connector, J1, on the eZ80Acclaim! MDS adapter board. Table 2 identifies the pins and their functions.

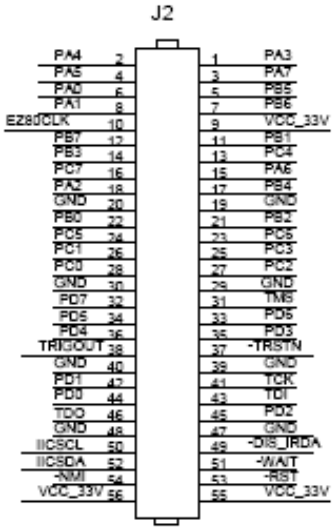

Figure 4. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	PA3	Bidirectional	n/a	Yes
2	PA4	Bidirectional	n/a	Yes
3	PA7	Bidirectional	n/a	Yes
4	PA5	Bidirectional	n/a	Yes
5	PB5	Bidirectional	n/a	Yes
6	PA0	Bidirectional	n/a	Yes
7	PB6	Bidirectional	n/a	Yes
8	PA1	Bidirectional	n/a	Yes
10	EZ80CLK	Output	n/a	Yes
11	PB1	Bidirectional	n/a	Yes
12	PB7	Bidirectional	n/a	Yes
13	PC4	Bidirectional	n/a	Yes
14	PB3	Bidirectional	n/a	Yes
15	PA6	Bidirectional	n/a	Yes
16	PC7	Bidirectional	n/a	Yes
17	PB4	Bidirectional	n/a	Yes
18	PA2	Bidirectional	n/a	Yes
21	PB3	Bidirectional	n/a	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
22	PB0	Bidirectional	n/a	Yes
23	PC6	Bidirectional	n/a	Yes
24	PC5	Bidirectional	n/a	Yes
25	PC3	Bidirectional	n/a	Yes
26	PC1	Bidirectional	n/a	Yes
27	PC2	Bidirectional	n/a	Yes
28	PC0	Bidirectional	n/a	Yes
31	TMS	Input	n/a	Yes
32	PD7	Bidirectional	n/a	Yes
33	PD6	Bidirectional	n/a	Yes
34	PD5	Bidirectional	n/a	Yes
35	PD3	Bidirectional	n/a	Yes
36	PD4	Bidirectional	n/a	Yes
37	$\overline{\text{TRSTN}}$	Input	Low	Yes
38	TRIGOUT	Output	n/a	Yes
41	TCK	Input	n/a	Yes
42	PD1	Bidirectional	n/a	Yes
43	TDI	Bidirectional	n/a	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 2. eZ80Acclaim! MDS Adapter Board I/O Mini-Module Connector J2 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
44	PD0	Bidirectional	n/a	Yes
45	PD2	Bidirectional	n/a	Yes
46	TDO	Output	n/a	Yes
49	$\overline{\text{DIS\_IRDA}}$	Input	Low	No
50	IICSCL	I/O	n/a	Yes
51	$\overline{\text{WAIT}}$	Input	Low	Yes
52	IICSDA	I/O	n/a	Yes
53	$\overline{\text{RST}}$	I/O	Low	Yes
54	$\overline{\text{NMI}}$	Input	Low	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Peripheral Bus External Connector JP1

Figure 5 illustrates the pin layout of Peripheral Bus External Connector JP2 in the 60-pin header on the eZ80Acclaim! MDS adapter board. Table 3 identifies the pins and their functions.

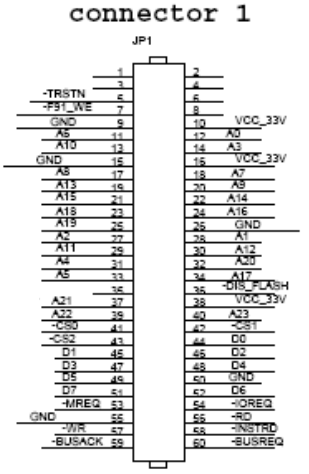

Figure 5. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1-4, 6, 8, 35	unused	n/a	n/a	n/a
5	$\overline{\text{TRSTN}}$	Input	Low	Yes
11	A6	Bidirectional	n/a	Yes
12	A0	Bidirectional	n/a	Yes
13	A10	Bidirectional	n/a	Yes
14	A3	Bidirectional	n/a	Yes
17	A8	Bidirectional	n/a	Yes
18	A7	Bidirectional	n/a	Yes
19	A13	Bidirectional	n/a	Yes
20	A9	Bidirectional	n/a	Yes
21	A15	Bidirectional	n/a	Yes
22	A14	Bidirectional	n/a	Yes
23	A18	Bidirectional	n/a	Yes
24	A16	Bidirectional	n/a	Yes
25	A19	Bidirectional	n/a	Yes
27	A2	Bidirectional	n/a	Yes
28	A1	Bidirectional	n/a	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
29	A11	Bidirectional	n/a	Yes
30	A12	Bidirectional	n/a	Yes
31	A4	Bidirectional	n/a	Yes
32	A20	Bidirectional	n/a	Yes
33	A5	Bidirectional	n/a	Yes
34	A17	Bidirectional	n/a	Yes
36	$\overline{\text{DIS\_FLASH}}$	Input	Low	No
37	A21	Bidirectional	n/a	Yes
39	A22	Bidirectional	n/a	Yes
40	A23	Bidirectional	n/a	Yes
41	$\overline{\text{CS0}}$	Output	Low	Yes
42	$\overline{\text{CS1}}$	Output	Low	Yes
43	$\overline{\text{CS2}}$	Output	Low	Yes
44-49	D[0:5]	Bidirectional	n/a	Yes
51	D7	Bidirectional	n/a	Yes
52	D6	Bidirectional	n/a	Yes
53	$\overline{\text{MREQ}}$	Output	Low	Yes
54	$\overline{\text{IOREQ}}$	Output	Low	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 3. eZ80Acclaim! MDS Adapter Board Peripheral Bus External Connector JP1 Identification[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
56	$\overline{RD}$	Ouput	Low	Yes
57	$\overline{WR}$	Output	Low	Yes
58	$\overline{INSTRD}$	Output	Low	Yes
59	$\overline{BUSACK}$	Output	Low	Yes
60	$\overline{BUSREQ}$	Input	Low	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

I/O External Connector JP2

Figure 6 illustrates the pin layout of the I/O Connector in the 60-pin header on the eZ80Acclaim! MDS adapter board. Table 4 identifies the pins and their functions.

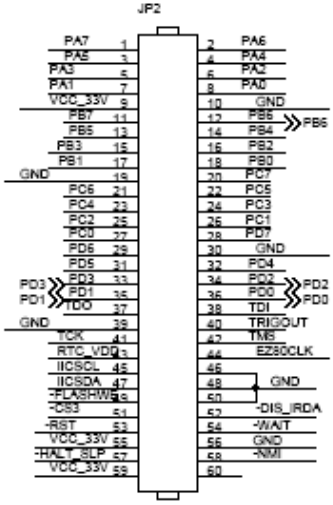

Figure 6. eZ80Acclaim! MDS Adapter Board I/O External Connector JP2

Table 4. eZ80Acclaim! MDS Adapter Board I/O External Connector JP2[1] Identification

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1 - 8	PA7 to PA0	Bidirectional	n/a	Yes
11 - 18	PB7 to PB0	Bidirectional	n/a	Yes
20 - 27	PC7 to PC0	Bidirectional	n/a	Yes
28, 29	PD7, PD6	Bidirectional	n/a	Yes
31 - 36	PD5 to PD0	Bidirectional	n/a	Yes
37	TDO	Output	n/a	Yes
38	TDI	I/O	n/a	Yes
40	TRIGOUT	Output	n/a	Yes
41	TCK	Input	n/a	Yes
42	TMS	Input	n/a	Yes
43	RTC_V_{DD}	Input	n/a	Yes
44	EZ80CLK	Output	n/a	Yes
45	IICSCL	I/O	n/a	Yes
47	IICSDA	I/O	n/a	Yes
49	$\overline{\text{FLASHWE}}$	Input	Low	No
51	$\overline{\text{CS3}}$	Output	Low	Yes
52	$\overline{\text{DIS\_IRDA}}$	Input	Low	No
53	$\overline{\text{RST}}$	I/O	Low	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Table 4. eZ80Acclaim! MDS Adapter Board I/O External Connector JP2[1] Identification (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
54	$\overline{\text{WAIT}}$	Input	Low	Yes
57	$\overline{\text{HALT\_SLP}}$	Output	Low	Yes
58	$\overline{\text{NMI}}$	Input	Low	Yes
60	unused	n/a	n/a	n/a

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80Acclaim! MDS adapter board schematics on pages 33 through 34.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

eZ80Acclaim! MDS Adapter Board Jumper Settings

The eZ80Acclaim! MDS adapter board contains four jumpers that are described in Table 5.

Table 5. eZ80Acclaim MDS Adapter Board Jumper Settings

Jumper Name	Position	Function	Affected Device
J4, FL_EN	IN (Default)	On-board Flash is enabled	On-board Flash (when installed)
	OUT	On-board Flash is disabled	
J6, FL_WEN[1]	IN	On-board Flash is disabled for writing.	On-board Flash (when installed)
	OUT	On-board Flash is enabled for writing	
J8, RS232-1 DIS	IN	RS232 output on connector P2 is disabled	DB9 connector P2
	OUT	RS232 output on connector P2 is enabled	
J9, IRDA_DIS[2]	IN (Default)	IrDA transceiver on eZ80F91 Mini Enet Module is disabled	IrDA transceiver (when installed)
	OUT	IrDA transceiver on eZ80F91 Mini Enet Module is enabled	

Notes:
1. If AM29LV160 is used, J6 and R6 should be OUT. If AT49BV162 is used, R6 should be IN, and J6 should be OUT.
2. Jumper J9 functions only when user has installed IrDA transceiver on eZ80F91 Mini Enet Module.

eZ80F91 Mini Enet Module

This section describes the eZ80F91 Mini Enet Module hardware, its interfaces and key components, including the CPU, real-time clock, and memory.

Functional Description

The eZ80F91 Mini Enet Module is a compact, high-performance module specially designed for the rapid development and deployment of embedded systems.

Despite its small footprint, the eZ80F91 Mini Enet Module provides a CPU, Flash memory, Ethernet interface, SRAM, and a real-time clock. This module is powered by the eZ80F91 microcontroller, a member of ZILOG's eZ80Acclaim!™ product family.

Fast Buffer

A Fast Buffer is located on the data bus to Flash memory. The purpose of this Fast Buffer is to avoid bus contention that can exist due to the slow turn-off time of Flash memory and the fast bus turn-around time of the eZ80F91 device (a generic feature of the eZ80Acclaim!™ family when is used in native mode). The discussion that follows references Figure 7.

Bus contention can occur when two or more devices drive a common bus. $\overline{CS0}$ on the eZ80F91 device drives the Flash $\overline{CE}$. Upon accessing Flash memory, $\overline{CS0}$ is driven High a maximum of 8.8ns after the next rising edge of the CPU Clock (T6—please refer to the External Memory Read Timing diagram in the eZ80F91 Product Specification (PS0192) for assistance). The Flash turn-off time (T_{OD}) is 25ns—the duration from $\overline{OE}$ or $\overline{CE}$ going High to Flash output drivers in a high-impedance state. For further information, see the MT28F008 data sheet on www.micron.com.

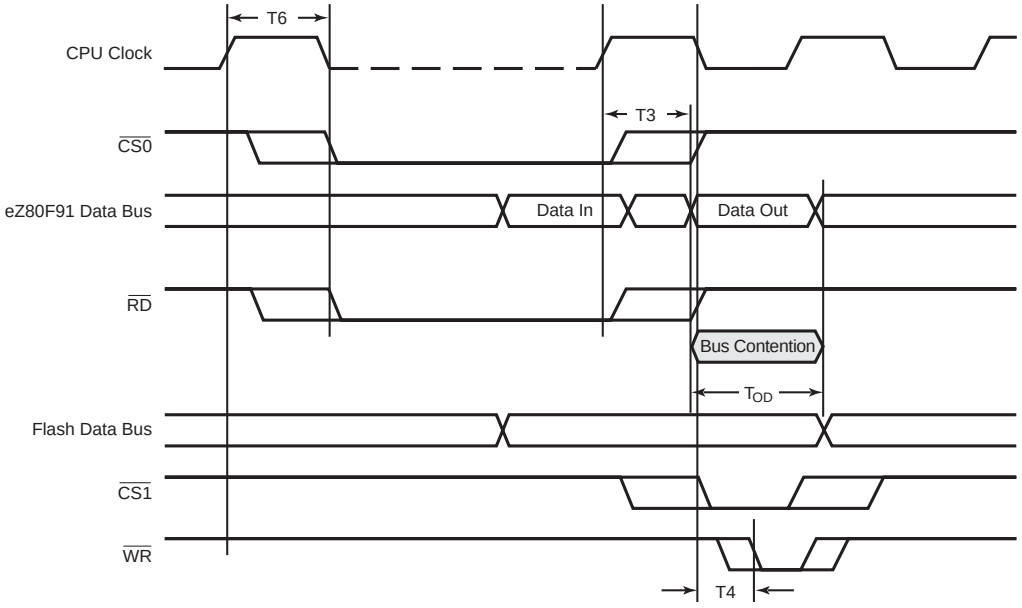

Figure 7. Possible Bus Contention without Fast Buffer

Essentially, after the eZ80F91 device accesses Flash memory, a time duration of 8.8ns + 25ns = 33.8ns can transpire before Flash memory stops driving the data bus. At that time, the eZ80F91 device is well into the next bus cycle. Assuming this next cycle is the Memory Write cycle, then the data output of the eZ80F91 device is valid not later than T3 = 7.5ns, and the write pulse is asserted not later than 4.5ns after the falling edge of the CPU Clock (14.5ns from the rising edge if the CPU Clock is 50MHz). The duration of bus contention, $T_{CON,}$ is 33.8ns – 7.5ns = 26.3ns. Refer to the External Memory Write Timing diagram in the eZ80F91 Product Specification (PS0192) for assistance.

With the addition of a Fast buffer, Flash turn-off time is reduced from 25ns to 5.5ns. Bus contention can still occur, but the amount of time it consumes is not T_{CON} = 26.3ns but rather T_{CON} = (8.8ns – 7.5ns + 5.5ns) = 6.8ns. At this faster rate, data that is being written does not become corrupted because the write pulse is not yet asserted.

As of the date of publication of this document, ZiLOG has not completed an analysis of the effect that this 6.8ns period of bus contention has on the design. An Application Note from Cypress Semiconductor titled *NoBL SRAM and Bus Contention* further explains this bus contention issue.

Operational Description

The purpose of the eZ80F91 Mini Enet Module as a feature of the eZ80F91 Modular Development Kit is to provide application developers with a design platform that enables them to make use of such eZ80F91 device features of the as on-chip EMAC, SRAM, Flash, etc.

eZ80F91 Mini Enet Module Memory

Static RAM

The eZ80F91 Mini Enet Module features 128KB of fast SRAM. Access speed is typically 12ns, allowing zero-wait-state operation at 50MHz. With the CPU at 50MHz, SRAM can be accessed with zero wait states in eZ80 mode. CS1_CTL ($\overline{CS1}$) can be set to `08h` (no wait states).

Note: The eZ80F91 Mini Enet Module is shipped with SRAM powered from the same power supply as the eZ80F91 device. The SRAM may also be powered separately by battery. To power SRAM from battery:

1. Remove R15
2. Ensure that R14 is in place.
3. Connect battery (-) to GND.
4. Connect battery (+) to J10.

Flash Memory

The eZ80F91 Mini Enet Module features 256KB of on-chip Flash memory, which can be programmed a single byte at a time, or in bursts of up to 256 bytes. Write operations can be performed using either memory or I/O instructions. Erasing bytes in Flash memory returns them to a value of FFh. Both the MASS ERASE and PAGE ERASE operations are self-timed by the Flash controller, leaving the CPU free to execute other operations in parallel. Upon power-up, the on-chip Flash memory is located in the address range 000000h–03FFFFh. Four wait states are programmed in Flash control register F8h.

On-chip Flash memory is prioritized over all external Chip Selects, can be enabled or disabled (power-on enabled), and can be programmed within any 256KB address space in the 16MB address range.

The eZ80F91 Mini Enet Module features the following memory configurations:

- On-chip SRAM: 8KB
- Off-chip SRAM: 128KB
- On-chip Flash: 256KB

Refer to the *eZ80F91 Product Specification*, PS0192, for details on programming internal Flash memory.

External Flash Memory

The eZ80F91 Mini Enet Module provides a footprint for 2MB of external Flash. The module supports additional external Flash devices via the full system bus, which is available on the expansion interface connectors.

Reset Generator

A supervisory chip on the eZ80Acclaim! MDS adapter board is connected to the eZ80F91 Reset input pin via pin 53 of mini-module connector J2.. It performs reliable Power-On Reset functions, generating a reset pulse

with a duration of 200ms if the power supply drops below 2.93V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80F91 Modular Development Kit with a low-impedance output (e.g. a 100-Ohm push button).

IrDA Transceiver

The eZ80F91 Mini Enet Module is shipped without an IrDA transceiver installed.

If you install an on-board transceiver, such as the ZiLOG ZHX1810, it is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, IR_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80F91 device.

To use the UART0 as a console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IRDA_SD) High or by pulling the $\overline{\text{DIS\_IRDA}}$ pin on the I/O connector Low. The shutdown feature is used for power savings. To enable the IrDA transceiver, $\overline{\text{DIS\_IRDA}}$ is left floating and PD2 is pulled Low.

The RxD and TxD signals on the transceiver perform the same functions as a standard RS232 port. However, these signals are processed as IrDA 3/16 coding pulses (sometimes called IrDA encoder/decoder pulses). When the IrDA function is enabled, the final output to the RxD and TxD pins are routed through the 3/16 pulse generator.

Another signal that is used in the eZ80F91 Mini Enet Module's IrDA system is Shut_Down (SD). The SD pin is connected to PD2 on the eZ80F91 Mini Enet Module. The IrDA control software on the user's wireless device must enable this pin to wake the IrDA transceiver. The SD pin must be set Low to enable the IrDA transceiver. On the eZ80F91 Mini Enet Module, a two-input OR gate is used to allow an external pin to shut

down the IrDA transceiver. Both pins must be set Low to enable this function.

The eZ80F91 Mini Enet Module features an Infrared Encoder/Decoder register that configures the IrDA function. This register is located at address 0BFh in the internal I/O register map.

The Infrared Encoder/Decoder register contains three control bits. Bit 0 enables or disables the IrDA encoder/decoder block. Bit 1, if it is set, enables received data to pass into the UART0 Receive FIFO data buffer. Bit 2 is a test function that provides a loopback sequence from the TxD pin to the RxD input.

Bit 1, the Receive Enable bit, is used to block data from filling up the Receive FIFO when the eZ80F91 Mini Enet Module is transmitting data. Because IrDA signal passes through the air as its transmission medium, transmitted data can also be received. This Receive Enable bit prevents this data from being received. After the eZ80F91 Mini Enet Module completes transmitting, this bit is changed to allow for incoming messages.

The code that follows provides an example of how this function is enabled on the eZ80F91 Mini Enet Module.

```
//Init_IRDA
// Make sure to first set PD2 as a port bit, an output and set it Low.

PD_ALT1 &= 0xFC;          // PD0 = uart0tx, PD1 = uart0_rx
PD_ALT2 |= 0x03;          // Enable alternate function
UART_LCTL0= 0x80;         // Select dlab to access baud rate generator
BRG_DLRL0=0x2F;           // Baud rate Masterclock/(16*baudrate)
BRG_DLRH0=0x00;           // High byte of baud rate
UART_LCTL0=0x00;          // Disable dlab
UART_FCTL0=0xC7;          // Clear tx fifo, enable fifo
UART_LCTL0=0x03;          // 8bit, N, 1 stop
IR_CTL = 0x03;            // enable IRDA Encode/decode and Receive
                          // enable bit.
```

```
//IRDA_Xmit
IR_CTL = 0x01;          //Disable receive
Putchar(0xb0);          //Output a byte to the uart0 port.
```

Internal On-Chip Flash Memory

To program the 32K boot block on the internal on-chip Flash memory, shunt JP1 on the eZ80F91 Mini Enet Module must be installed. Table 6 lists the settings shunt JP1.

Table 6. Shunt JP1, eZ80F91 Mini Enet Module

Symbol	Jumper Name	Shunt Status	Function	Affected Device
JP1	$\overline{\text{F91\_WE}}$	In (Default)	On-chip Flash is enabled for writing to boot block.	On-chip Flash
		Out	On-chip Flash memory boot block is write-protected.	On-chip Flash

Flash Loader Utility

The Flash Loader utility integrated within ZDS II allows the user a convenient way to program on-chip Flash memory. Please refer to the *ZiLOG Developer Studio—eZ80Acclaim! User Manual* (UM0144) for more details.

ZDS II

ZiLOG Developer Studio II (ZDS II) Integrated Development Environment is a complete stand-alone system that provides a state-of-the-art development environment. Based on the Windows® Win98SE/NT4.0-SP6/Win2000-SP2/WinXP user interfaces, ZDS II integrates a language-sensitive editor, project manager, C-Compiler, assembler, linker, librarian, and source-level symbolic debugger that supports the eZ80F91 device.

For more information on ZDS II, refer to the *ZiLOG Developer Studio—eZ80Acclaim!™ User Manual*, UM0144.

Troubleshooting

Overview

Before contacting ZiLOG Customer Support to submit a problem report, please follow these simple steps. If a hardware failure is suspected, contact a local ZiLOG representative for assistance.

IrDA Port Not Working

If you plan on using the IrDA transceiver on the eZ80F91 Mini Enet Module, make sure the hardware is set up as follows:

- Jumper J9 on the eZ80Accaim! MDS adapter board must be OFF (to enable the control gate that drives the IrDA device)
- Set port pin PD2 Low. When this port pin and Jumper J9 are turned OFF, the IrDA device is enabled.
- Disable the RS232 output by installing a shunt on jumper J8 on the eZ80Acclaim! MDS adapter board.

Contacting ZiLOG Customer Support

For additional troubleshooting solutions, see ZDS II Online Help.

For valuable information about hardware and software development tools, visit ZiLOG Customer Support online. Download the latest released version of ZiLOG Developer Studio!

Get the latest software updates from ZiLOG as soon as they are available!

eZ80Acclaim! MDS Adapter Board Schematic

Figures 8 and 9 provide a schematic for the eZ80Acclaim! MDS adapter board.The SRAM chip U2 and buffer U1 are not installed; they are shown for reference purposes only.

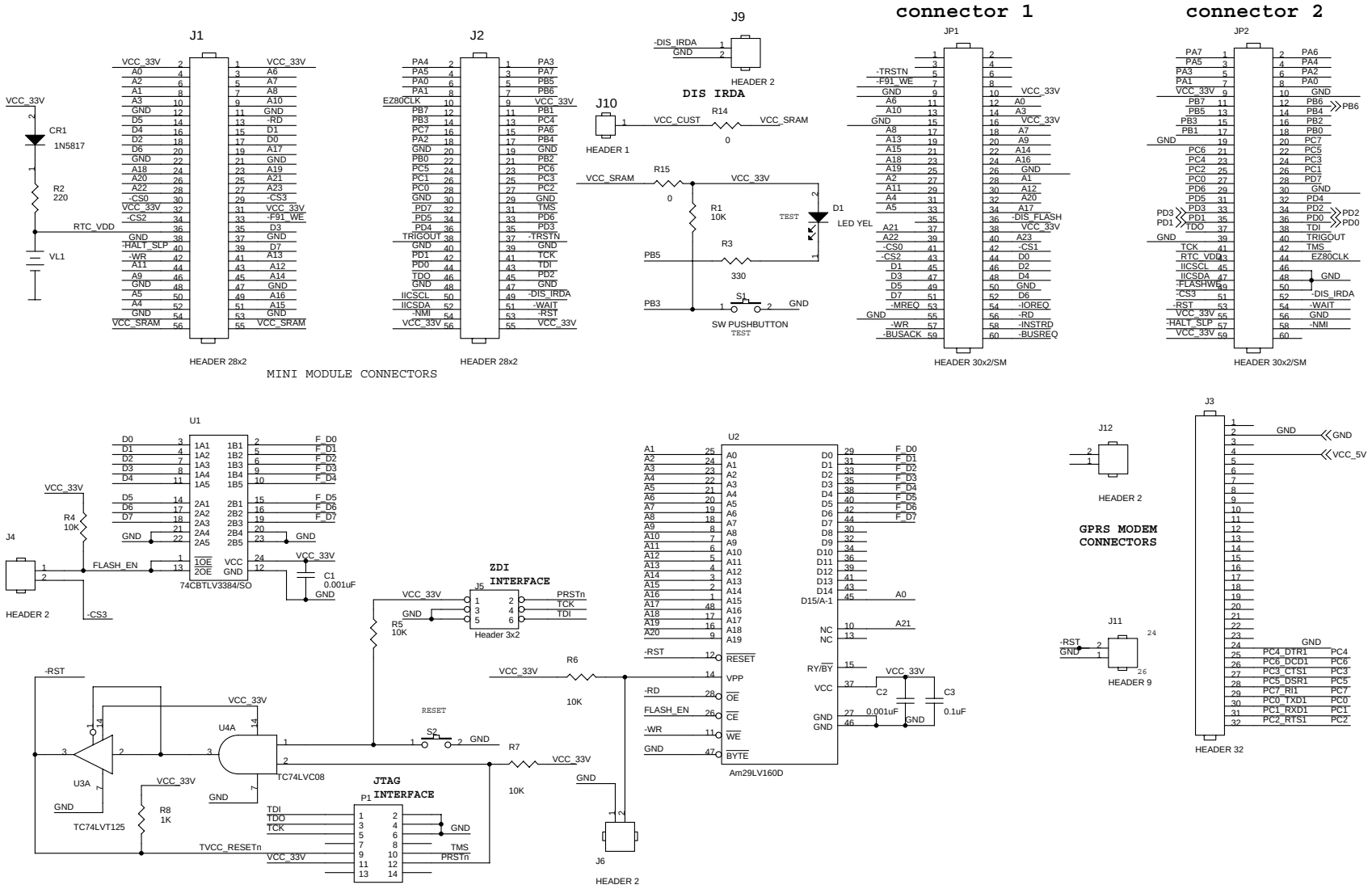

Figure 8. eZ80Acclaim MDS Adapter Board Schematic (1 of 2)

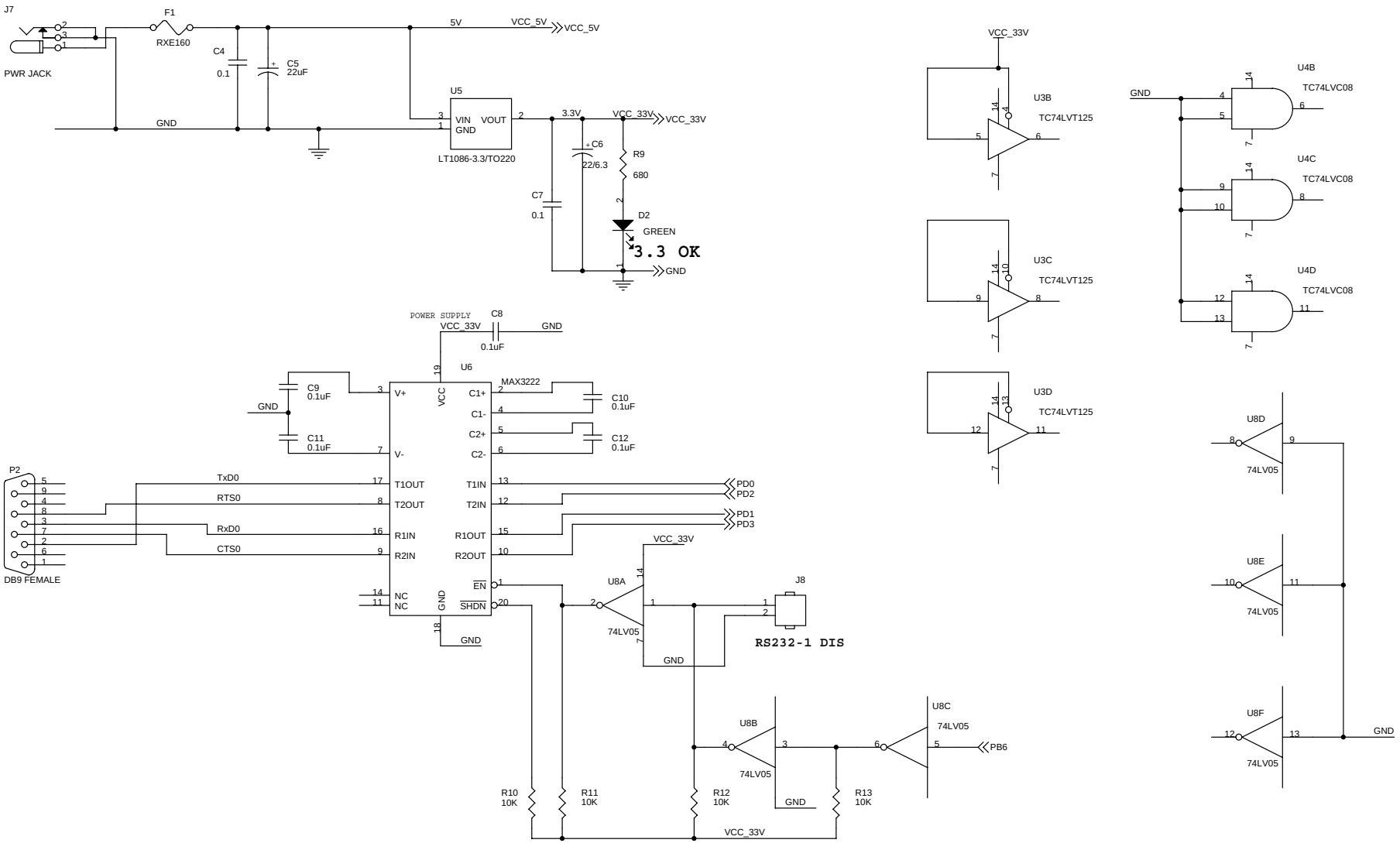

Figure 9. eZ80Acclaim! MDS Adapter Board Schematic (2 of 2)

eZ80F91 Mini Enet Module

Figures 10 through 11 diagram the layout of the eZ80F91 Mini Enet Module. The IrDA device is not installed on the module; it appears for reference purposes only.

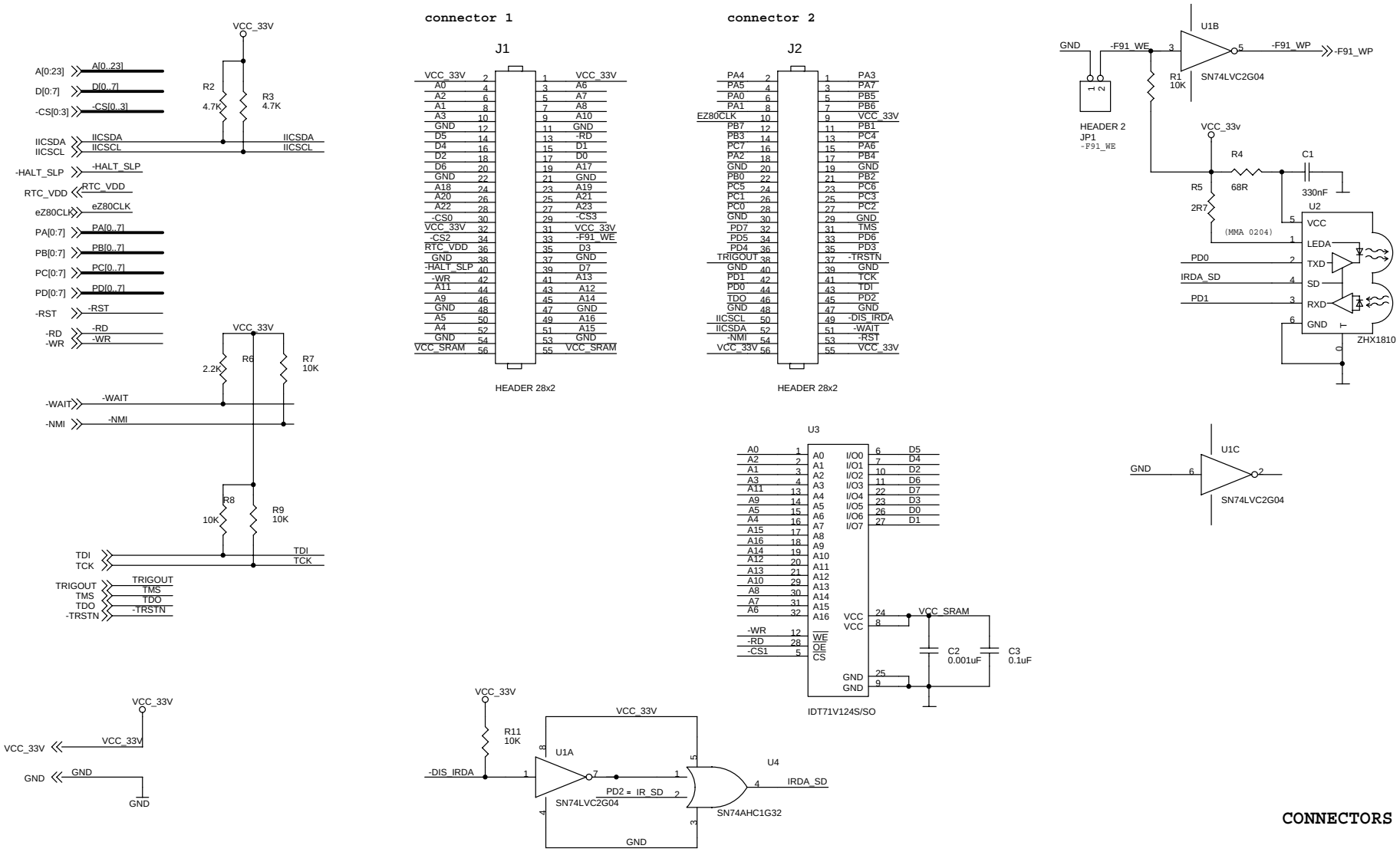

Figure 10. eZ80F91 Mini Enet Module Schematic (1 of 2)

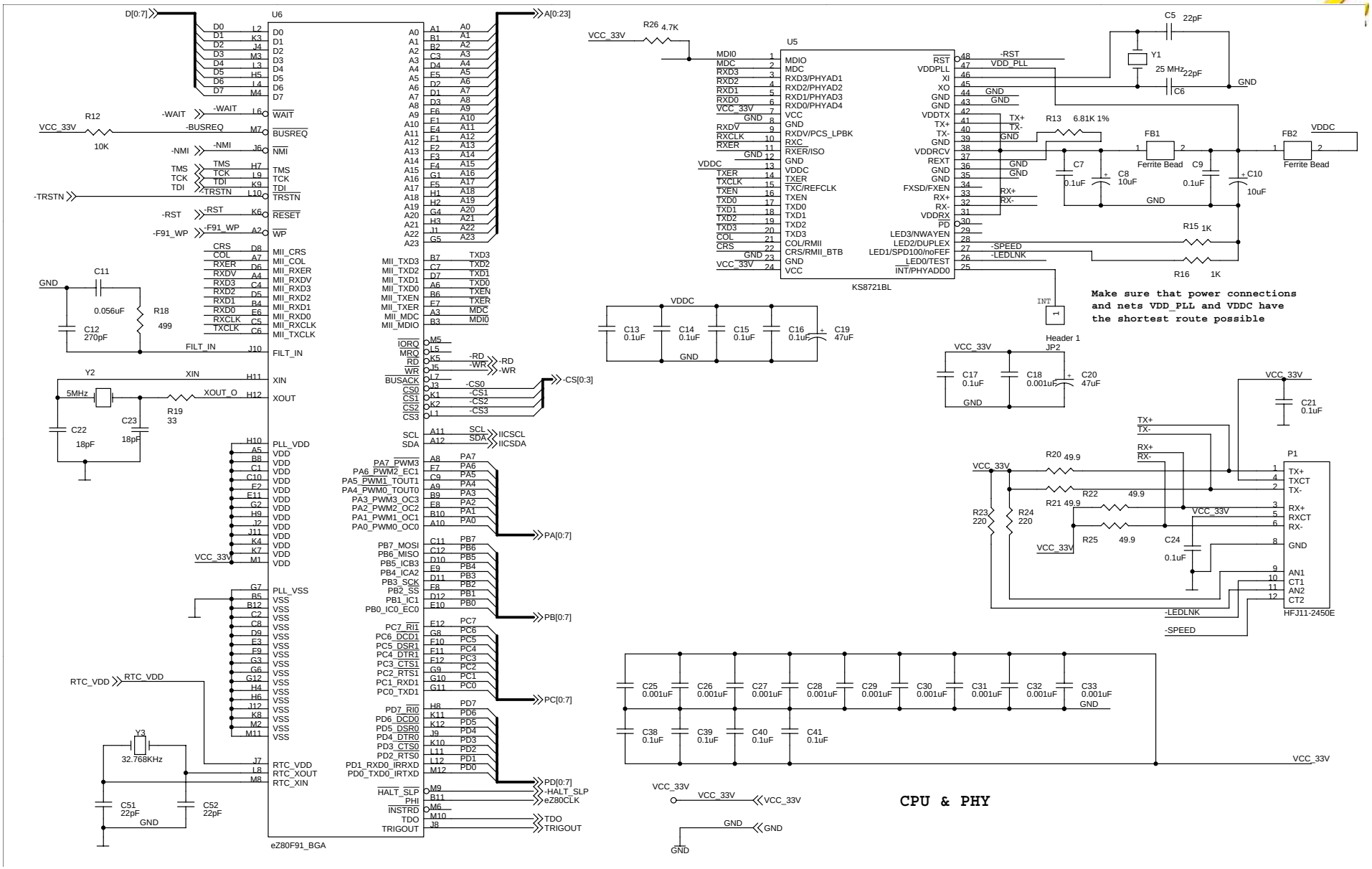

Figure 11. eZ80F91 Mini Enet Module Schematic (2 of 2)

Customer Feedback Form

If you note any inaccuracies while reading this User Manual, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

eZ80F91 Modular Development Kit
Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.