AN3319
Application note

STEVAL-ISV006V2: solar battery charger using the SPV1040

Introduction

The SPV1040 is a high efficiency, low power and low voltage DC-DC converter that provides a single output voltage up to 5.2 V. Startup is guaranteed at 0.3 V and the device operates down to 0.45 V when coming out from MPPT mode. It is a 100 kHz fixed frequency PWM step-up (or boost) converter able to maximize the energy generated by few solar cells (polycrystalline or amorphous). The duty cycle is controlled by an embedded unit running an MPPT algorithm with the goal of maximizing the power generated from the panel by continuously tracking its output voltage and current.

The SPV1040 guarantees the safety of overall application and of converter itself by stopping the PWM switching in the case of an overcurrent or overtemperature condition.

The IC integrates a 120 mΩ N-channel MOSFET power switch and a 140 mΩ P-channel MOSFET synchronous rectifier.

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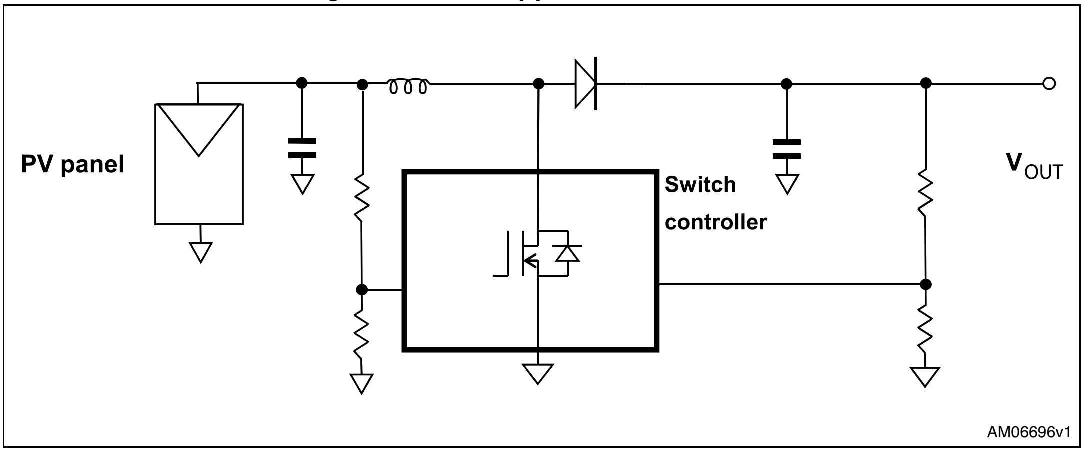
1 Application overview

Figure 1 shows the typical architecture of a boost converter based solar battery charger:

Figure 1. Boost application schematic

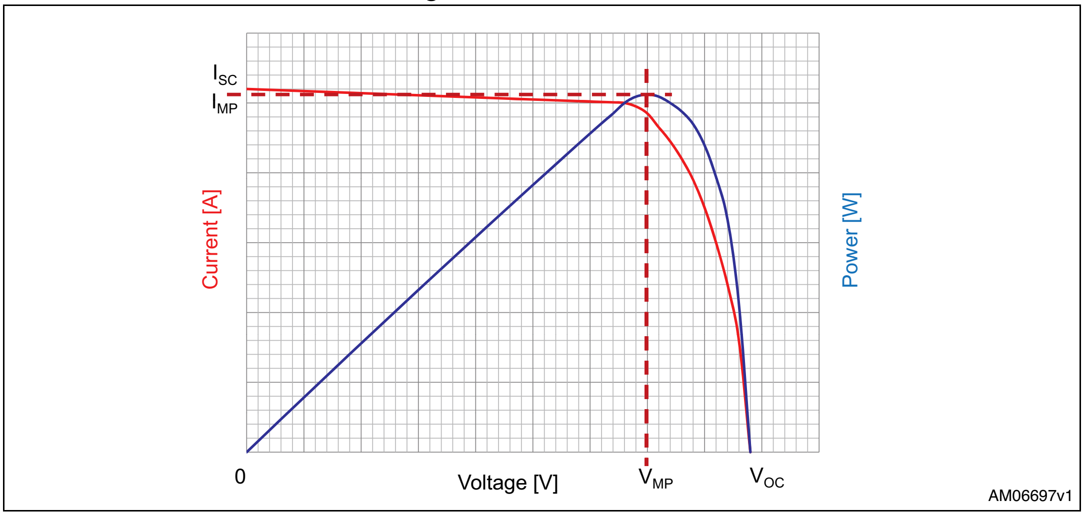


The SPV1040 adapts the characteristics of load to those of panel. In fact, a PV panel is made up of a series of PV cells. Each PV cell provides voltage and current which depend on the PV cell size, on its technology, and on the light irradiation power. The main electrical parameters of a PV panel (typically provided at light irradiation of 1000 W/m^2, T_{amb}=25 °C) are:

- V_{OC} (open circuit voltage)
- V_{MP} (voltage at maximum power point)
- I_{SC} (short-circuit current)
- I_{MP} (current at maximum power point)

Figure 2 shows the typical characteristics of a PV cell:

Figure 2. PV cell curve



MPP (maximum power point) is the working point of the PV cell at which the product of the extracted voltage and current provides the maximum power.

2 Boost switching application

A step-up (or boost) converter is a switching DC-DC converter able to generate an output voltage higher than (or at least equal to) the input voltage.

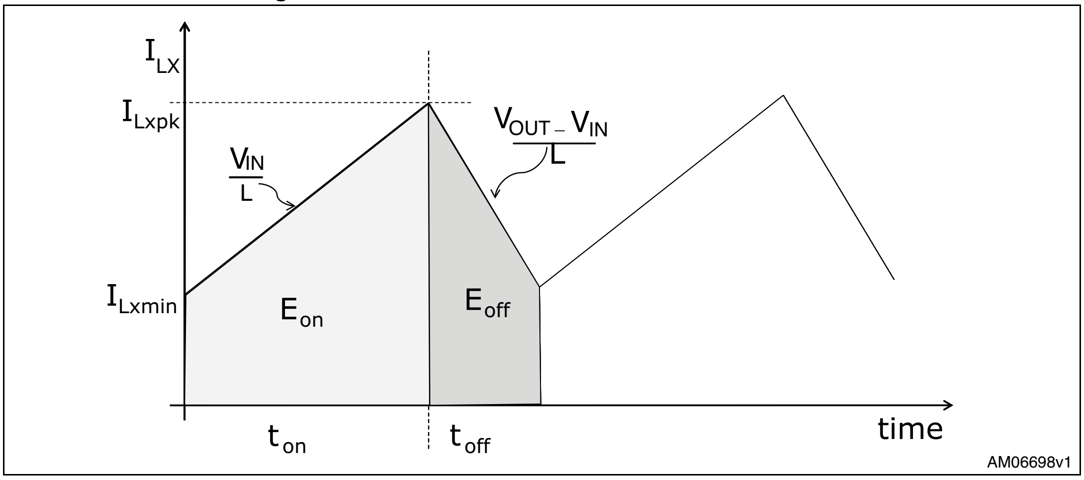
Referring to *Figure 1*, the switching element (S_w) is typically driven by a fixed frequency square waveform generated by a PWM controller.

When S_w is closed (t_{on}) the inductor stores energy and its current increases with a slope depending on the voltage across the inductor and its inductance value. During this time the output voltage is sustained by C_{OUT} and the diode does not allow any charge transfer from the output to input stage.

When S_w is open (t_{off}), the current in the inductor is forced, flowing toward the output until voltage at the input is higher than the output voltage. During this phase the current in the inductor decreases while the output voltage increases.

Figure 3 shows the behavior of inductor current.

Figure 3. Inductor current in continuous mode



The energy stored in the inductor during t_{on} is ideally equal to the energy released during t_{off}, therefore the relation between t_{on} and t_{off} can be written as follows:

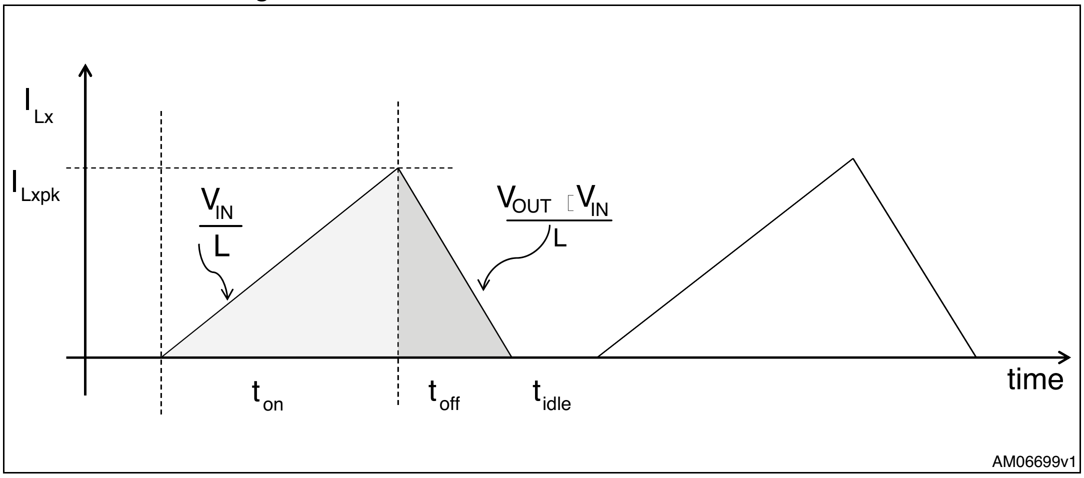
$$D = \frac{t_{on}}{(t_{on} + t_{off})}$$

where “D” is the duty cycle of the square waveform driving the switching element.

Boost applications can work in two different modes depending on the minimum inductor current within the switching period, that is if it is not null or null respectively:

- Continuous mode (CM)
- Discontinuous mode (DCM)

Figure 4. Inductor current in discontinuous mode



Obviously the efficiency is normally higher in CM.

Inductance and switching frequency (F_{sw}) impact the working mode. In fact, in order to have the system working in CM, the rule below should be followed:

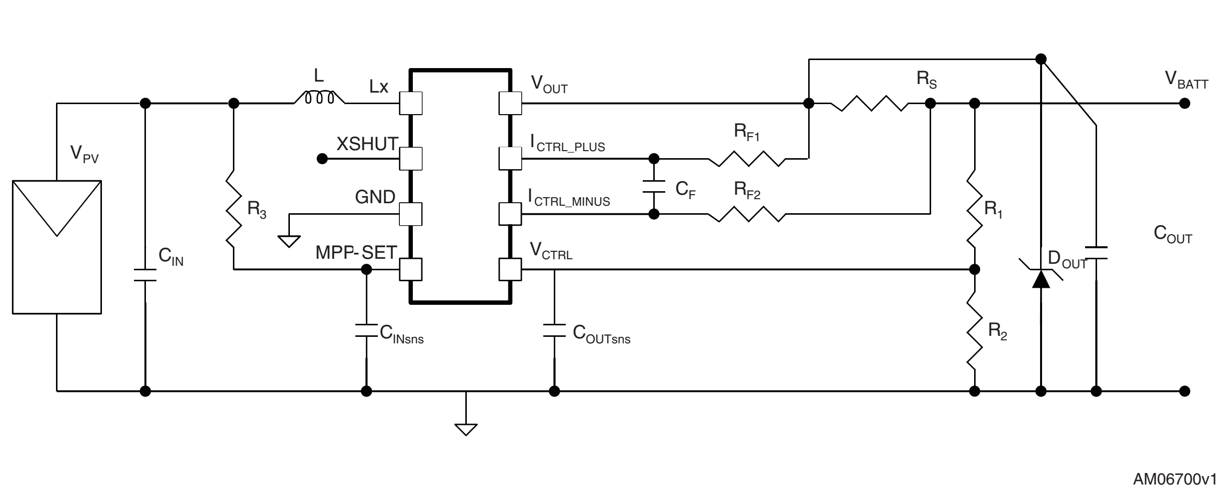
$$L > \frac{V_{OUT}^2}{P_{IN}} \cdot \frac{(D \cdot (1 - D))^2}{2 \cdot F_{SW}}$$

According to the above, L is minimum for D = 50 %.

3 SPV1040 description

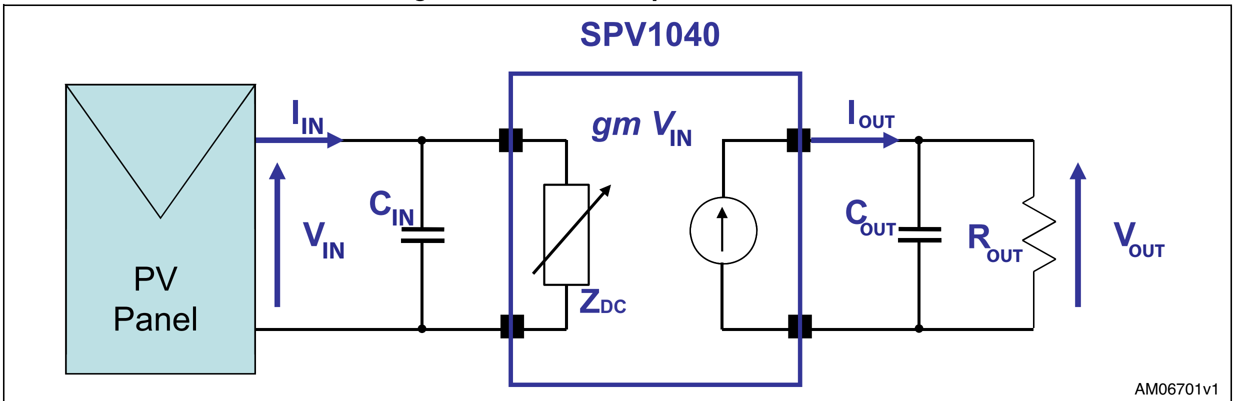
The following is a quick overview of SPV1040 functions, features, and operating modes.

Figure 5. Typical application schematic using the SPV1040



The SPV1040 acts as an impedance adapter between the input source and output load which is:

Figure 6. SPV1040 equivalent circuit



Through the MPPT algorithm, it sets up the DC working point properly by guaranteeing $Z_{IN} = Z_m$ (assuming Z_m is the impedance of the supply source). In this way, the power extracted from the supply source ($P_{IN} = V_{IN} * I_{IN}$) is maximum ($P_M = V_M * I_M$).

The voltage-current curve shows all the available working points of the PV panel at a given solar irradiation. The voltage-power curve is derived from the voltage-current curve by plotting the product V*I for each voltage generated.

Figure 7. MPPT working principle

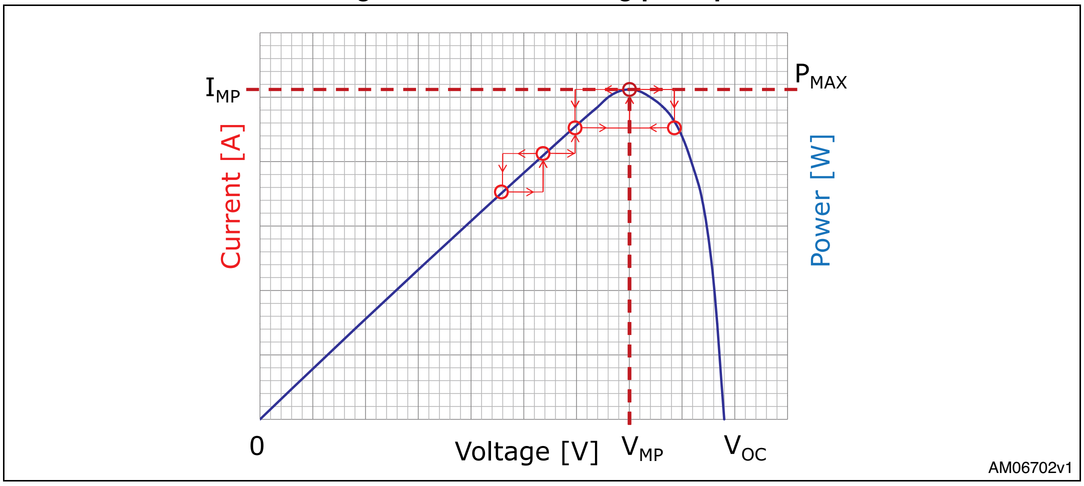
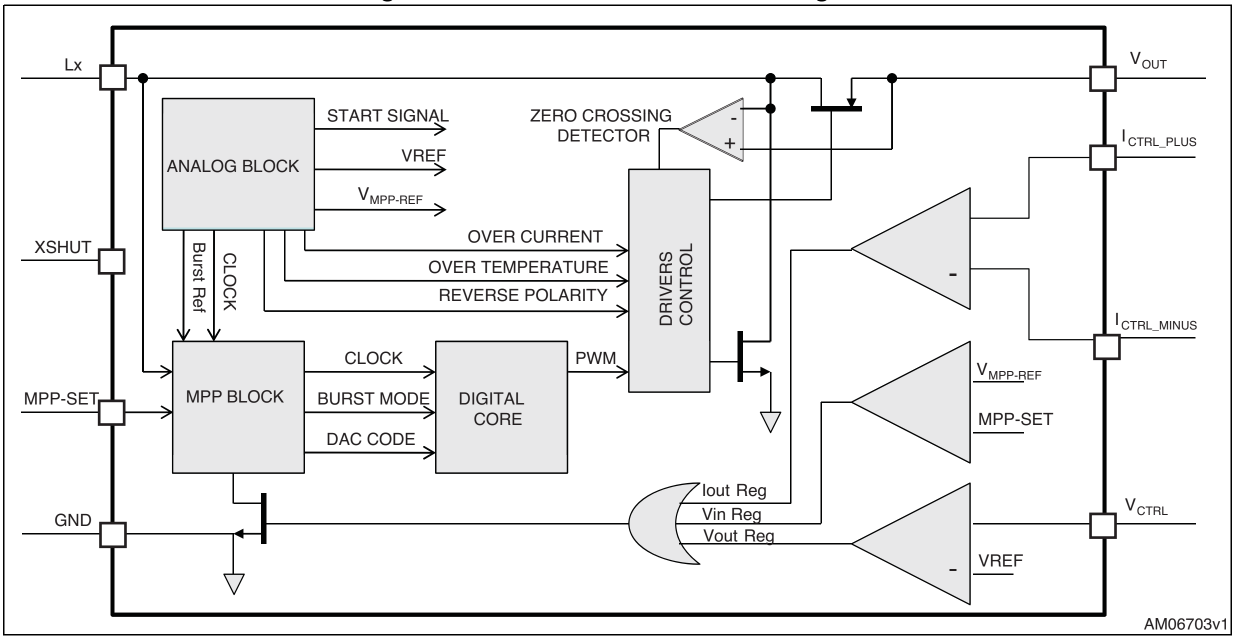


Figure 7 shows the logical sequence followed by the device which proceeds for successive approximations in the search for the MPP. This method is called “Perturb and Observe”. The diagram shows that a comparison is made between the digital value of the power Pn generated by the solar cells and sampled at instant n, and the value acquired at the previous sampling period Pn-1. This allows the MPPT algorithm to determine the sign of duty cycle and to increment or decrement it by a predefined amount. In particular, the direction of adjustment (increment or decrement of duty cycle) remains unchanged until condition Pn≥Pn-1 occurs, that is, for as long as it registers an increase of the instantaneous power extracted from the cells string. On the contrary, when it registers a decrease of the power Pn<Pn-1, the sign of duty cycle adjustment is inverted.

In the meantime, SPV1040 sets its own duty cycle according to the MPPT algorithm, other controls are simultaneously executed in order to guarantee complete application safety. These controls are mainly implemented by integrated voltage comparators whose thresholds are properly set.

Figure 8. SPV1040 internal block diagram



The duty cycle set by the MPPT algorithm can be overwritten if one of the following is triggered:

- Overcurrent protection (OVC), peak current on low side switch ≥ 1.8 A
- Overtemperature protection (OVT), internal temperature ≥ 155 °C
- Output voltage regulation, V_{CTRL} pin triggers 1.25 V
- Output current regulation R_s * (I_{CTRL_PLUS} - I_{CTRL_MINUS}) ≥ 50 mV
- MPP-SET voltage $V_{MPP\text{-}SET}$ ≤ 300 mV at the start-up and $V_{MPP\text{-}SET}$ ≤ 450 mV in working mode.

Application components must be carefully selected to avoid any undesired trigger of the above thresholds.

In order to improve the overall system efficiency, and to reduce the BOM, the SPV1040 also integrates a zero crossing block whose role is to turn-off the synchronous rectifier to prevent reverse current flowing from output to input.

4 Application example

Figure 9 and *10* show the demonstration board of a solar battery charger based on SPV1040 and on a status of charge indication circuit.

Figure 9. STEVAL-ISV006V2 top view

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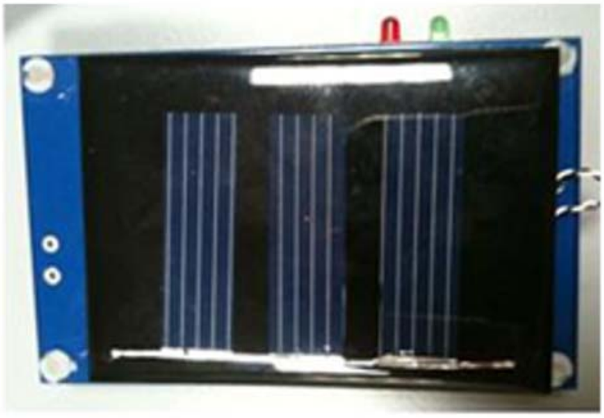
Figure 10. STEVAL-ISV006V2 bottom view



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STEVAL-ISV006V2 has been designed to recharge any type of battery (except lithium compound) which maximum voltage (V_{BATT_max}) ≤ 5.2 V and supplied by up to 5 W PV panels (constrained by $V_{OC}<V_{BATT\_max}$).

By default STEVAL-ISV006V2 is set as follows:

- Loaded by a 220 mF super capacitor
- Supplied by a 200 mW PV panel (V_{OC} = 1.65 V, I_{SC} = 150 mA)
- Maximum output current 1 A

The output trimmer VR_2 allow regulating V_{CTRL} across battery.

Maximum output current can be regulated by replacing R_s current sensing resistor according to application requirements.

Please refer to *Section 6*: external component selection for details about the whole application set-up.

Further, STEVAL-ISV006V2 provides a simple charge status circuit with 2 LEDs:

- Red LED on and green LED off, if the battery voltage is lower than charge threshold
- Red LED off and green LED on, if the battery voltage is higher than charge threshold

Charge threshold can be regulated by trimmer VR_{10}. Charge status circuit can be bypassed by opening jumper J1.

5 Schematic and bill of material

Figure 11. STEVAL-ISV006V2 schematic

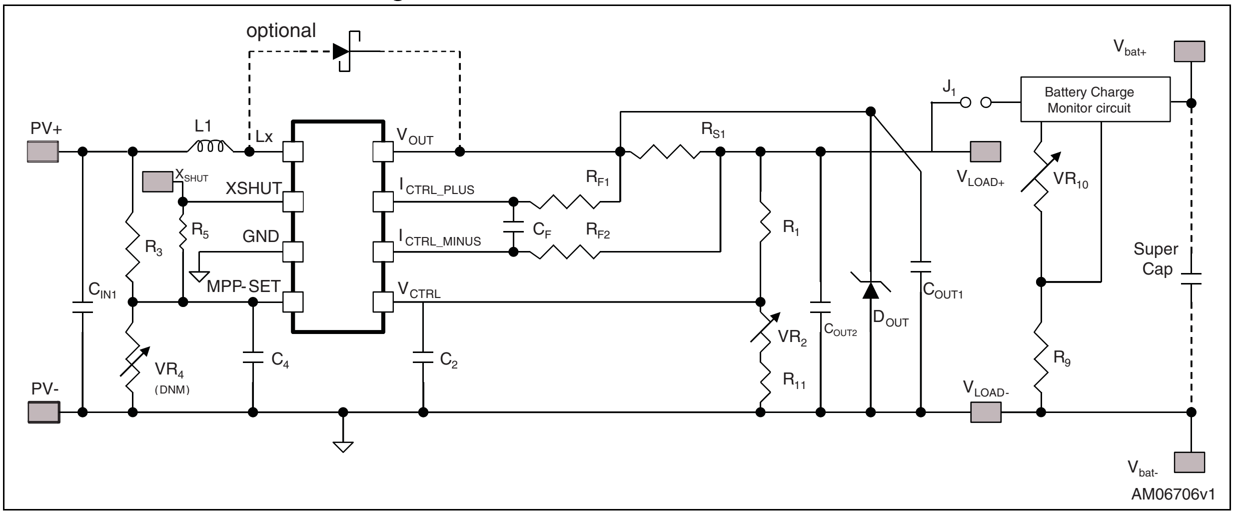


Table 1 shows the list of external components used in the demonstration board.

Table 1. BOM

Component (alternate label)	Name	Value	Supplier	Serial number
U25/26	Solar battery charger		STMicroelectronics	SPV1040T
PV panel	Poly-crystalline PV panel	200 mW	NBSZGD	SZGD7050-3P
CIN1	Input capacitor	10 μF	EPCOS	C2012X5R1A106K
C4	Voltage sensing capacitor	100 nF	EPCOS	C2012X5R1H104K
C2	Voltage sensing capacitor	1 nF	EPCOS	C2012C0G1H102J
COUT1	Output capacitor	4.7 μF	EPCOS	C2012X5R0J475K
COUT2	Output capacitor	10 μF	EPCOS	C2012X5R1A106K
R3	Input voltage partitioning resistor	1 kΩ	Cyntec	RG2012P1001BN
VR2, VR10 VR4 (DNM)	OUT, MPP-SET and charge indication partitioning resistor	0-1 MkΩ	VISHAY	63M-105
R1	Output voltage partitioning resistor	1 MΩ	Cyntec	RG2012P105BN
R11	Output voltage partitioning resistor	330 kΩ	Cyntec	RG2012P334BN
R5	Pull-up resistor	0	Cyntec	RL1220TR010FN

Table 1. BOM (continued)

Component (alternate label)	Name	Value	Supplier	Serial number
L1	Inductor	10 μH	Coilcraft Coilcraft EPCOS	XAL6060-103 MSS7341-103 B82442T1103K050
J28	Super capacitor	220 nF	Panasonic	EECS0HD224H
Dout1	Protection diode		STMicroelectronics	SMM4F5.0
RS1	Output current sense	10 mΩ	Cyntec	RL1220TR000FN
RF1, RF2	Noise filterirng resistors	1 kΩ	Cyntec	RG2012P1001BN
CF1	Noise filtering capacitor	1 μF	EPCOS	C2012X7R1C105K
U27	QUAD comparator		STMicroelectronics	TS339
D1	Green LED	1.8 V, 2 mA	Avago Tech.	HLMP-1790
D4	Red LED	1.8 V, 2 mA	Avago Tech.	HLMP-1700
D5	Reference diode		STMicroelectronics	STPS160U
R6, R7	LED protection resistors	1 kΩ	Cyntec	RG2012P1001BN
R8	Reference resistors	1 MΩ	Cyntec	RG2012P105BN
R9	Charge status threshold resistors	27 kΩ	Cyntec	RG2012P2701BN

6 External component selection

SPV1040 requires a set of external components and their proper selection guarantees both the best chip functionality and system efficiency.

Input voltage capacitor

C_{IN} is the input capacitor connected to the input rail in order to reduce the voltage ripple.

According to the maximum current (I_{SC}) provided by the PV panel connected at the input, the following formula should be considered to select the proper capacitance value for a specified maximum input voltage ripple ($V_{IN\_rp\_max}$):

$$C_{IN} \geq \frac{I_{SC}}{F_{SW} \cdot V_{IN\_rp\_max}}$$

Maximum voltage of this capacitor is strictly dependent on the input source (typically between 1 V and 3 V).

Low-ESR capacitors are a good choice to increase the whole system efficiency. In order to reduce the ESR effect, it is suggested to split the input capacitance into two capacitors placed in parallel.

Input voltage partitioning

$V_{MPP-SET}$ is the pin used to monitor the voltage generated by the solar cells.

The $V_{MPP-SET}$ pin can be directly connected to PV+ rail through a 1 kΩ R_3 resistor.

With regard to the $V_{MPP-SET}$ pin, two constraints must be taken into account:

- When SPV1040 is off, $V_{MPP-SET}$ voltage must be ≥0.3 to turn-on the device
- When SPV1040 is in operating mode, it enters BURST MODE if $V_{MPP-SET}$ decreases triggering the 450 mV threshold.

Input voltage sensing capacitor

C_4 is placed as close as possible to the $V_{MPP-SET}$ pin to reject noise on $V_{MPP-SET}$ voltage.

However, $V_{MPP-SET}$ must be able to follow the V_{IN} waveform to allow SPV1040 to monitor input voltage variations.

It means that the time constant R_3*C_4 must be chosen according to system properties, which is the MPPT tracking time ($T_{MPP} \cong 1$ ms). The rule below must be followed in order to select C_4 capacitance:

$$C_4 \leq T_{MPP} \cdot \frac{1}{R_3} = 10^{-3} \cdot \frac{1}{10^3}$$

Assuming R_3= 1 kΩ then: $C_4 \leq 10\mu F$

Inductor selection

Inductor selection is a crucial point for this application. The following application constraints must be taken into account:

- Maximum input current (i.e. I_{MP} and I_{SC} of PV panel)
- Maximum input voltage (i.e. V_{MP} and Voc of PV panel)
- Overcurrent threshold of SPV1040 (1.8 A)
- Maximum duty cycle of SPV1040 (90 %).

The input current from the PV panel flows into the inductor, so:

$$I_{Lxrms} \cong I_{MP} < I_{SC}$$

According to *Figure 3*, during the charge phase (switch on), peak current on the inductor depends on the applied voltage (V_{IN}) on the inductance (L_x), and on the duty cycle (t_{on}).

Considering the maximum duty cycle (90 %):

$$I_{LXpeak} = I_{LXrms} + \frac{9 \cdot 10^{-6} V_{MP}}{2L_x}$$

Taking into account the overcurrent threshold:

$$I_{LXpeak} < 1.8A$$

Finally, inductance should be chosen according to the following formula:

$$L_X > \frac{1}{2} \cdot \frac{9 \cdot 10^{-6} V_{MP}}{2 - I_{LXrms}} = \frac{1}{2} \cdot \frac{9 \cdot 10^{-6} V_{MP}}{2 - I_{MP}}$$

A safer choice is to replace V_{MP} with V_{OC}.

Usually, inductances ranging between 10 μH to 100 μH satisfy most application requirements.

Other critical parameters for the inductor choice are Irms, saturation current, and size.

Irms is the self rising temperature of the inductor, affecting the nominal inductance value. In particular, the inductance decreases with Irms and the temperature increases. As a consequence the inductor current peak can reach or surpass 1.8 A.

Inductor size also affects the maximum current deliverable to the load. In any case, the saturation current of the choke should be higher than the peak current limit of the input source. Hence, the suggested saturation current must be > 1.8 A.

At the same size, small inductance values guarantee both faster response to load transients and higher efficiency.

Inductors with low series resistance are suggested in order to guarantee high efficiency.

Output voltage capacitor

A minimum output capacitance must be added at the output in order to reduce the voltage ripple.

Critical parameters for capacitors are: capacitance, maximum voltage, and ESR.

According to the maximum current (I_{SC}) provided by the PV panel connected at the input, the following formula can be used to select the proper capacitance value (C_{OUT}) for a specified maximum output voltage ripple ($V_{OUT\_rp\_max}$):

$$C_{OUT} \geq \frac{I_{SC}}{F_{SW} \cdot V_{OUT\_rp\_max}}$$

Maximum voltage of this capacitor is strictly dependent on the output voltage range. SPV1040 can support up to 5.2 V, so the suggested maximum voltage for these capacitors is 10 V.

Low-ESR capacitors are a good choice to increase the whole system efficiency.

Output voltage partitioning

R_1 and R_2 are the two resistors used for partitioning the output voltage.

The said V_{OUT_max} the maximum output voltage of the battery, R_1 and R_2 must be selected according to the following rule:

$$\frac{R_1}{R_2} = \frac{V_{OUT\_max}}{1.25} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R_1 and R_2, their power dissipation must be taken into account.

Assuming a negligible current flowing into the V_{CTRL} pin, maximum power dissipation on the series R_1+R_2 is:

$$P_{VCTRL\_sns} = \frac{(V_{OUTmax})^2}{R_1 + R_2}$$

As an empirical rule, R_1 and R_2 should be selected to get:

$$P_{VCTRL\_sns} \ll 0.01 \cdot (V_{OUT\_max} \cdot I_{OUT\_max})$$

Note: In order to guarantee proper functionality of the V_{CTRL} pin, the current flowing into the series R_1+R_2 should be in the range between 2 µA and 20 µA.

Output voltage sensing capacitor

C_2 is placed in parallel to R_2 and as close as possible to the V_{CTRL} pin.

Its role is to reject the noise on the voltage sensed by the V_{CTRL} pin.

Capacitance value depends on the time constant resulting from R_2 (τ_{OUT}= C_2*R_1//R_2) and from the system switching frequency (100 kHz), as follows:

$$\tau_{out} \cong 10 * \frac{1}{F_{ssw}}$$

$$C_2 \cong 10 * \frac{1}{F_{ssw}} * \frac{1}{R_1 // R_2}$$

Output current sensing filter

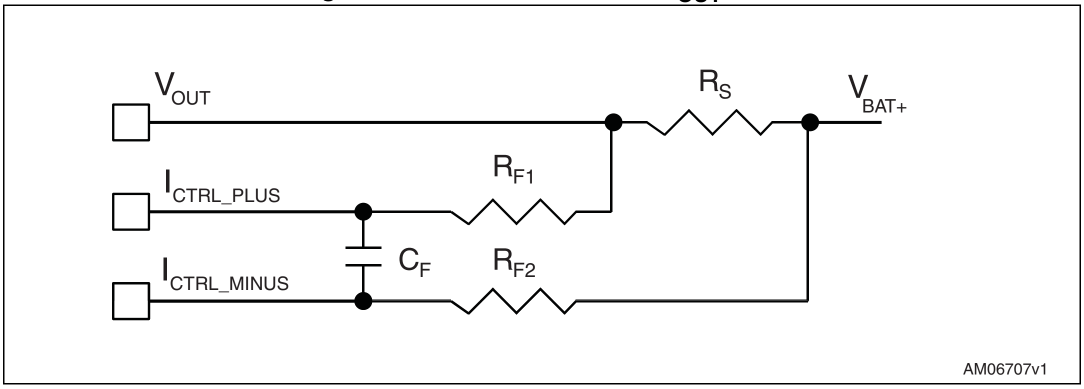
R_s is placed in the output rail between the I_{CTRL_MINUS} and I_{CTRL_PLUS} pins.

Its role is to sense the output current (I_{OUT}) flowing toward the load. Voltage drop on R_s is sensed by the I_{CTRL_MINUS} and I_{CTRL_PLUS} pins and compared with the 50 mV internal threshold.

$$R_S \cong \frac{50mV}{I_{OUT\_max}}$$

The triangular waveform of the current and noise may cause unexpected triggering of the 50 mV threshold. This can be avoided with a filter such as the one shown below:

Figure 12. STEVAL-ISV006V2 I_{OUT} filter



Suggested values are:

R_{F1}=R_{F2} = 1 kΩ

C_F = 1 μF

Output protection diode

If the load is not a battery, D_{OUT} is required and placed in parallel to the output load. Its role is to protect the devices in case a PV cell providing I_{MP} > 0.5 A is connected when very low load is connected.

In fact, SPV1040 is supplied by the V_{OUT} pin, so in the above condition the device is still off when the PV cell is connected and a voltage spike can occur damaging the converter and the battery.

In order to guarantee the best system performance and reliability, D_{OUT} should be selected as follows:

$V_{BR} > V_{OUT\_max}$

$V_{CL} \leq 5.5$ V

D_{OUT} must be able to dissipate the following maximum power:

$P_{max} = I_{SC} {}^* V_{CL}$

XSHUT resistor

The XSHUT pin controls SPV1040 turn-on (0.3 V ≤ XSHUT ≤ 5.2 V) or turn-off (XSHUT < 0.3 V).

R_5 is a 0 Ω pull-up resistor shorting the XSHUT and MPP-SET pins.

Removing R5 enables the external control of the XSHUT pin to turn the SPV1040 on/off.

6.1 Optional Schottky

An external Schottky diode between L_x and V_{OUT} pins is mandatory in all the applications with $V_{BATT\_max} > 4.8$ V.

In fact, voltage on L_x pin can go above the maximum absolute voltage threshold (5.5 V) due to the voltage drop on the high side integrated switch when this is off (discontinuous mode) and current needs to flow from input to output.

This Schottky diode should be chosen according to the following criteria:

$$V_F \leq 5.5V - V_{BATT\_max} \text{ and } I_F \geq I_{Lmax}$$

For setting up the application and simulating the related test results please go to www.st.com/edesignstudio.

7 Layout

Figure 13. STEVAL-ISV006V2 PCB top view

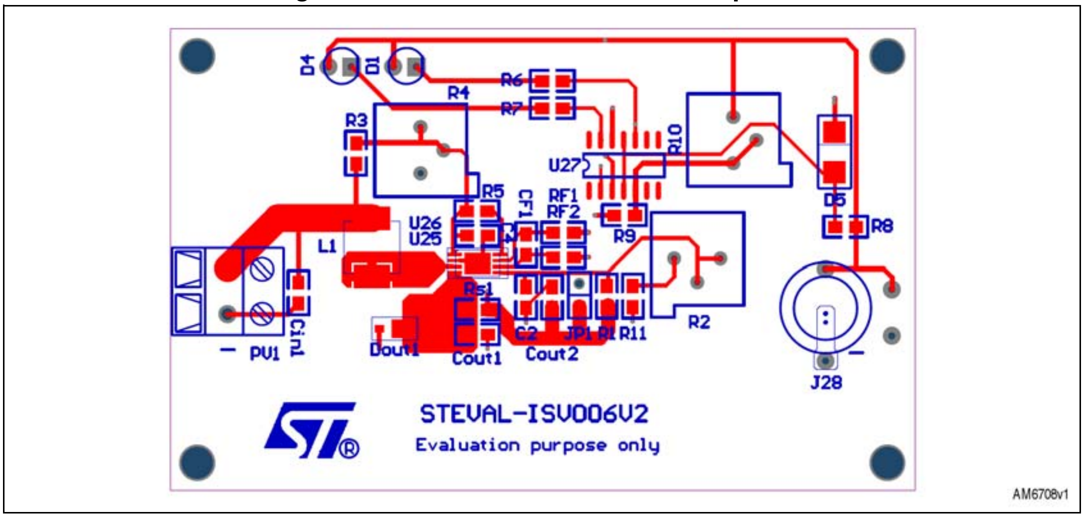
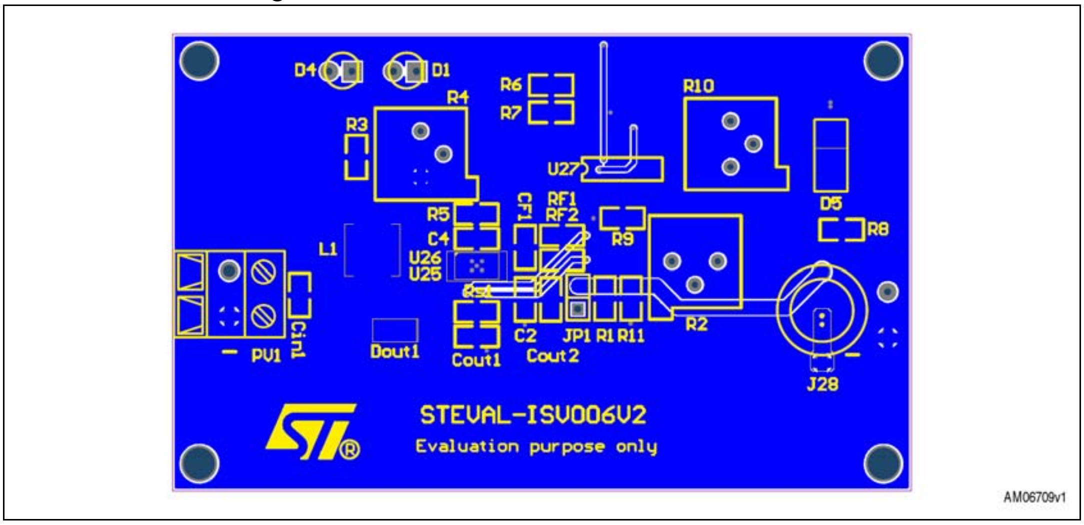


Figure 14. STEVAL-ISV006V2 PCB bottom view



Layout guidelines

PCB layout is very important in order to minimize voltage and current ripple, high frequency resonance problems, and electromagnetic interference. It is essential to keep the paths where the high switching current circulates as small as possible in order to reduce radiation and resonance problems.

Large traces for high current paths and an extended ground plane reduce noise and increase efficiency.

The output and input capacitors should be placed as close as possible to the device.

The external resistor dividers, if used, should be as close as possible to the $V_{MPP\text{-}SET}$ and V_{CTRL} pins of the device, and as far as possible from the high current circulating paths, in order to avoid picking up noise.

Appendix A SPV1040 parallel and series connection

Output pins of many SPV1040s can be connected either in parallel or in series. In both cases the output power (Pout) depends on light irradiation of each panel, on application efficiency, and on the specific constraints of the selected topology.

The objective of this section is to explain how the output power is impacted by the selected topology.

An example with 3 PV panels (panel1, panel2, panel3) is presented, but the conclusion can be extended to a larger number of PV panels.

If the panel is lighted and the SPV1040 is on (it means that light irradiation intensity is such that $V_{MPP\text{-}SET} \geq 0.3$ V):

$$P_{OUTx} = \eta P_{INx} \quad [x = 1..3]$$

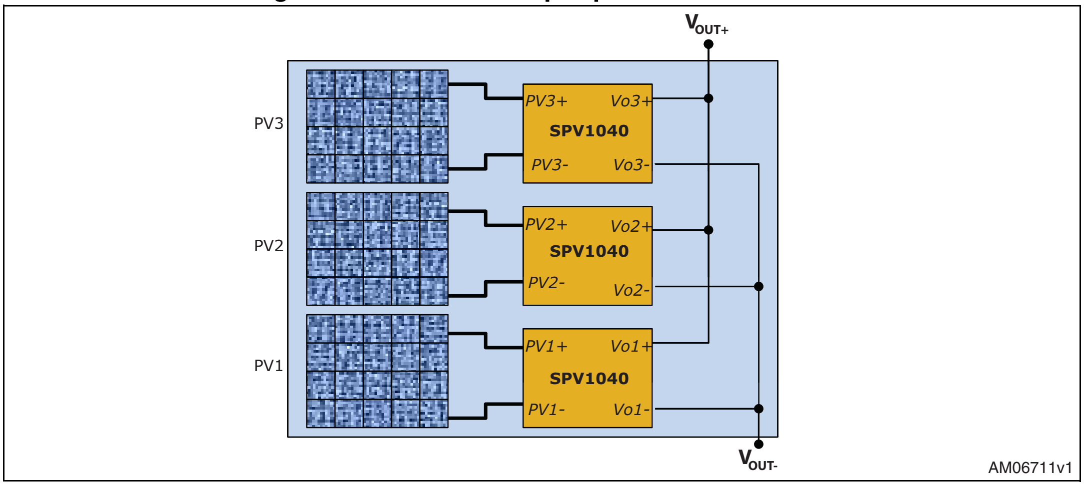
If the panel is completely shaded: $P_{OUTx}=0$

SPV1040 parallel connection

This topology guarantees the desired output voltage even when only one panel is irradiated. The obvious constraint of this topology is that V_{OUT} is limited to the SPV1040 maximum output voltage.

Figure 15 shows the parallel connection topology:

Figure 15. SPV1040 output parallel connection



The output partitioning (R_1/R_2) of each SPV1040 must be coherent with the desired V_{OUTX}.

According to the topology:

$V_{OUT}=V_{OUT1}=V_{OUT2}=V_{OUT3}$

$I_{OUT}=I_{OUT1}+I_{OUT2}+I_{OUT3}$

According to the light irradiation on each panel and to the system efficiency (η), the output power results:

$$P_{OUT} = P_{OUT1} + P_{OUT2} + P_{OUT3}$$
$$P_{OUTx} = V_{OUTx} * I_{OUTx} \qquad [x = 1..3]$$
$$P_{INx} = V_{INx} * I_{INx} \qquad [x = 1..3]$$

Therefore:

$$P_{OUT} = V_{OUT}(I_{OUT1} + I_{OUT2} + I_{OUT3}) = \eta P_{IN1} + \eta P_{IN2} + \eta P_{IN3}$$

Each SPV1040 contributes to the output power providing I_{OUTX}.

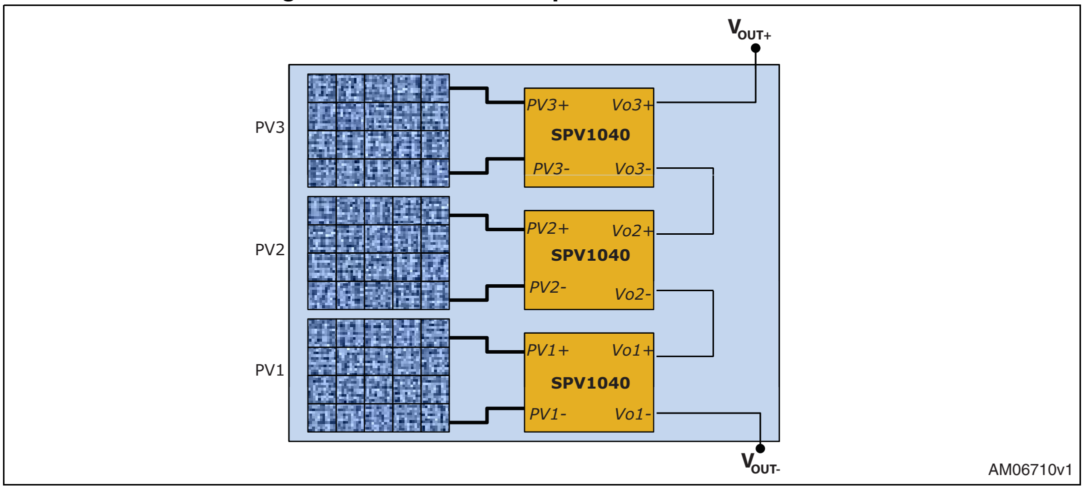
Finally, the desired V_{OUT} is guaranteed if at least one of the 3 PV panels provides enough power to turn-on the SPV1040 relating to it.

SPV1040 series connection

This topology provides an output voltage that is the sum of the output voltages of the SPV1040 connected in series. The objective of this section is to explain how the output power is impacted by the selected topology.

Figure 16 shows the series connection topology:

Figure 16. SPV1040 output series connection



In this case, the topology imposes:

$$I_{OUT} = I_{OUT1} = I_{OUT2} = I_{OUT3}$$
$$V_{OUT} = V_{OUT1} + V_{OUT2} + V_{OUT3}$$

In case irradiation is the same for each panel:

$$P_{OUT1} = P_{OUT2} = P_{OUT3}$$
$$P_{OUT} = 3 * P_{OUTx} \qquad [x = 1..3]$$
$$P_{OUTx} = \frac{1}{3} P_{OUT}$$
$$P_{OUTx} = V_{OUTx} * I_{OUTx} = V_{OUT1} * I_{OUT}$$

Therefore:

$$V_{OUTx} = \frac{1}{3} V_{OUT}$$

For example, assuming P_{OUT} = 3 W and V_{OUT} = 12 V, then

V_{OUTx} = 4 V.

Lower irradiation for one panel, for example on panel 2, causes lower output power, so lower V_{OUT2} due to the I_{OUT} imposed by the topology:

$$V_{OUTx} = \frac{P_{OUTx}}{I_{OUT}}$$

The output voltage required by the load can be provided by the 1st and the 3rd SPV1040 but only up to the limit imposed by each of their R_1/R_2 partitionings.

Some examples can help in understanding the various scenarios assuming that each R_1/R_2 limits V_{OUTx} to 4.8 V.

Example 1:

Panel 2 has 75 % irradiation of panels 1 and 3:

$$V_{OUT2} = \frac{3}{4} * V_{OUT1} = \frac{3}{4} * V_{OUT3}$$

$$P_{OUT1} = P_{OUT3} = 1W$$

$$P_{OUT2} = \frac{3}{4} P_{OUT1} = 0.75W$$

$$P_{OUT} = P_{OUT1} + P_{OUT2} + P_{OUT3} = 2.75W$$

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{2.75}{12} = 0.23A$$

$$V_{OUT1} = V_{OUT3} = \frac{1}{0.23} = 4.35V$$

$$V_{OUT2} = \frac{0.75}{0.23} = 3.26V$$

Two SPV1040s (1st and 3rd) supply the voltage drop caused by the lower irradiation on panel 2.

Warning: **SPV1040 is a boost controller, so V_{OUTx} must be higher than V_{INx}, otherwise the SPV1040 turns off and the input power is transferred to the output stage through the integrated P-channel MOS without entering the switching mode.**

Example 2:

Panel 2 has 50 % irradiation of panels 1 and 3:

$$P_{OUT2} = \frac{1}{2} \cdot P_{OUT1} = \frac{1}{2} \cdot P_{OUT3}$$

$$P_{OUT1} = P_{OUT3} = 1W$$

$$P_{OUT2} = \frac{1}{2} P_{OUT1} = 0.5W$$

$$P_{OUT} = P_{OUT1} + P_{OUT2} + P_{OUT3} = 2.5W$$

$$I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{2.5}{12} = 0.21A$$

$$V_{OUT1} = V_{OUT3} = \frac{1}{0.21} = 4.76V$$

$$V_{OUT2} = \frac{0.5}{0.21} = 2.38V$$

In this case the system is close to its maximum voltage limit, in fact, a lower irradiation on panel 2 impacts V_{OUT1} and/or V_{OUT3} which are very close to the maximum output voltage threshold (4.8 V) imposed by R_1/R_2 partitioning.

Example 3:

Panel 2 completely shaded.

In this case the maximum V_{OUT} can be 9.6 V ($V_{OUT1}+V_{OUT3}$).

The current flow is guaranteed by the body diodes of the power MOSFETs integrated in the SPV1040 (or by the bypass diodes, if any, placed between V_{OUT-} and V_{OUT+}).

Revision history

Table 2. Document revision history

Date	Revision	Changes
02-Feb-2011	1	Initial release
18-Apr-2011	2	– Demonstration board changed: from STEVAL-ISV006V1 to STEVAL-ISV006V2 – *Figure 9*, *10*, *11*, *13* and *14* modified – *Section 4* modified – *Table 1* modified
04-May-2011	3	Modified: *Table 1*
08-Sep-2011	4	– Modified: *Section 3* and *4* – Changed: *Table 1: BOM* – Changed: *Figure 5*, *8*, *9* and *11* – Modified: *Input voltage partitioning*, *Input voltage sensing capacitor*
12-Sep-2011	5	Minor text changes
21-Sep-2011	6	– Modified: *Figure 5*, *8* and *11* – Modified: text and equation for *Input voltage sensing capacitor* in *Section 6: External component selection*
18-Nov-2011	7	Modified: value of the component RS1 in *Table 1*
21-Mar-2013	8	Updated *Figure 8*.