ZL30163
Network Synchronization Clock Translator
Short Form Data Sheet

May 2013

Features

- Fully compliant SEC (G.813) and EEC (G.8262) flexible rate conversion digital phase locked loop (DPLL)
- Two programmable DPLLs/Numerically Controlled Oscillators (NCOs) synchronize to any clock rate from 1 Hz to 750 MHz
- Four programmable synthesizers generate any clock rate from 1 Hz to 750 MHz with maximum jitter below 0.62 ps RMS
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- DPLLs filter jitter from 0.1 mHz up to 1 kHz
- Automatic hitless reference switching and digital holdover on reference fail
- Nine input references configurable as single ended or differential and two single ended input references
- Any input reference can be fed with sync (frame pulse) or clock

Ordering Information

ZL30163GDG2 144 Pin LBGA Trays

Pb Free Tin/Silver/Copper
-40°C to +85°C
Package Size: 13 x 13 mm

- Programmable DPLLs can synchronize to sync pulse and sync pulse/clock pair
- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Field programmable via the SPI/I^2C interface

Applications

- SyncE/SONET/SDH Timing Cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI

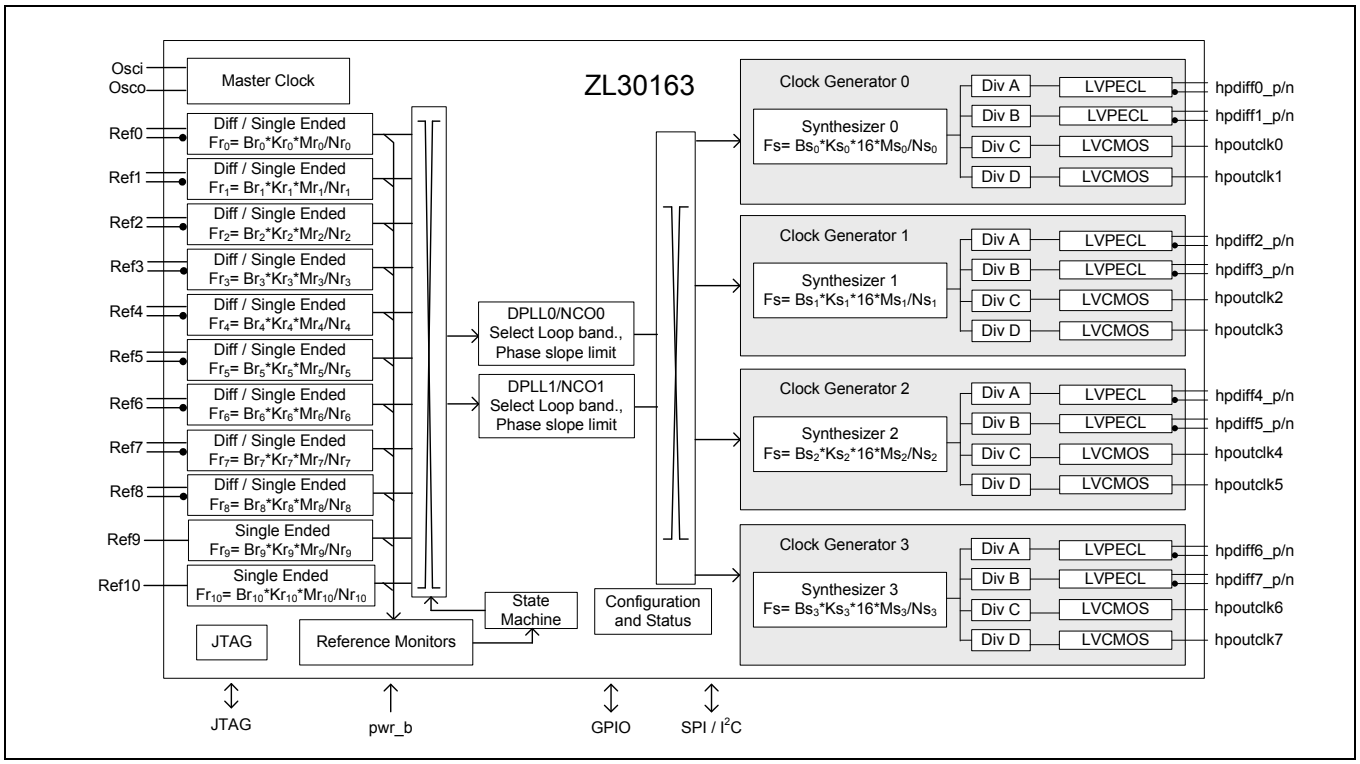


Figure 1 - Functional Block Diagram

1.0 Pin Diagram

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12
A	hpdiff0_p	VDD0	NC	VDD1	osco_1V8	VDD2	osco_3V3	osci_3V3	VDD3	NC	VDD4	hpdiff2_p
B	hpdiff0_n	VSS	NC	VSS	osci_1V8	VSS	XOin	VCORE0	VSS	NC	VSS	hpdiff2_n
C	hpdiff1_p	hpdiff1_n	VDD5	VSS	VSS	VCORE1	VSS	VSS	VSS	VDD6	hpdiff3_n	hpdiff3_p
D	VDD7	VSS	hpoutclk0	hpoutclk1	VSS	VSS	VSS	VSS	hpoutclk3	hpoutclk2	VSS	VDD8
E	NC	VDD9	VDD10	VSS	VSS	VSS	VSS	VSS	VSS	VDD11	IC1	NC
F	NC	trst_b	hpoutclk4	hpoutclk5	VSS	VSS	VSS	VSS	hpoutclk6	hpoutclk7	pwr_b	NC
G	tdi	tdo	tms	VSS	VSS	VSS	VSS	VSS	VDD12	gpio1	gpio0	IC2
H	hpdiff4_p	hpdiff4_n	tck	VSS	VSS	VSS	VSS	VSS	VCORE2	gpio2	hpdiff6_n	hpdiff6_p
J	VDD13	VSS	gpio4	VSS	VSS	VSS	VSS	VSS	VCORE3	gpio3	VSS	VDD14
K	hpdiff5_p	hpdiff5_n	gpio5	gpio6	VSS	VCORE4	cs_b_asel0	sck_scl	si_sda	so_asel1	hpdiff7_n	hpdiff7_p
L	VDD15	VSS	ref1_p	ref1_n	ref3_p	ref3_n	ref5_p	ref5_n	ref6_n	ref8_p	ref8_n	ref10
M	VCORE5	VSS	ref0_p	ref0_n	ref2_p	ref2_n	ref4_p	ref4_n	ref6_p	ref7_p	ref7_n	ref9

1 - A1 corner is identified by metallized markings.

Figure 2 - Package Description

2.0 Pin Description

All device inputs and outputs are LVCMOS unless it is specifically stated to be differential. For the I/O column, there are digital inputs (I), digital outputs (O), analog inputs (A-I) and analog outputs (A-O).

Ball #	Name	I/O	Description
Input Reference			
M3 M4 L3 L4 M5 M6 L5 L6 M7 M8 L7 L8 M9 L9 M10 M11 L10 L11	ref0_p ref0_n ref1_p ref1_n ref2_p ref2_n ref3_p ref3_n ref4_p ref4_n ref5_p ref5_n ref6_p ref6_n ref7_p ref7_n ref8_p ref8_n	I	**Input References 0 to 8.** Input reference sources used for synchronization. The positive and negative pair of these inputs accepts a differential input signal. The refx_p input terminal accepts a CMOS input reference. These inputs can be used as an external feedback input. Maximum frequency limit on single ended inputs is 177.5 MHz, and 750 MHz on differential inputs.
M12 L12	ref9 ref10	I	**Input References 9 and 10.** Input reference sources used for synchronization. These inputs are the same as inputs 0 to 8, but only single ended. These inputs can be used as an external feedback input. Maximum frequency limit is 177.5 MHz.
Output Clocks			
D3 D4 D10 D9 F3 F4 F9 F10	hpoutclk0 hpoutclk1 hpoutclk2 hpoutclk3 hpoutclk4 hpoutclk5 hpoutclk6 hpoutclk7	O	**High Performance Output Clocks 0 to 7.** These outputs can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz.

Table 1 - Pin Description

Ball #	Name	I/O	Description
A1 B1 C1 C2 A12 B12 C12 C11 H1 H2 K1 K2 H12 H11 K12 K11	hpdiff0_p hpdiff0_n hpdiff1_p hpdiff1_n hpdiff2_p hpdiff2_n hpdiff3_p hpdiff3_n hpdiff4_p hpdiff4_n hpdiff5_p hpdiff5_n hpdiff6_p hpdiff6_n hpdiff7_p hpdiff7_n	O	**High Performance Differential Output Clocks 0 to 7 (LVPECL).** These outputs can be configured to provide any one of the available high performance differential output clocks. Maximum frequency limit on differential outputs is 750 MHz.
Control and Status			
F11	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The **pwr_b** pin should be held low for 2 ms after all power supplies are stabilized. This pin is internally pulled-up to V_{DD}. User can access device registers either 125 ms after **pwr_b** goes high, or after bit 7 in register at address 0x000 goes high (which can be determined by polling).

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
G11 G10 H10 J10 J3 K3 K4	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose I/O pins. Example GPIO functions include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • Differential output clock enable • High performance LVCMOS outputs enable • Host Interrupt Output to flag status changes All GPIO functions are listed in 5.2, “GPIO Configuration“. Pins 5:0 are internally pulled down to GND and pin 6 is internally pulled up to V_{DD}. Unused GPIO pins can be left unconnected. After power on reset, device GPIO[0,1,3] configure basic device function. GPIO3 sets I^2C or SPI control mode, GPIO[1,0] sets master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1 kΩ resistor for their assigned functions at reset; or they must be driven low or high for 125 ms after reset, and released and then used for normal GPIO functions. The GPIO4 pin must be either pulled low with an external 1 kΩ resistor; or it must be driven low for 125 ms after reset, and then released and used for normal GPIO functions. GPIO[5,6] are not used during power up.
Host Interface			
K8	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I^2C mode. As an input this pin is internally pulled up to V_{DD}.
K9	si_sda	I/O	**Serial Interface Input.** The input serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when the host interface is configured for I^2C mode. This pin is internally pulled up to V_{DD}.
K10	so_asel1	I/O	**Serial Interface Output.** As an output, the serial stream holds the read data bits. This pin is also a part of the I^2C address select when the host interface is configured for I^2C mode.
K7	cs_b_asel0	I	**Chip Select for Serial Interface.** As serial interface chip select, this is an active low signal. This pin is also a part of the I^2C address select when the host interface is configured for I^2C mode.This pin is internally pulled up to V_{DD}.
JTAG (IEEE 1149.1) and Test			
G12	IC2	I	**Internal Connection**. Connect this pin to GND.
E11	IC1	A-I/O	**Internal Connection.** Leave unconnected.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
G2	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G1	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
F2	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be held low or pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock.** Provides the clock for the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
G3	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock Note: The **osci_1V8/osco_1V8** pins are preferred to connect a crystal to the device. The **XOin** pin is preferred to connect a crystal oscillator (XO) to the device.			
A7	osco_3V3	A-O	**3.3V Crystal Master Clock Output.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osci_3V3**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be left unconnected.
A8	osci_3V3	I	**3.3V Crystal Master Clock Input.** For the alternative connection method for a crystal, the crystal is connected from this pin to **osco_3V3**. For clock oscillator operation or the use of a crystal between **osci_1V8** and **osco_1V8**, this pin should be grounded.
A5	osco_1V8	A-O	**1.8V Crystal Master Clock Output.** For the primary connection method for a crystal, the crystal is connected from this pin to **osci_1V8**. Not suitable for driving other devices. For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be left unconnected.
B5	osci_1V8	I	**1.8V Crystal Master Clock Input.** For the primary connection method for a crystal, the crystal is connected from this pin to **osco_1V8.** For clock oscillator operation or the use of a crystal between **osci_3V3** and **osco_3V3**, this pin should be grounded.
B7	XOin	I	**XO Master Clock Output.** For clock oscillator operation, this pin is connected to the output of the oscillator. For crystal operation using either method, this pin should be grounded.
Power and Ground			

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B8 C6 H9 J9 K6 M1	V_{CORE0} V_{CORE1} V_{CORE2} V_{CORE3} V_{CORE4} V_{CORE5}		**Positive Supply Voltage.** +1.8V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations
A2 A4 A6 A9 A11 C3 C10 D1 D12 E2 E3 E10 G9 J1 J12 L1	V_{DD0} V_{DD1} V_{DD2} V_{DD3} V_{DD4} V_{DD5} V_{DD6} V_{DD7} V_{DD8} V_{DD9} V_{DD10} V_{DD11} V_{DD12} V_{DD13} V_{DD14} V_{DD15}		**Positive Supply Voltage.** +3.3V_{DC} nominal. These pins should not be connected together on the board. Please refer to ZLAN-327 for recommendations

Table 1 - Pin Description (continued)

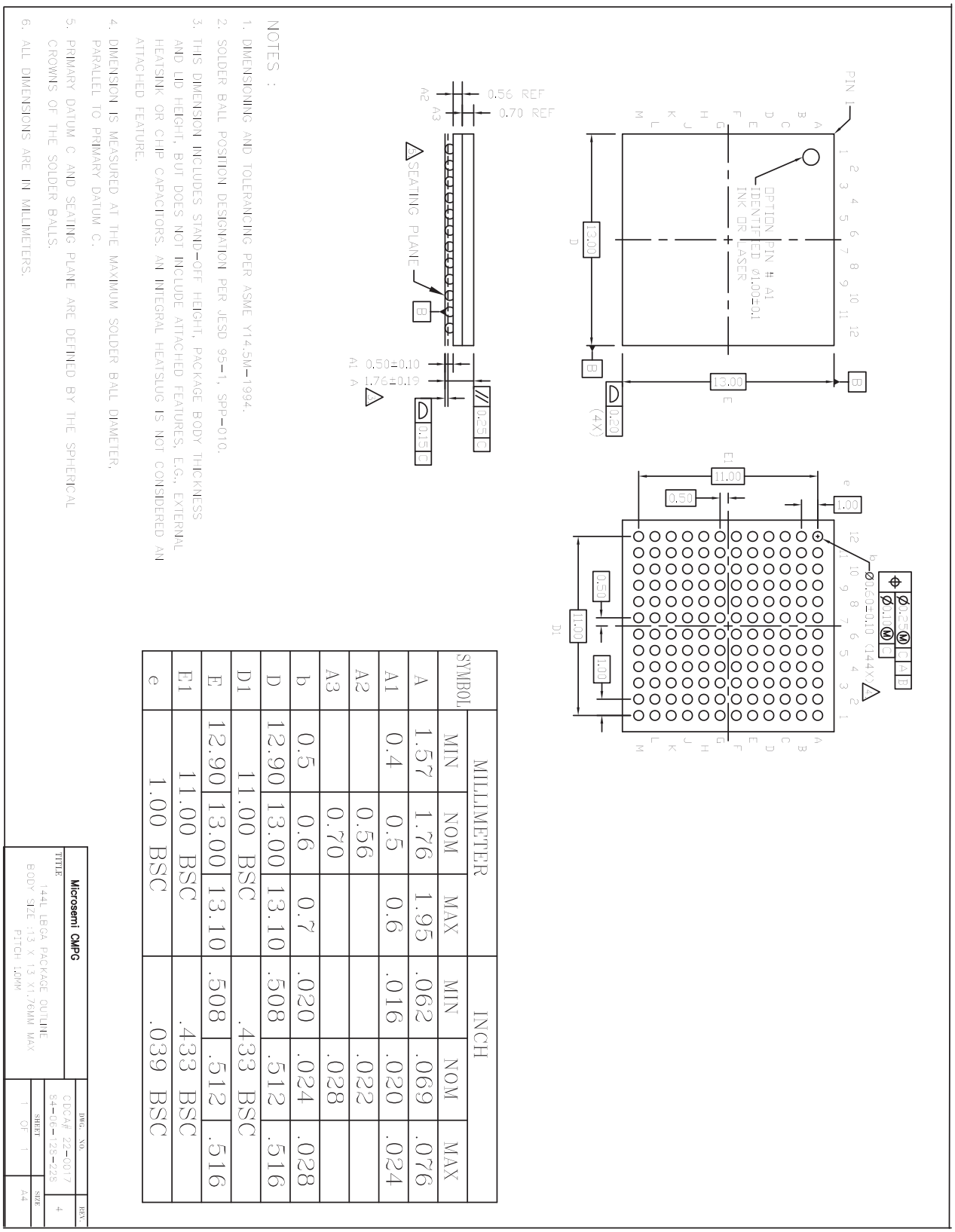
Ball #	Name	I/O	Description
B2 B4 B6 B9 B11 C4 C5 C7 C8 C9 D2 D11 E4 E9 G4 H4 H5 H6 H7 H8 J2 J4 J5 J6 J7 J8 J11 K5 L2 M2 D5 D6 D7 D8 E5 E6 E7 E8 F5 F6 F7 F8 G5 G6 G7 G8	V_{SS}		**Ground.** 0 Volts.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
A3 A10 B3 B10 E1 E12 F1 F12	NC		**No Connect.** These pins should be left open.

Table 1 - Pin Description (continued)

3.0 Mechanical Drawing



NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.57	1.76	1.95	.062	.069	.076
A1	0.4	0.5	0.6	.016	.020	.024
A2		0.56			.022	
A3		0.70			.028	
b	0.5	0.6	0.7	.020	.024	.028
D	12.90	13.00	13.10	.508	.512	.516
D1		11.00 BSC			.433 BSC	
E	12.90	13.00	13.10	.508	.512	.516
E1		11.00 BSC			.433 BSC	
e		1.00 BSC			.039 BSC	

Microsemi CMPG			
TITLE: 144L LBGA PACKAGE OUTLINE 13 X 13 X1.76MM MAX BODY SIZE PITCH 1.00MM		DWG. NO: CDCA# 22-0017 S4-06-128-225	REV: 4
	SHEET: 1 OF 1	SIZE: A4	

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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