OCTAL ±100V 1.8A ULTRASOUND PULSER

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Rev.2.0_01

The ABLIC Inc. HDL6V5582 is an eight-channel, high-voltage, high-speed fully-integrated pulser for medical ultrasound imaging applications. The HDL6V5582 consists of logic interface, level translators, MOSFET gate drive buffers with internally-generated floating voltage supplies, and high-voltage, high-current MOSFETs for pulsing and active ground damping for each channel.

Functions

The HDL6V5582 can be used as

- 8-channel, 3-level pulser with active ground damping with 2-input per channel
- 4-channel, 5-level pulser with active ground damping with 3-input per channel

Features

- 0 to ±100V output voltage
- ±1.8A source and sink peak current for pulsing with output blocking high-voltage (HV) diodes
- ±0.5A source and sink peak current for active ground damping with output blocking HV diodes
- 25Ω (±0.5A) active high-voltage clamping without output blocking HV diodes (analog SW type)
- 500Ω (±0.05A) active ground damping without output blocking HV diodes (analog SW type)
- Internally-generated floating voltage supplies to the gate drive buffers
- 3-to-5 decoder with clock/transparent mode control for 5-level operation
- Up to 20MHz operation frequency (@±60V output, 220pF load)
- 1.8V to 5V CMOS logic interface
- 4-mode output drive current control for power saving
- Thermal protection
- Latch-up free, less crosstalk between channels (SOI CMOS technology)
- 52-lead 8mm x 8mm QFN package (RoHS compliant)

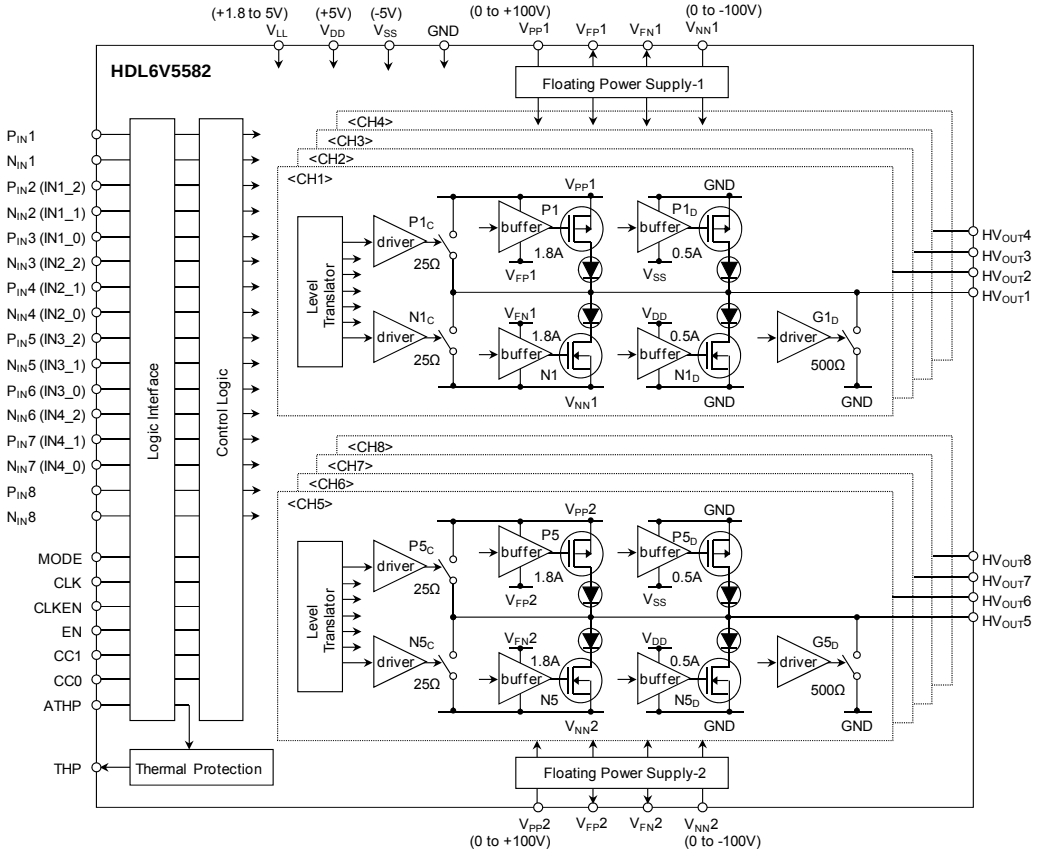


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units
1	Positive logic supply	V_{LL}	-0.4 to +7	V
2	Positive logic and level translator supply	V_{DD}	-0.4 to +7	V
3	Negative logic and level translator supply	V_{SS}	-7 to +0.4	V
4	Positive high voltage supplies (x=1,2)	$V_{PP}x$	-0.5 to +105	V
5	Negative high voltage supplies (x=1,2)	$V_{NN}x$	-105 to +0.5	V
6	Differential high voltage supplies (x=1,2)	$V_{PP}x$- $V_{NN}x$	+210	V
7	High voltage outputs (x=1~8)*	$HV_{OUT}x$	-105 to +105	V
8	THP (THermal Protection) output	THP	-0.4 to +7	V
9	All logic input voltages (x=1~8)	$P_{IN}x$, $N_{IN}x$, EN, CLK, CLKEN, CC1, CC0, ATHP, MODE	-0.4 to +7	V
10	Operating junction temperature	T_{Jop}	-20 to +150	°C
11	Storage temperature	T_{STG}	-55 to +150	°C
12	Maximum power dissipation	P_{Dmax}	4	W

Note: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Conditions, and Circuits (Recommended)

2.1 Operating Supply Voltages and Conditions

Table 2 Recommended Operating Supply Voltages and Conditions

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic voltage supply	V_{LL}	2.4	2.5 to 5	V_{DD}	V	Clock mode(≤80MHz)
			2.6	2.7 to 5	V_{DD}	V	Clock mode(≤100MHz)
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Positive low voltage supply	V_{DD}	4.75	5	5.25	V	
3	Negative low voltage supply	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high voltage supplies (x=1,2)	$V_{PP}x$	0	-	100	V	
5	Negative high voltage supplies (x=1,2)	$V_{NN}x$	-100	-	0	V	
6	Differential high voltage supplies (x=1,2)	$V_{PP}x$- $V_{NN}x$	0	-	200	V	
7	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V	
8	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V	
9	IC substrate voltage *	V_{SUB}	-	0	-	V	
10	Slew rate limit of $V_{PP}x$, $V_{NN}x$ (x=1,2)	SR_{MAX}	-	-	25	V/ms	
11	Operating free-air temperature	T_A	0	25	75	°C	

Note: * Substrate bottom is internally connected to the central thermal pad on the bottom of the package. It must be soldered to the ground.

2.2 Power-Up/Down Sequence

Power-Up Sequence

1	V_{LL}
2	V_{DD}, V_{SS}
3	Set EN=1 *
4	$V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
5	Logic control signals

Power-Down Sequence

1	Set EN=1 *
2	$V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
3	V_{DD}, V_{SS}
4	V_{LL}

High-voltage Change Sequence during Power-ON

1	Set EN=1 *
2	Change $V_{PP}1$, $V_{PP}2$, $V_{NN}1$, $V_{NN}2$
3	Logic control signals

Note:
* If CLKEN=0 (clock mode), it is required to set EN=1 before applying high voltages in order to avoid failure. EN=1 sets $HV_{OUT}x$ to high-impedance (HiZ) regardless of clock state.
If CLKEN=1 (transparent mode), it is also workable to set $P_{IN}x$=$N_{IN}x$=0 instead of EN=1.

Note:
It is indispensable to avoid the occurrence of the excessive voltage beyond the maximum rating in applying and cutting of the power supplies.

2.3 Application Circuits

(a) 8-channel 3-level pulser with active ground damping (MODE=1)

Clock mode (CLKEN=0) is not available in 8-channel 3-level operation (MODE=1)

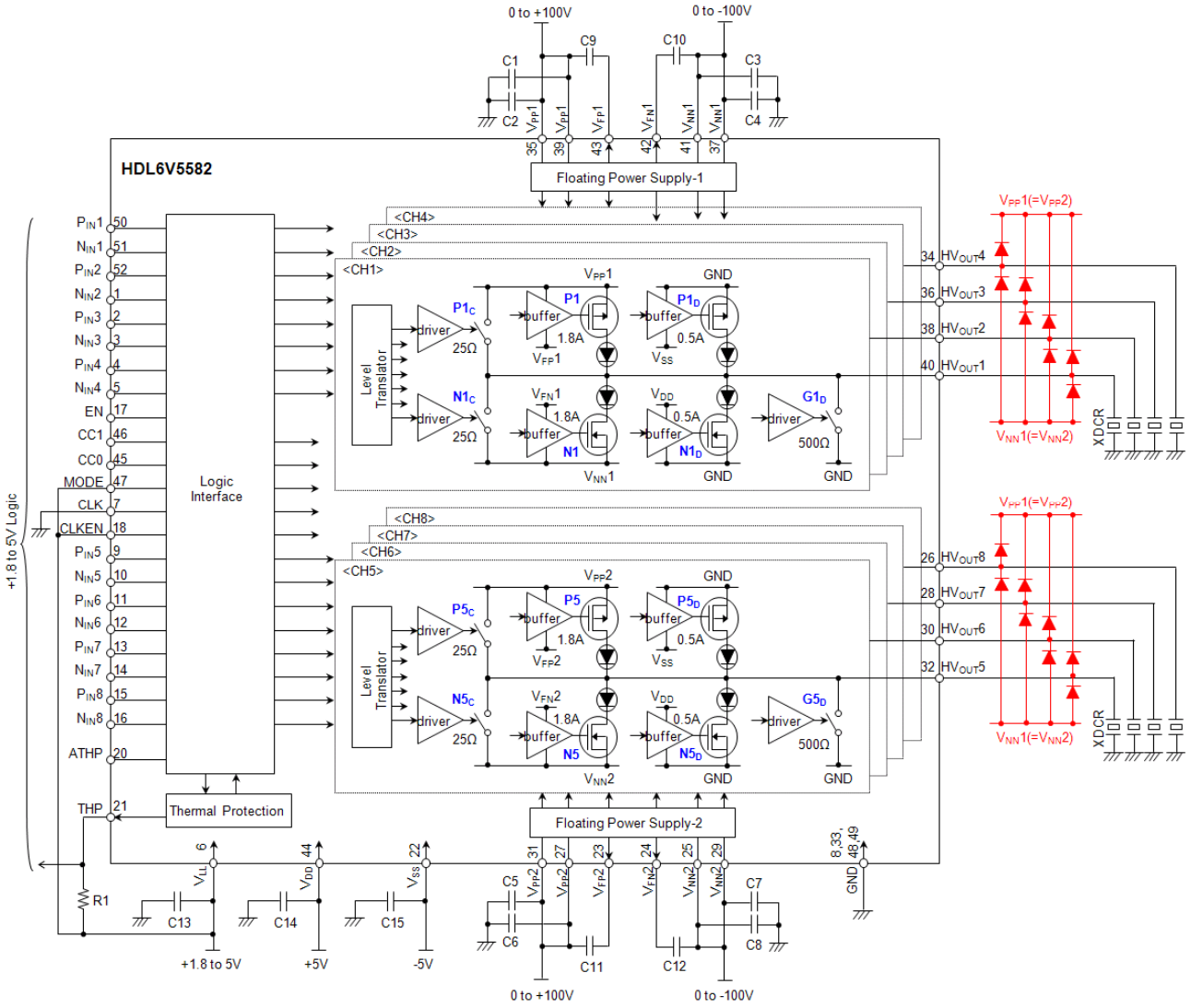


Fig. 2-(a) Typical Application Circuit-1

Note:

1. High-voltage power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±1.8A. Therefore, ceramic capacitors of over 200V 0.1uF to 1uF (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1uF to 1uF (C13~15) should also be connected close to the low-voltage power supply pins, $V_{LL}/V_{DD}/V_{SS}$.
2. Ceramic capacitors of over 15V 0.1uF to 1uF (C9~12) should be connected between each floating voltage pin ($V_{FP}x/V_{FN}x$) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between $HV_{OUT}x$ and $V_{PP}x/V_{NN}x$ as shown in Fig.2-(a) are strongly recommended to avoid excessive voltage overshoot caused by a reflection from a probe.

2.3 Application Circuits (Cont.)

(b) 4-channel 5-level pulser with active ground damping (MODE=0)

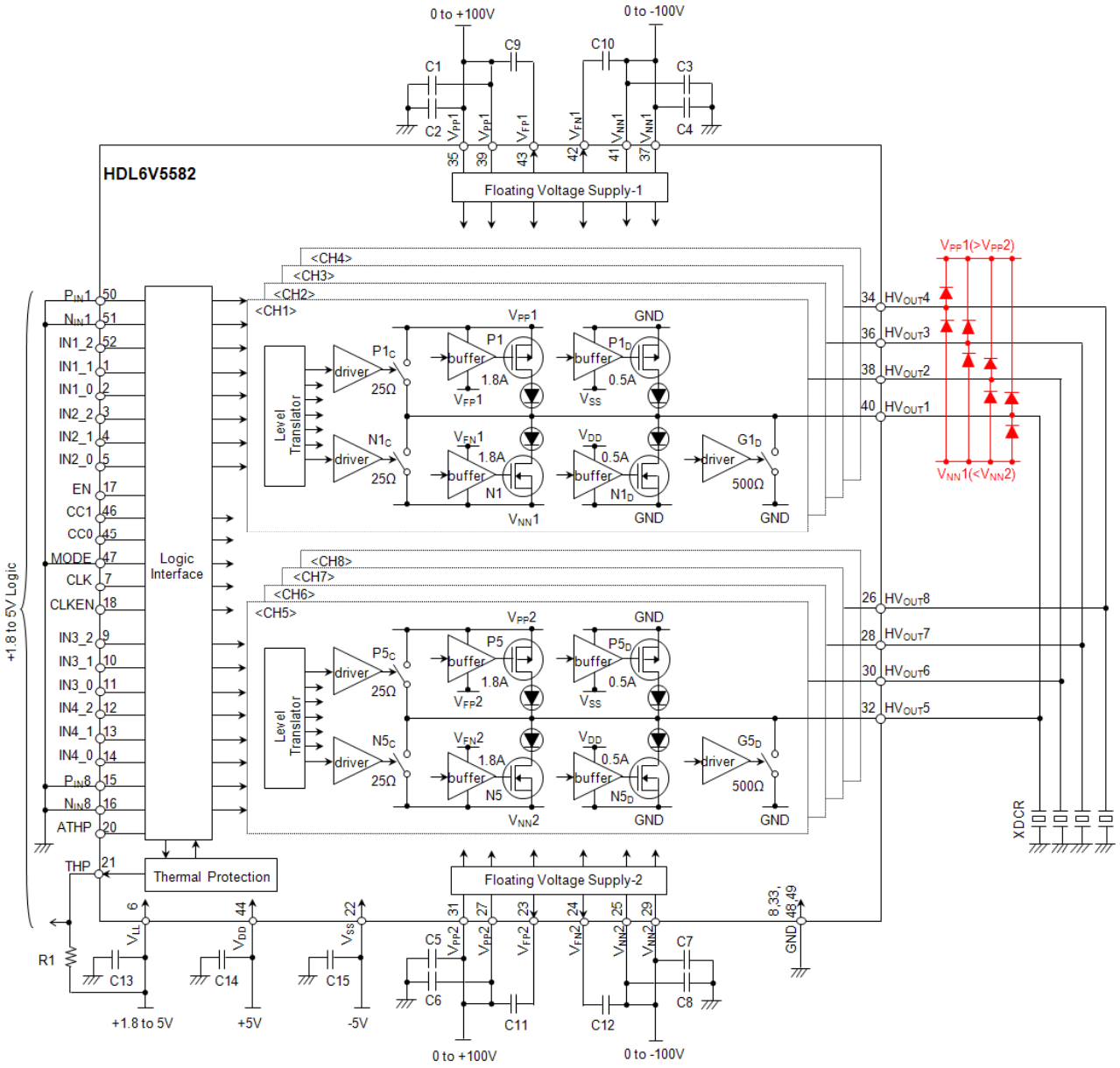


Fig. 2-(b) Typical Application Circuit-2

Note:

1. High-voltage power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±1.8A. Therefore, ceramic capacitors of over 200V 0.1uF to 1uF (C1~8) should be connected as close to the pins as possible for bypassing purpose. Ceramic capacitors of over 15V 0.1uF to 1uF (C13~15) should also be connected close to the low-voltage power supply pins, $V_{LL}/V_{DD}/V_{SS}$.
2. Ceramic capacitors of over 15V 0.1uF to 1uF (C9~12) should be connected between each floating voltage pin ($V_{FP}x/V_{FN}x$) and high-voltage power supply pin for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. **[PRECAUTION]** External high-voltage clamp diodes between $HV_{OUT}x$ and $V_{PP}1/V_{NN}1$(highest voltage) as shown in Fig.2-(b) are strongly recommended to avoid excessive voltage overshoot caused by a reflection from a probe.

3. Electrical Characteristics

3.1 MODE=1 (8-channel 3-level pulser with active ground damping)

DC Characteristics

Table 3 DC Characteristics

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, MODE=1, CLK=0, CLKEN=1, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	µA	P_{IN}x, N_{IN}x, EN, CC1, CC0, CLK, CLKEN, MODE
			-	66	-	µA	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	µA	P_{IN}x, N_{IN}x, CLK, ATHP
			-	66	-	µA	EN, CC1, CC0, CLKEN, MODE 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	0.5	-	µA	Quiescent current-1 EN=1(Disable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V
5	V_{DD} current	I_{DDQD}	-	2.0	-	mA	
6	V_{SS} current	I_{SSQD}	-	1.0	-	mA	
7	$V_{PP}1$ current	I_{PP1QD}	-	0.2	-	mA	
8	$V_{NN}1$ current	I_{NN1QD}	-	0.2	-	mA	
9	$V_{PP}2$ current	I_{PP2QD}	-	0.2	-	mA	
10	$V_{NN}2$ current	I_{NN2QD}	-	0.2	-	mA	
11	V_{LL} current	I_{LLQE}	-	66	-	µA	Quiescent current-2 EN=0(Enable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V P_{IN}x=1, N_{IN}x=1 (x=1~8)
12	V_{DD} current	I_{DDQE}	-	8.0	-	mA	
13	V_{SS} current	I_{SSQE}	-	7.5	-	mA	
14	$V_{PP}1$ current	I_{PP1QE}	-	1.3	-	mA	
15	$V_{NN}1$ current	I_{NN1QE}	-	1.4	-	mA	
16	$V_{PP}2$ current	I_{PP2QE}	-	1.3	-	mA	
17	$V_{NN}2$ current	I_{NN2QE}	-	1.4	-	mA	
18	V_{LL} current	I_{LLPW}	-	75	-	µA	Operating current-1 8-channel active Bipolar 1-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V EN=0, ATHP=0 Current mode=4
19	V_{DD} current	I_{DDPW}	-	8.1	-	mA	
20	V_{SS} current	I_{SSPW}	-	7.6	-	mA	
21	$V_{PP}1$ current	I_{PP1PW}	-	1.8	-	mA	
22	$V_{NN}1$ current	I_{NN1PW}	-	2.2	-	mA	
23	$V_{PP}2$ current	I_{PP2PW}	-	1.8	-	mA	
24	$V_{NN}2$ current	I_{NN2PW}	-	2.2	-	mA	

Table 3 DC Characteristics (cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V_{LL} current	I_{LLCW4}	-	0.49	-	mA	Operating current-2 8-channel active Bipolar Continuous Wave Current mode=4 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
26	V_{DD} current	I_{DDCW4}	-	60	-	mA	
27	V_{SS} current	I_{SSCW4}	-	60	-	mA	
28	$V_{PP}1$ current	I_{PP1CW4}	-	90	-	mA	
29	$V_{NN}1$ current	I_{NN1CW4}	-	88	-	mA	
30	$V_{PP}2$ current	I_{PP2CW4}	-	90	-	mA	
31	$V_{NN}2$ current	I_{NN2CW4}	-	88	-	mA	
32	V_{LL} current	I_{LLCW3}	-	0.56	-	mA	Operating current-3 8-channel active Bipolar Continuous Wave Current mode=3 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
33	V_{DD} current	I_{DDCW3}	-	55	-	mA	
34	V_{SS} current	I_{SSCW3}	-	53	-	mA	
35	$V_{PP}1$ current	I_{PP1CW3}	-	86	-	mA	
36	$V_{NN}1$ current	I_{NN1CW3}	-	84	-	mA	
37	$V_{PP}2$ current	I_{PP2CW3}	-	86	-	mA	
38	$V_{NN}2$ current	I_{NN2CW3}	-	84	-	mA	
39	V_{LL} current	I_{LLCW2}	-	0.56	-	mA	Operating current-4 8-channel active Bipolar Continuous Wave Current mode=2 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
40	V_{DD} current	I_{DDCW2}	-	51	-	mA	
41	V_{SS} current	I_{SSCW2}	-	47	-	mA	
42	$V_{PP}1$ current	I_{PP1CW2}	-	82	-	mA	
43	$V_{NN}1$ current	I_{NN1CW2}	-	80	-	mA	
44	$V_{PP}2$ current	I_{PP2CW2}	-	82	-	mA	
45	$V_{NN}2$ current	I_{NN2CW2}	-	80	-	mA	
46	V_{LL} current	I_{LLCW1}	-	0.62	-	mA	Operating current-5 8-channel active Bipolar Continuous Wave Current mode=1 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
47	V_{DD} current	I_{DDCW1}	-	46	-	mA	
48	V_{SS} current	I_{SSCW1}	-	41	-	mA	
49	$V_{PP}1$ current	I_{PP1CW1}	-	75	-	mA	
50	$V_{NN}1$ current	I_{NN1CW1}	-	74	-	mA	
51	$V_{PP}2$ current	I_{PP2CW1}	-	75	-	mA	
52	$V_{NN}2$ current	I_{NN2CW1}	-	74	-	mA	

AC Characteristics

Table 4 AC Characteristics

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, EN=0, 8-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	$t_{dr(on)}$	-	44	-	ns	Bipolar half cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.3
2	Delay time on outputs fall	$t_{df(on)}$	-	44	-	ns	
3	Delay time off outputs rise	$t_{dr(off)}$	-	44	-	ns	
4	Delay time off outputs fall	$t_{df(off)}$	-	44	-	ns	
5	$\|t_{dr(on)}-t_{df(on)}\|$ Delay time matching	$\Delta t_{delay(on)}$	-	±1		ns	
6	$\|t_{dr(off)}-t_{df(off)}\|$ Delay time matching	$\Delta t_{delay(off)}$	-	±1		ns	
7	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 2-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.4
8	Output rise time	t_r	-	18	-	ns	
9	Output fall time	t_f	-	18	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	20	-	ps	Bipolar Continuous, f=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V Current mode=1, See Fig.5
12	Enable time	t_{EN}	-	44	-	ns	EN fall edge to output burst
13	Disable time	t_{DIS}	-	80	-	ns	EN rise edge to no output

Thermal Protection Characteristics

Table 5 Thermal Protection Characteristics

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	1.0	V	V_{LL}=3.3V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	90	110	130	ºC	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

Device Characteristics

Table 6 Output P-Channel MOSFET Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	$I_{OUT}P$	-	-1.8	-	A	Vgs=-5V, Vds=-100V
2	Channel resistance	$R_{ON}P$	-	7	-	Ω	Vgs=-5V, Id=-0.5A
3	Output capacitance	$C_{OSS}P$	-	30	-	pF	Vgs=0V, Vds=-10V, f=1MHz

Note: These items above are not tested when shipped.

Table 7 Output N-Channel MOSFET Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	$I_{OUT}N$	-	1.8	-	A	Vgs=5V, Vds=100V
2	Channel resistance	$R_{ON}N$	-	7	-	Ω	Vgs=5V, Id=0.5A
3	Output capacitance	$C_{OSS}N$	-	10	-	pF	Vgs=0V, Vds=10V, f=1MHz

Note: These items above are not tested when shipped.

Table 8 Output P-Channel Damp MOSFET Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	$I_{OUT}P_D$	-	-0.5	-	A	Vgs=-5V, Vds=-100V
2	Channel resistance	$R_{ON}P_D$	-	25	-	Ω	Vgs=-5V, Id=-0.1A
3	Output capacitance	$C_{OSS}P_D$	-	8	-	pF	Vgs=0V, Vds=-10V, f=1MHz

Note: These items above are not tested when shipped.

Table 9 Output N-Channel Damp MOSFET Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Output saturation current	$I_{OUT}N_D$	-	0.5	-	A	Vgs=5V, Vds=100V
2	Channel resistance	$R_{ON}N_D$	-	25	-	Ω	Vgs=5V, Id=0.1A
3	Output capacitance	$C_{OSS}N_D$	-	3	-	pF	Vgs=0V, Vds=10V, f=1MHz

Note: These items above are not tested when shipped.

Table 10 Active Clamper/Damper Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	On-state resistance (Px_C)	R_{ONPC}	-	25	-	Ω	Vgs=-5V, Id=-0.1A
2	On-state resistance (Nx_C)	R_{ONNC}	-	25	-	Ω	Vgs=5V, Id=0.1A
3	On-state resistance (Gx_D)	R_{ONGD}	-	500	-	Ω	Vgs=5V, Id=0.01A

Note: These items above are not tested when shipped.

Table 11 Output HV Diode Characteristics

T_A=25°C

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FDHV}	-	1.0	-	V	I_F=100mA
2	Reverse voltage	V_{RDHV}	200	-	-	V	I_R=1μA

Note: These items above are not tested when shipped.

3.2 MODE=0 (4-channel 5-level pulser with active ground damping)

3.2.1 Clock Mode (CLKEN=0)

DC Characteristics

Table 12 DC Characteristics (Clock mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, MODE=0, CLK=100MHz, CLKEN=0, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	µA	INx_2, INx_1, INx_0, EN, CC1, CC0, CLK, CLKEN, MODE
			-	66	-	µA	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	µA	INx_2, INx_1, INx_0, CLK, ATHP
			-	66	-	µA	EN, CC1, CC0, CLKEN, MODE 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	0.62	-	mA	Quiescent current-1 EN=1(Disable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V
5	V_{DD} current	I_{DDQD}	-	7.0	-	mA	
6	V_{SS} current	I_{SSQD}	-	1.0	-	mA	
7	$V_{PP}1$ current	I_{PP1QD}	-	0.20	-	mA	
8	$V_{NN}1$ current	I_{NN1QD}	-	0.20	-	mA	
9	$V_{PP}2$ current	I_{PP2QD}	-	0.20	-	mA	
10	$V_{NN}2$ current	I_{NN2QD}	-	0.20	-	mA	
11	V_{LL} current	I_{LLQE}	-	0.67	-	mA	Quiescent current-2 EN=0(Enable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_2=1, INx_1=0, INx_0=0 (x=1~4)
12	V_{DD} current	I_{DDQE}	-	13	-	mA	
13	V_{SS} current	I_{SSQE}	-	7.5	-	mA	
14	$V_{PP}1$ current	I_{PP1QE}	-	1.3	-	mA	
15	$V_{NN}1$ current	I_{NN1QE}	-	1.4	-	mA	
16	$V_{PP}2$ current	I_{PP2QE}	-	1.3	-	mA	
17	$V_{NN}2$ current	I_{NN2QE}	-	1.4	-	mA	
18	V_{LL} current	I_{LLPW}	-	0.77	-	mA	Operating current-1 4-channel active Bipolar 3-level 1-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V EN=0, ATHP=0 Current mode=4
19	V_{DD} current	I_{DDPW}	-	17	-	mA	
20	V_{SS} current	I_{SSPW}	-	7.6	-	mA	
21	$V_{PP}1$ current	I_{PP1PW}	-	1.9	-	mA	
22	$V_{NN}1$ current	I_{NN1PW}	-	2.4	-	mA	
23	$V_{PP}2$ current	I_{PP2PW}	-	1.3	-	mA	
24	$V_{NN}2$ current	I_{NN2PW}	-	1.4	-	mA	

Table 12 DC Characteristics (Clock mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V_{LL} current	I_{LLPW}	-	0.77	-	mA	Operating current-2 4-channel active Bipolar 5-level 1-cycle f=4.2MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V EN=0, ATHP=0 Current mode=4 See Fig.9
26	V_{DD} current	I_{DDPW}	-	17	-	mA	
27	V_{SS} current	I_{SSPW}	-	7.8	-	mA	
28	$V_{PP}1$ current	I_{PP1PW}	-	1.7	-	mA	
29	$V_{NN}1$ current	I_{NN1PW}	-	1.9	-	mA	
30	$V_{PP}2$ current	I_{PP2PW}	-	1.5	-	mA	
31	$V_{NN}2$ current	I_{NN2PW}	-	1.8	-	mA	
32	V_{LL} current	I_{LLCW4}	-	1.0	-	mA	Operating current-3 4-channel active Bipolar 3-level Continuous Current mode=4 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
33	V_{DD} current	I_{DDCW4}	-	43	-	mA	
34	V_{SS} current	I_{SSCW4}	-	33	-	mA	
35	$V_{PP}1$ current	I_{PP1CW4}	-	100	-	mA	
36	$V_{NN}1$ current	I_{NN1CW4}	-	96	-	mA	
37	$V_{PP}2$ current	I_{PP2CW4}	-	1.3	-	mA	
38	$V_{NN}2$ current	I_{NN2CW4}	-	1.4	-	mA	
39	V_{LL} current	I_{LLCW3}	-	1.1	-	mA	Operating current-4 4-channel active Bipolar 3-level Continuous Current mode=3 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
40	V_{DD} current	I_{DDCW3}	-	40	-	mA	
41	V_{SS} current	I_{SSCW3}	-	30	-	mA	
42	$V_{PP}1$ current	I_{PP1CW3}	-	95	-	mA	
43	$V_{NN}1$ current	I_{NN1CW3}	-	92	-	mA	
44	$V_{PP}2$ current	I_{PP2CW3}	-	1.2	-	mA	
45	$V_{NN}2$ current	I_{NN2CW3}	-	1.3	-	mA	
46	V_{LL} current	I_{LLCW2}	-	1.1	-	mA	Operating current-5 4-channel active Bipolar 3-level Continuous Current mode=2 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
47	V_{DD} current	I_{DDCW2}	-	38	-	mA	
48	V_{SS} current	I_{SSCW2}	-	27	-	mA	
49	$V_{PP}1$ current	I_{PP1CW2}	-	89	-	mA	
50	$V_{NN}1$ current	I_{NN1CW2}	-	87	-	mA	
51	$V_{PP}2$ current	I_{PP2CW2}	-	1.1	-	mA	
52	$V_{NN}2$ current	I_{NN2CW2}	-	1.2	-	mA	
53	V_{LL} current	I_{LLCW1}	-	1.2	-	mA	Operating current-6 4-channel active Bipolar 3-level Continuous Current mode=1 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
54	V_{DD} current	I_{DDCW1}	-	35	-	mA	
55	V_{SS} current	I_{SSCW1}	-	23	-	mA	
56	$V_{PP}1$ current	I_{PP1CW1}	-	82	-	mA	
57	$V_{NN}1$ current	I_{NN1CW1}	-	81	-	mA	
58	$V_{PP}2$ current	I_{PP2CW1}	-	1.0	-	mA	
59	$V_{NN}2$ current	I_{NN2CW1}	-	1.1	-	mA	

AC Characteristics

Table 13 AC Characteristics (Clock mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, MODE=0, EN=0, CLK=100MHz, CLKEN=0, 4-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input clock frequency	f_{CLK}	-	100	-	MHz	See Fig.6 D= τ /T
2	Duty cycle	D	40	50	60	%	
3	Setup time	t_{SU}	0.0	-	-	ns	
4	Hold time	t_{HOLD}	4.0	-	-	ns	
5	Delay time on outputs rise	$t_{dr(on)}$	-	57	-	ns	Bipolar 3-level half cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.7
6	Delay time on outputs fall	$t_{df(on)}$	-	57	-	ns	
7	Delay time off outputs rise	$t_{dr(off)}$	-	57	-	ns	
8	Delay time off outputs fall	$t_{df(off)}$	-	57	-	ns	
9	$\lvert t_{dr(on)}-t_{df(on)}\rvert$ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
10	$\lvert t_{dr(off)}-t_{df(off)}\rvert$ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
11	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 3-level 2-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.8
12	Output rise time	t_r	-	19	-	ns	
13	Output fall time	t_f	-	19	-	ns	
14	Second harmonic distortion	HD2	-	-40	-	dBc	
15	Second harmonic distortion	HD2	-	-40	-	dBc	Bipolar 5-level 1-cycle, f=4.2MHz PRT=200µs, Current mode=4 $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V, See Fig.9
16	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	20	-	ps	Bipolar Continuous, f=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V Current mode=1, See Fig.10
17	Enable time	t_{EN}	-	57	-	ns	EN fall edge to output burst
18	Disable time	t_{DIS}	-	80	-	ns	EN rise edge to no output

See Table 5 through 11 for the characteristics of Thermal Protection, and Devices.

3.2.2 Transparent Mode (CLKEN=1, CLK=0)

Table 14 DC Characteristics (Transparent mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, MODE=0, CLK=0, CLKEN=1, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Input logic high current	I_{IH}	-10	-	10	μA	INx_2, INx_1, INx_0, EN, CC1, CC0, CLK, CLKEN, MODE
			-	66	-	μA	ATHP 50kΩ internal pull-down resistor
2	Input logic low current	I_{IL}	-10	-	10	μA	INx_2, INx_1, INx_0, CLK, ATHP
			-	66	-	μA	EN, CC1, CC0, CLKEN, MODE 50kΩ internal pull-up resistor
3	Input logic capacitance	C_{IN}	-	2	-	pF	-
4	V_{LL} current	I_{LLQD}	-	66	-	μA	Quiescent current-1 EN=1(Disable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V
5	V_{DD} current	I_{DDQD}	-	2.0	-	mA	
6	V_{SS} current	I_{SSQD}	-	1.0	-	mA	
7	$V_{PP}1$ current	I_{PP1QD}	-	0.20	-	mA	
8	$V_{NN}1$ current	I_{NN1QD}	-	0.20	-	mA	
9	$V_{PP}2$ current	I_{PP2QD}	-	0.20	-	mA	
10	$V_{NN}2$ current	I_{NN2QD}	-	0.20	-	mA	
11	V_{LL} current	I_{LLQE}	-	0.14	-	mA	Quiescent current-2 EN=0(Enable), ATHP=0 Current mode=4 $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V INx_2=1, INx_1=0, INx_0=0 (x=1~4)
12	V_{DD} current	I_{DDQE}	-	8.0	-	mA	
13	V_{SS} current	I_{SSQE}	-	7.5	-	mA	
14	$V_{PP}1$ current	I_{PP1QE}	-	1.3	-	mA	
15	$V_{NN}1$ current	I_{NN1QE}	-	1.4	-	mA	
16	$V_{PP}2$ current	I_{PP2QE}	-	1.3	-	mA	
17	$V_{NN}2$ current	I_{NN2QE}	-	1.4	-	mA	
18	V_{LL} current	I_{LLPW}	-	0.14	-	mA	Operating current-1 4-channel active Bipolar 3-level 1-cycle f=5MHz, PRT=200μs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V EN=0, ATHP=0 Current mode=4
19	V_{DD} current	I_{DDPW}	-	8.1	-	mA	
20	V_{SS} current	I_{SSPW}	-	7.6	-	mA	
21	$V_{PP}1$ current	I_{PP1PW}	-	1.9	-	mA	
22	$V_{NN}1$ current	I_{NN1PW}	-	2.4	-	mA	
23	$V_{PP}2$ current	I_{PP2PW}	-	1.3	-	mA	
24	$V_{NN}2$ current	I_{NN2PW}	-	1.4	-	mA	

Table 14 DC Characteristics (Transparent mode; cont.)

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
25	V_{LL} current	I_{LLPW}	-	0.14	-	mA	Operating current-2 4-channel active Bipolar 5-level 1-cycle f=4.2MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V EN=0, ATHP=0 Current mode=4 See Fig.9
26	V_{DD} current	I_{DDPW}	-	8.1	-	mA	
27	V_{SS} current	I_{SSPW}	-	7.8	-	mA	
28	$V_{PP}1$ current	I_{PP1PW}	-	1.7	-	mA	
29	$V_{NN}1$ current	I_{NN1PW}	-	1.9	-	mA	
30	$V_{PP}2$ current	I_{PP2PW}	-	1.5	-	mA	
31	$V_{NN}2$ current	I_{NN2PW}	-	1.8	-	mA	
32	V_{LL} current	I_{LLCW4}	-	0.35	-	mA	Operating current-3 4-channel active Bipolar 3-level Continuous Current mode=4 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
33	V_{DD} current	I_{DDCW4}	-	34	-	mA	
34	V_{SS} current	I_{SSCW4}	-	33	-	mA	
35	$V_{PP}1$ current	I_{PP1CW4}	-	99	-	mA	
36	$V_{NN}1$ current	I_{NN1CW4}	-	95	-	mA	
37	$V_{PP}2$ current	I_{PP2CW4}	-	1.3	-	mA	
38	$V_{NN}2$ current	I_{NN2CW4}	-	1.4	-	mA	
39	V_{LL} current	I_{LLCW3}	-	0.42	-	mA	Operating current-4 4-channel active Bipolar 3-level Continuous Current mode=3 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
40	V_{DD} current	I_{DDCW3}	-	32	-	mA	
41	V_{SS} current	I_{SSCW3}	-	30	-	mA	
42	$V_{PP}1$ current	I_{PP1CW3}	-	94	-	mA	
43	$V_{NN}1$ current	I_{NN1CW3}	-	92	-	mA	
44	$V_{PP}2$ current	I_{PP2CW3}	-	1.2	-	mA	
45	$V_{NN}2$ current	I_{NN2CW3}	-	1.3	-	mA	
46	V_{LL} current	I_{LLCW2}	-	0.42	-	mA	Operating current-5 4-channel active Bipolar 3-level Continuous Current mode=2 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
47	V_{DD} current	I_{DDCW2}	-	30	-	mA	
48	V_{SS} current	I_{SSCW2}	-	27	-	mA	
49	$V_{PP}1$ current	I_{PP1CW2}	-	89	-	mA	
50	$V_{NN}1$ current	I_{NN1CW2}	-	88	-	mA	
51	$V_{PP}2$ current	I_{PP2CW2}	-	1.1	-	mA	
52	$V_{NN}2$ current	I_{NN2CW2}	-	1.2	-	mA	
53	V_{LL} current	I_{LLCW1}	-	0.49	-	mA	Operating current-6 4-channel active Bipolar 3-level Continuous Current mode=1 f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V EN=0, ATHP=0
54	V_{DD} current	I_{DDCW1}	-	27	-	mA	
55	V_{SS} current	I_{SSCW1}	-	23	-	mA	
56	$V_{PP}1$ current	I_{PP1CW1}	-	82	-	mA	
57	$V_{NN}1$ current	I_{NN1CW1}	-	81	-	mA	
58	$V_{PP}2$ current	I_{PP2CW1}	-	1.0	-	mA	
59	$V_{NN}2$ current	I_{NN2CW1}	-	1.1	-	mA	

AC Characteristics

Table 15 AC Characteristics (Transparent mode)

V_{LL}=3.3V, V_{DD}=5V, V_{SS}=-5V, T_A=25°C, 220pF//1kΩ load, MODE=0, EN=0, CLK=0, CLKEN=1, 4-channel active, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Delay time on outputs rise	$t_{dr(on)}$	-	52	-	ns	Bipolar 3-level half cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.7
2	Delay time on outputs fall	$t_{df(on)}$	-	52	-	ns	
3	Delay time off outputs rise	$t_{dr(off)}$	-	52	-	ns	
4	Delay time off outputs fall	$t_{df(off)}$	-	52	-	ns	
5	$\|t_{dr(on)}-t_{df(on)}\|$ Delay time matching	$\Delta t_{delay(on)}$	-	±1	±3	ns	
6	$\|t_{dr(off)}-t_{df(off)}\|$ Delay time matching	$\Delta t_{delay(off)}$	-	±1	±3	ns	
7	Output frequency range	f_{OUT}	-	-	20	MHz	Bipolar 3-level 2-cycle f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode=4 See Fig.8
8	Output rise time	t_r	-	19	-	ns	
9	Output fall time	t_f	-	19	-	ns	
10	Second harmonic distortion	HD2	-	-40	-	dBc	
11	Second harmonic distortion	HD2	-	-40	-	dBc	Bipolar 5-level 1-cycle, f=4.2MHz PRT=200µs, Current mode=4 $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-30V, See Fig.9
12	Delay jitter on rise or fall	t_{Jr}, t_{Jf}	-	20	-	ps	Bipolar Continuous, f=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V Current mode=1, See Fig.10
13	Enable time	t_{EN}	-	52	-	ns	EN fall edge to output burst
14	Disable time	t_{DIS}	-	80	-	ns	EN rise edge to no output

See Table 5 through 11 for the characteristics of Thermal Protection, and Devices.

4. Switching Time Diagram (EN=0)

4.1 MODE=1 (8-channel 3-level pulser with active ground damping)

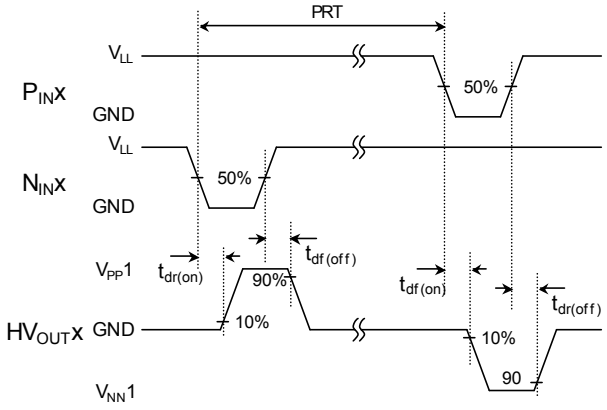


Fig. 3 Propagation delay time

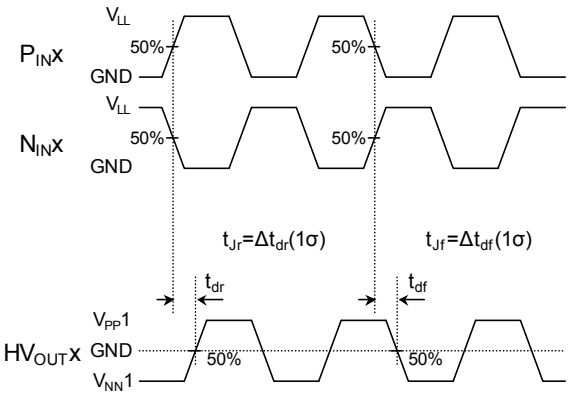


Fig. 5 Delay jitter on rise/fall

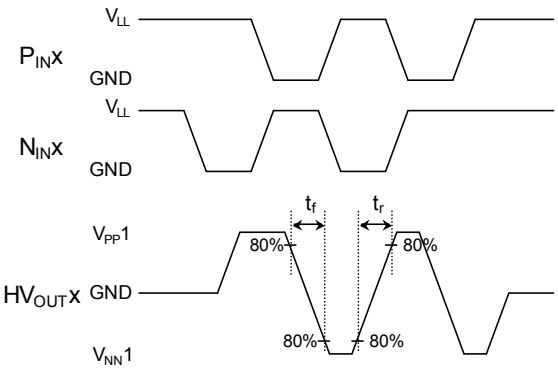


Fig. 4 Output rise/fall time

4.2 MODE=0 (4-channel 5-level pulser with active ground damping)

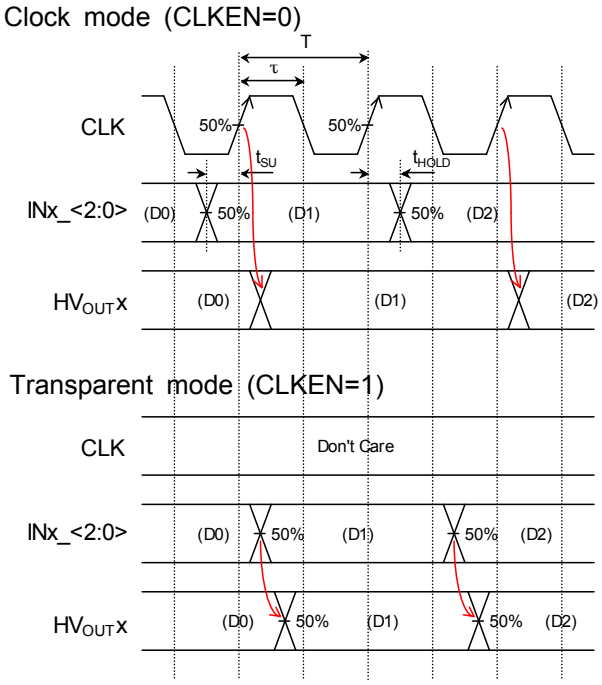


Fig. 6 Setup/hold time

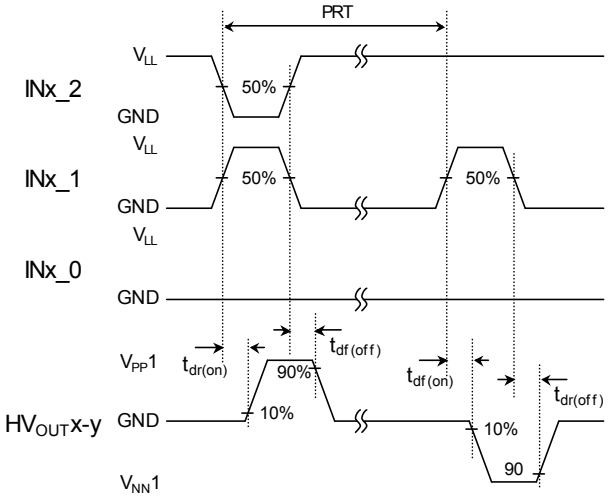


Fig. 7 Propagation delay time

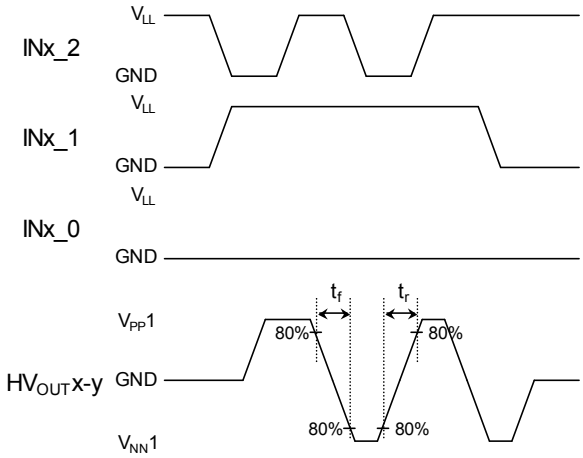


Fig. 8 Output rise/fall time

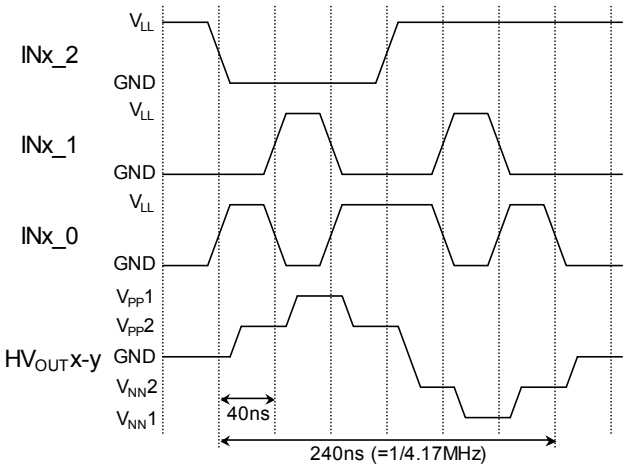


Fig. 9 5-level 1-cycle operation

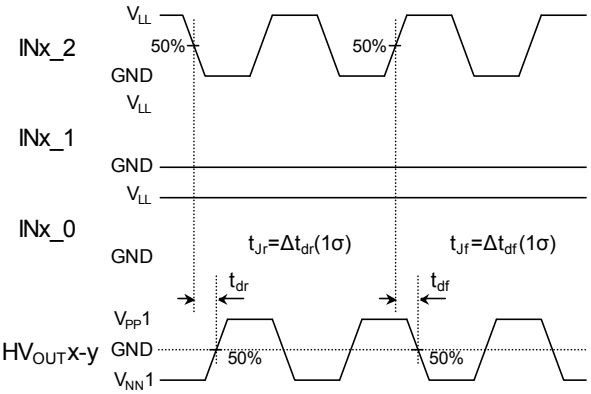


Fig. 10 Delay jitter on rise/fall

5. Truth Table

5.1 MODE=1 (8-channel 3-level pulser with active ground damping)

Table 16 Truth Table (8-channel 3-level)

Logic Inputs				HV MOSFET status							Output
MODE	**EN**	**$P_{IN}x$**	**$N_{IN}x$**	**Px**	**Px_C**	**Nx**	**Nx_C**	**Px_D**	**Nx_D**	**Gx_D**	**$HV_{OUT}x$**
				+HV	+HV	-HV	-HV	GND	GND	GND	
1	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ
1	0	0	1	OFF	OFF	**ON**	**ON**	OFF	OFF	OFF	-HV
1	0	1	0	**ON**	**ON**	OFF	OFF	OFF	OFF	OFF	+HV
1	0	1	1	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	GND
1	1	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ

Note:
- x=1~8
- $V_{PP}1$/ $V_{NN}1$= $V_{PP}2$/ $V_{NN}2$=+/-HV
- 2 inputs/channel

5.2 MODE=0 (4-channel 5-level pulser with active ground damping)

Table 17 Truth Table (4-channel 5-level)

Logic Inputs					HV MOSFET status														Output
MODE	**EN**	**INx_2**	**INx_1**	**INx_0**	**Px**	**Px_C**	**Nx**	**Nx_C**	**Px_D**	**Nx_D**	**Gx_D**	**Py**	**Py_C**	**Ny**	**Ny_C**	**Py_D**	**Ny_D**	**Gy_D**	**$HV_{OUT}x$-y**
		Pol	HV1	HV2	+HV1	+HV1	-HV1	-HV1	GND	GND	GND	+HV2	+HV2	-HV2	-HV2	GND	GND	GND	
0	0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ
0	0	0	0	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	OFF	OFF	OFF	OFF	OFF	+HV2
0	0	0	1	X	**ON**	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	+HV1
0	0	1	0	0	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	GND
0	0	1	0	1	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	OFF	OFF	OFF	-HV2
0	0	1	1	X	OFF	OFF	**ON**	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	-HV1
0	1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	HiZ

Note:
- HV_{OUT}x-y stands for connecting HV_{OUT}x and HV_{OUT}y (x=1~4, y=5~8). Four pairs of output must be HV_{OUT}1-5, HV_{OUT}2-6, HV_{OUT}3-7, and HV_{OUT}4-8, respectively. See Fig.2-(b).
- $V_{PP}1$/$V_{NN}1$=+/-HV1, $V_{PP}2$/$V_{NN}2$=+/-HV2
- 3 inputs/channel

6. Drive Current Mode Control

Table 18 Drive Current Mode Control Table

			$\|I_{OUT}\|$ [A] *1	
Current Mode	**CC1**	**CC0**	**Px**	**Nx**
1	0	0	0.45	0.45
2	0	1	0.9	0.9
3	1	0	1.35	1.35
4	1	1	1.8	1.8

Note:
*1) Output saturation current @ |Vds|=100V
Following current mode is recommended:
- Current mode=4 for high voltage, short pulse train operations
- Current mode=1 for low voltage, long pulse train or even continuous wave operations

7. Pin Configuration

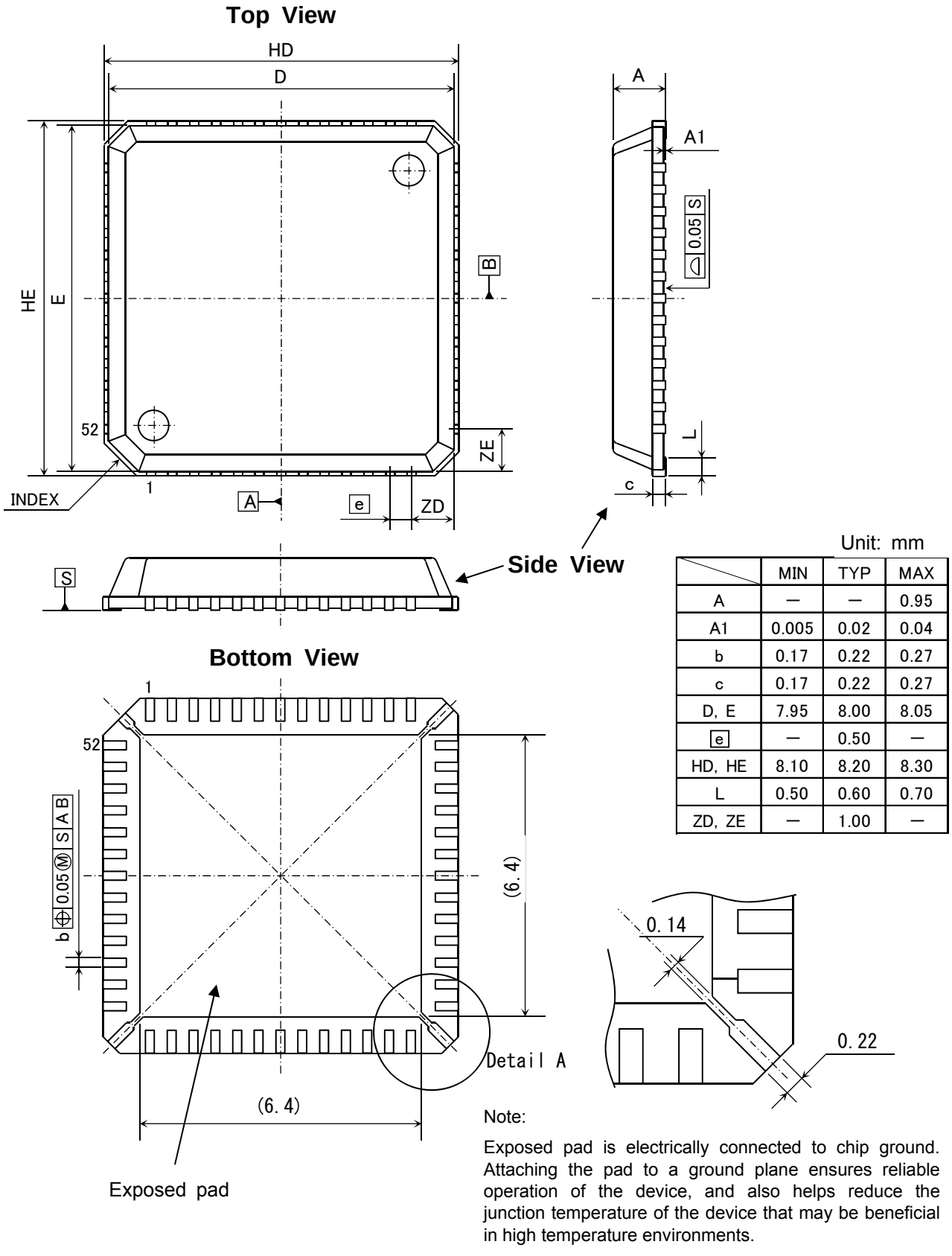
Table 19 Pin Configuration

Pin#	Pin Name	I/O	Function
1	$N_{IN}2$ (IN1_1)	I	Input logic control of the output of channel 2 @ MODE=1 (Input logic control of the 2nd significant bit for coupled output of channel 1 and channel 5 @ MODE=0)
2	$P_{IN}3$ (IN1_0)	I	Input logic control of the output of channel 3 @ MODE=1 (Input logic control of the least significant bit for coupled output of channel 1 and channel 5 @ MODE=0)
3	$N_{IN}3$ (IN2_2)	I	Input logic control of the output of channel 3 @ MODE=1 (Input logic control of the most significant bit for coupled output of channel 2 and channel 6 @ MODE=0)
4	$P_{IN}4$ (IN2_1)	I	Input logic control of the output of channel 4 @ MODE=1 (Input logic control of the 2nd significant bit for coupled output of channel 2 and channel 6 @ MODE=0)
5	$N_{IN}4$ (IN2_0)	I	Input logic control of the output of channel 4 @ MODE=1 (Input logic control of the least significant bit for coupled output of channel 2 and channel 6 @ MODE=0)
6	V_{LL}	-	Positive voltage supply of low voltage interface (+1.8~5V)
7	CLK	I	Clock Input (100MHz typ)
8	GND	-	Drive power ground (0V)
9	$P_{IN}5$ (IN3_2)	I	Input logic control of the output of channel 5 @ MODE=1 (Input logic control of the most significant bit for coupled output of channel 3 and channel 7 @ MODE=0)
10	$N_{IN}5$ (IN3_1)	I	Input logic control of the output of channel 5 @ MODE=1 (Input logic control of the 2nd significant bit for coupled output of channel 3 and channel 7 @ MODE=0)
11	$P_{IN}6$ (IN3_0)	I	Input logic control of the output of channel 6 @ MODE=1 (Input logic control of the least significant bit for coupled output of channel 3 and channel 7 @ MODE=0)
12	$N_{IN}6$ (IN4_2)	I	Input logic control of the output of channel 6 @ MODE=1 (Input logic control of the most significant bit for coupled output of channel 4 and channel 8 @ MODE=0)
13	$P_{IN}7$ (IN4_1)	I	Input logic control of the output of channel 7 @ MODE=1 (Input logic control of the 2nd significant bit for coupled output of channel 4 and channel 8 @ MODE=0)
14	$N_{IN}7$ (IN4_0)	I	Input logic control of the output of channel 7 @ MODE=1 (Input logic control of the least significant bit for coupled output of channel 4 and channel 8 @ MODE=0)
15	$P_{IN}8$	I	Input logic control of the output of channel 8 @ MODE=1; Connect to the ground @ MODE=0
16	$N_{IN}8$	I	Input logic control of the output of channel 8 @ MODE=1; Connect to the ground @ MODE=0
17	EN	I	Control of drive output enable, 1=off, 0=on (50kΩ internal pull-up)
18	CLKEN	I	Control of clock enable, 1=clock disable, 0=clock enable (50kΩ internal pull-up)
19	NC	-	No connection.
20	ATHP	I	Control of active THP enable, 1=disable, 0=enable (50kΩ internal pull-down)
21	THP	O	Thermal protection output, open N-MOS drain
22	V_{SS}	-	Negative low voltage power supply (-5V)
23	$V_{FP}2$	-	Built-in floating gate drive power supply-2 for HV P-MOS of channel 5 through 8
24	$V_{FN}2$	-	Built-in floating gate drive power supply-2 for HV N-MOS of channel 5 through 8
25	$V_{NN}2$	-	Negative high voltage power supply for channel 5 through 8 (-100 to 0V)
26	$HV_{OUT}8$	O	High voltage output of channel 8

Table 19 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
27	$V_{PP}2$	-	Positive high voltage power supply for channel 5 through 8 (0 to +100V)
28	$HV_{OUT}7$	O	High voltage output of channel 7
29	$V_{NN}2$	-	Negative high voltage power supply for channel 5 through 8 (-100 to 0V)
30	$HV_{OUT}6$	O	High voltage output of channel 6
31	$V_{PP}2$	-	Positive high voltage power supply for channel 5 through 8 (0 to +100V)
32	$HV_{OUT}5$	O	High voltage output of channel 5
33	GND	-	Drive power ground (0V)
34	$HV_{OUT}4$	O	High voltage output of channel 4
35	$V_{PP}1$	-	Positive high voltage power supply for channel 1 through 4 (0 to +100V)
36	$HV_{OUT}3$	O	High voltage output of channel 3
37	$V_{NN}1$	-	Negative high voltage power supply for channel 1 through 4 (-100 to 0V)
38	$HV_{OUT}2$	O	High voltage output of channel 2
39	$V_{PP}1$	-	Positive high voltage power supply for channel 1 through 4 (0 to +100V)
40	$HV_{OUT}1$	O	High voltage output of channel 1
41	$V_{NN}1$	-	Negative high voltage power supply for channel 1 through 4 (-100 to 0V)
42	$V_{FN}1$	-	Built-in floating gate drive power supply-1 for HV N-MOS of channel 1 through 4
43	$V_{FP}1$	-	Built-in floating gate drive power supply-1 for HV P-MOS of channel 1 through 4
44	V_{DD}	-	Positive low voltage power supply (+5V)
45	CC0	I	Control of the least significant bit for drive current mode (50kΩ internal pull-up)
46	CC1	I	Control of the most significant bit for drive current mode (50kΩ internal pull-up)
47	MODE	I	1=8-channel 3-level with 2-input/ch, 0=4-channel 5-lelvel with 3-input/ch (50kΩ internal pull-up)
48	GND	-	Drive power ground (0V)
49	GND	-	Drive power ground (0V)
50	$P_{IN}1$	I	Input logic control of the output of channel 1 @ MODE=1; Connect to the ground @ MODE=0
51	$N_{IN}1$	I	Input logic control of the output of channel 1 @ MODE=1; Connect to the ground @ MODE=0
52	$P_{IN}2$ (IN1_2)	I	Input logic control of the output of channel 2 @ MODE=1 (Input logic control of the most significant bit for coupled output of channel 1 and channel 5 @ MODE=0)

8. Package Outline



Unit: mm

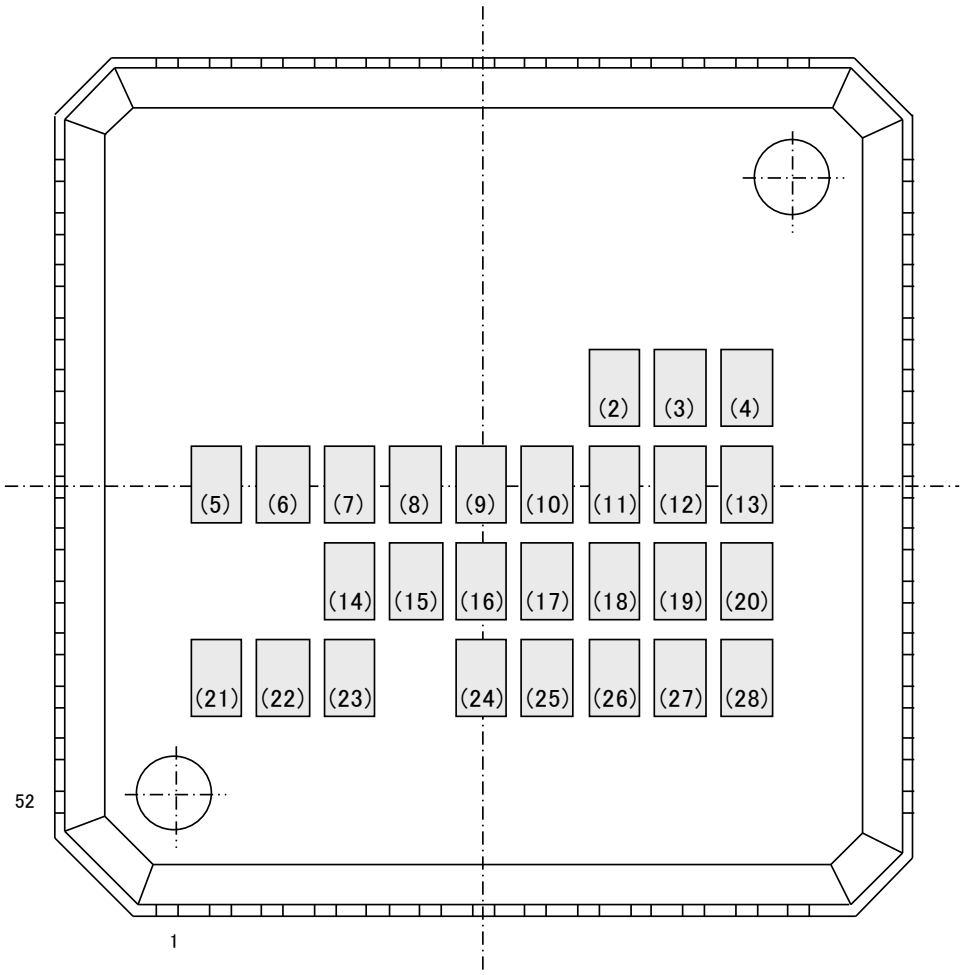
	MIN	TYP	MAX
A	—	—	0.95
A1	0.005	0.02	0.04
b	0.17	0.22	0.27
c	0.17	0.22	0.27
D, E	7.95	8.00	8.05
e	—	0.50	—
HD, HE	8.10	8.20	8.30
L	0.50	0.60	0.70
ZD, ZE	—	1.00	—

Note:

Exposed pad is electrically connected to chip ground. Attaching the pad to a ground plane ensures reliable operation of the device, and also helps reduce the junction temperature of the device that may be beneficial in high temperature environments.

Fig.11 Package Outline (52-Lead QFN Package)

9. Package Marking



No.	Code
(2)	Year sealed : the last one digit of the year
(3)	Month sealed : A~M (exc. " I ") in the order of Jan. to Dec.
(4)	Week sealed : 1~5
(5)~(13)	HDL6V5582 (product name)
(14)~(23)	Quality control code
(24)~(28)	Country of origin

Fig.12 Package Marking

10. Transport Media, Quantity

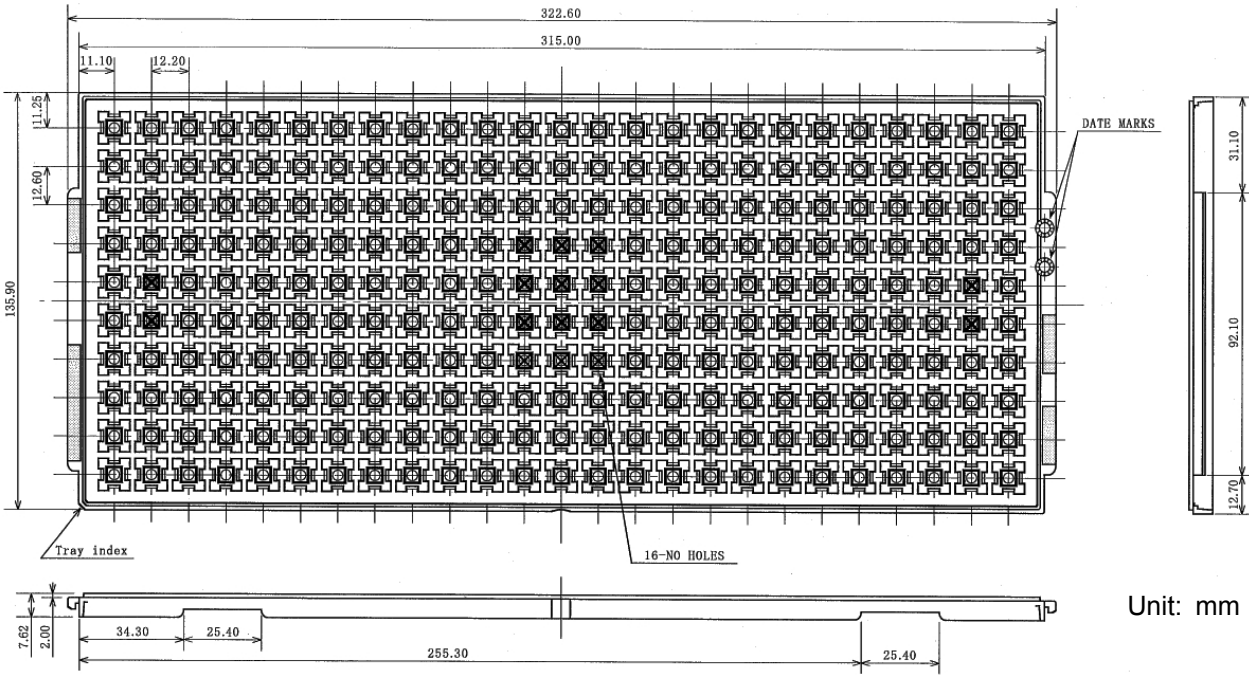
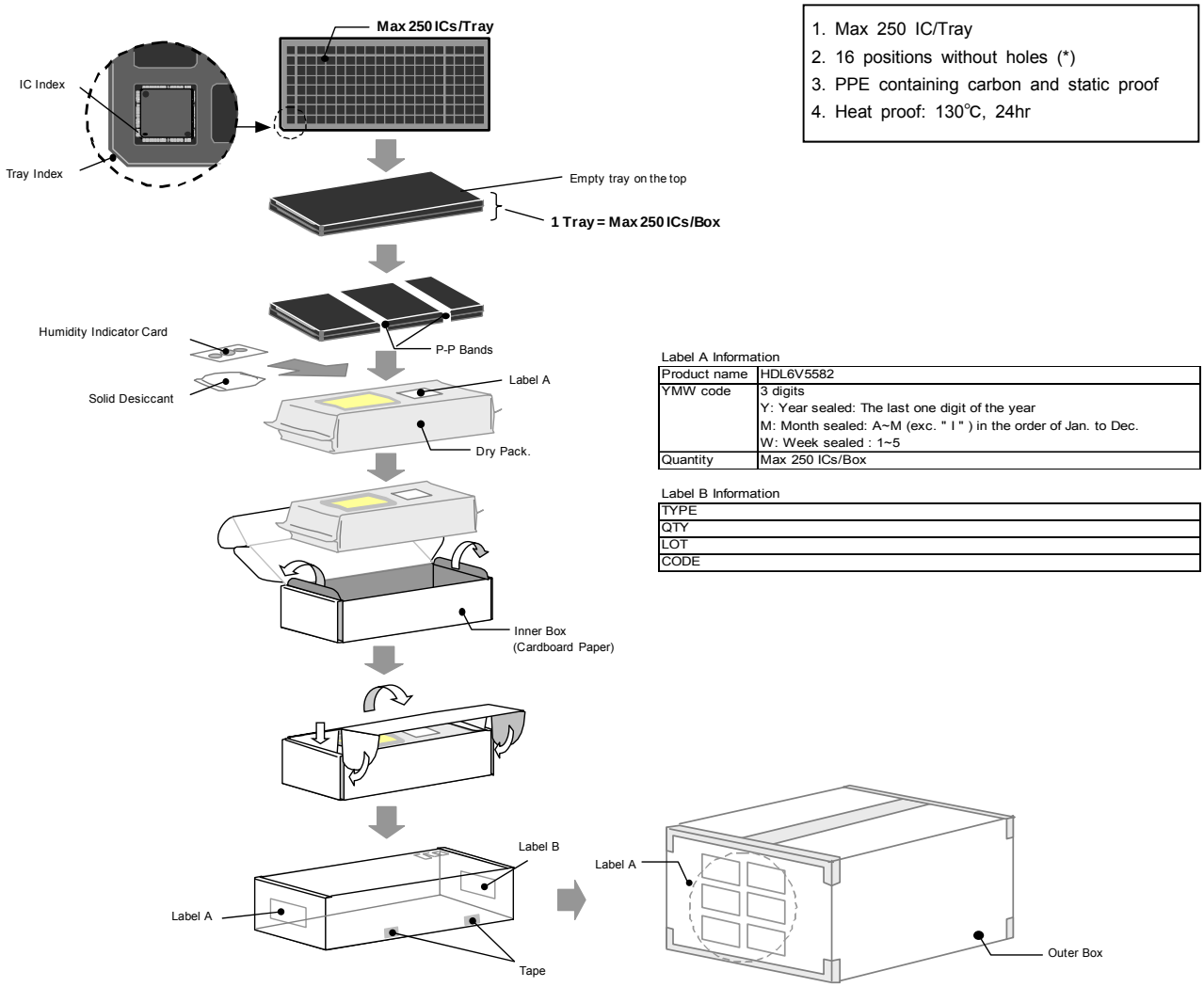


Fig.13 IC Tray Outline



1. Max 250 IC/Tray
2. 16 positions without holes (*)
3. PPE containing carbon and static proof
4. Heat proof: 130℃, 24hr

Label A Information

Product name	HDL6V5582
YMW code	3 digits Y: Year sealed: The last one digit of the year M: Month sealed: A~M (exc. " I ") in the order of Jan. to Dec. W: Week sealed : 1~5
Quantity	Max 250 ICs/Box

Label B Information

TYPE
QTY
LOT
CODE

Fig.14 Transport Media, Quantity

11. Mounting, Storage

11.1 Mounting Pad Design Example

Unit: mm

HE	8.20
HD	8.20
e	0.50
b3	0.32±0.05
L2	0.55±0.05
L1	0.20±0.05

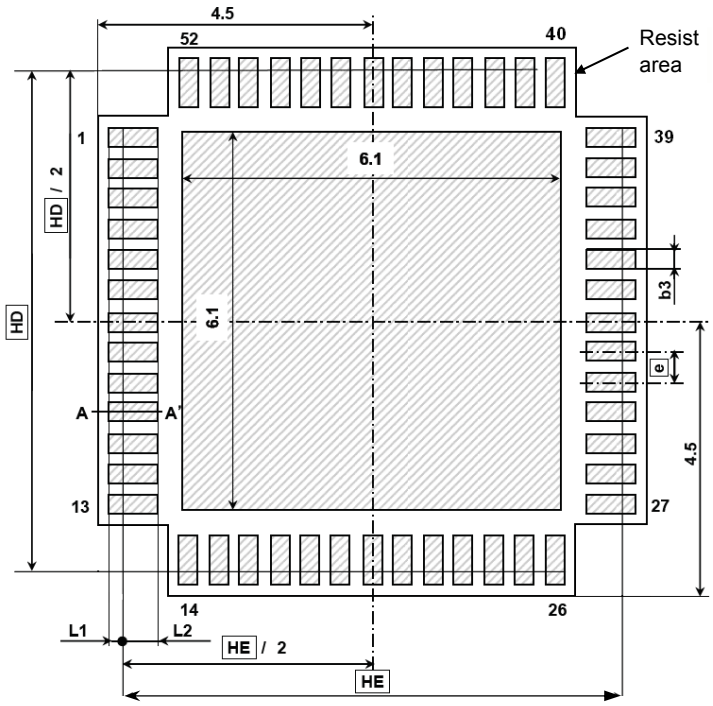


Fig.15 Mounting Pad Design Example

11.2 Storage Conditions

11.2.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

11.2.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking, or within 10 days of total exposure after the second dehumidification.

11.3 Reflow Conditions

Typical full heating methods such as Infrared (IR), Hot air, and N2 reflow process are applicable. IR/Air reflow heating conditions are shown below.

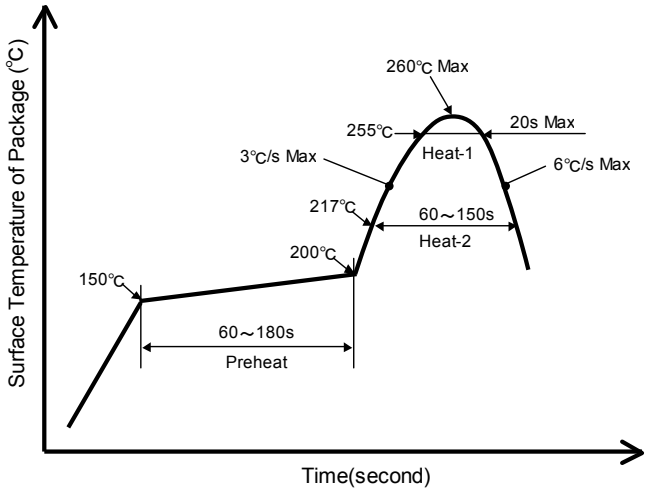


Fig.16 IR/Air Reflow Heating Conditions

12. Inspection

Hundred percent inspections shall be conducted on electrical characteristics.

13. Important Notice

13.1 ABLIC Inc. warrants performance of its hardware products (hereinafter called “products”) to the specifications applicable at the time of sale in accordance with the Product Specification. Testing and other quality control techniques are utilized to the extent ABLIC Inc. i needs to meet specifications described in the Product Specification. Specific testing of all parameters of each device is not necessarily performed, except those mandated by related laws and/or regulations.

13.2 Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.

13.3 ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

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14. Cautions

14.1 Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

14.1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

14.1.2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.

14.1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

14.1.4 Prevent friction with other materials made with high polymer.

14.1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

14.1.6 Avoid dealing with or storing products in an extremely arid environment.

14.2 “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

14.3 Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

14.4 Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

14.5 Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

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   Prior consultation with our sales office is required when considering the above uses.
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   The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
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