TDA525X and TDA7255V Family

ASK/FSK Transceiver

Using CLKDIV Output of the TDA525X & TDA7255V Transceiver

Application Note

Revision 1.0, 2010-11-11

Wireless Sense & Control

Edition 2010-11-11

Published by
Infineon Technologies AG
81726 Munich, Germany

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Page or Item	**Subjects (major changes since previous revision)**
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Table of Contents

	Table of Contents	4
	List of Figures	5
	List of Tables	6
1	**Subject**	7
2	**PLL Architecture**	8
3	**CLKDIV Sources**	9
4	**CLKDIV Register Settings**	10
5	**Determining Harmonics with Respect to the CKLDIV Signal**	12
6	**Direct Conversion Systems**	13
7	**Analysis of Harmonics vs Duty Cycle of the CLKDIV Signal**	14
7.1	Duty Cycle of 50%	15
7.2	Duty Cycle of 50.5%	17
7.3	Duty Cycle of 50.4%	21
7.4	Duty Cycle of 50.26% vs 50.52%	24
8	**When using Higher Frequency CLKDIV Sources**	25
9	**Solution to the Problem if Higher Clock Signal are used in the Application**	26
10	**Conclusion**	27

List of Figures

Figure 1 TDA5255/TDA7255V Block Diagram . . . 7
Figure 2 PLL Architecture and local Oscillator Signals . . . 8
Figure 3 Programmable CLKDIV Blocks . . . 9
Figure 4 Down Conversion Blocks for the TDA525x/TDA7255V . . . 13
Figure 5 Harmonics of an Symmetrical Signal (τ of rise and fall time is 8ns) . . . 15
Figure 6 Symmetrical Signal odd Harmonics (τ of the rising and falling edge is 1.808% of T) . . . 16
Figure 7 No even Harmonics appear in the Case of absolute Symmetry . . . 16
Figure 8 All Harmonics of a unsymmetrical Signal with a Duty-cycle of 50.5% . . . 17
Figure 9 Minima and Maxima of the relative Average Value of each Harmonic . . . 18
Figure 10 Odd Harmonics associated to a Duty-cycle of 50% . . . 19
Figure 11 The relative Amplitude of the Odd Harmonics => Min at n=100; Max at n=200 . . . 19
Figure 12 Even Harmonics associated to a Duty-cycle of 50.5% . . . 20
Figure 13 First Maxima at n=100 and the second Minima at n=200 . . . 20
Figure 14 All Harmonics associated to a Duty-cycle of 50.4% . . . 21
Figure 15 Odd Harmonics with a Minima at n=125 . . . 21
Figure 16 Relative Amplitude of odd Harmonics with a Periodicity of 250 . . . 22
Figure 17 Even Harmonics with a clear Minimum at n=250 . . . 22
Figure 18 Relative Amplitude of even Harmonics, Periodicity of 250, first Maximum at n=125 . . . 23
Figure 19 Relative Amplitude, even Harmonics, D.-C.= ~50.26% vs. D.-C.= ~50.52% . . . 24
Figure 20 Relative Amplitude, odd Harmonics, D.-C.= ~50.26% vs. D.-C.= ~50.52% . . . 24
Figure 21 Quasi-Direct Conversion Receiver Front-End . . . 25
Figure 22 PCB Connection for Harmonic De-Coupling Capacitor . . . 26

List of Tables

Table 1 Sub Address Register 0Dxh: CLK_DIV 10
Table 2 CLK_DIV Output Selection 10
Table 3 CLK_DIV Setting 10

1 Subject

The receiver part of the TDA525X/TDA7255V transceiver is a kind of direct conversion receiver. Therefore one of the higher order even harmonics of the clock (CLKDIV) falls in band of the received RF. Under certain circumstances this could cause a reduction of the sensitivity, especially when using higher clock frequencies.

The TDA525x/TDA7255V series of transceivers provides a programmable clock output function from the CLKDIV output from pin 26. This output is programmable such that it can provide a buffered clock output that is derived from the reference oscillator running around 18 MHz. The clock output that is derived from the reference oscillator can also be a divided via a programmable clock divider, or the clock source can be switched to a 32 kHz clock, which is generated from an internal 32 kHz RC oscillator.

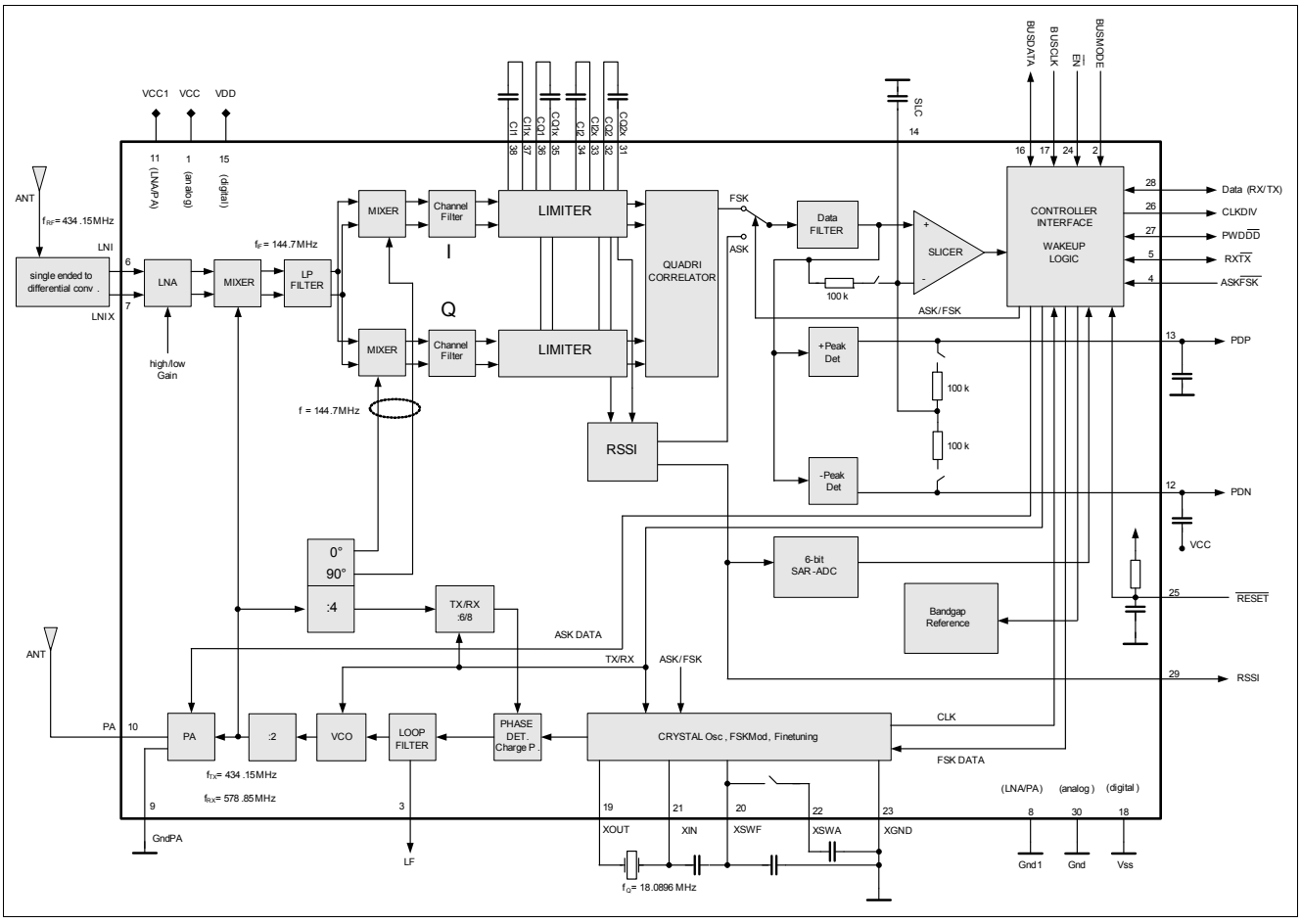

Figure 1 TDA5255/TDA7255V Block Diagram

2 PLL Architecture

When determining the crystal frequency for the transceiver one must observe the synthesizers within the Phase Lock Loop (PLL) path. The PLL architecture of the TDA525x/TDA7255V transceiver consists of two separate oscillators known as a Voltage Control Oscillator (VCO). One is used in transmit (TX) mode and the other is used in receive (RX) mode. The crystal frequency is determined by a division factor of the synthesizers in the path between the Local Oscillator (LO) and the Phase Detector (PD). The fist divider block in the synthesizer path after the LO signal is a divide by 4, which is then followed by a divide by 6 block when in the TX mode (see **Figure 1**). The multiplication of the two dividers then yields a value of 24.

As a Result the Crystal Frequency is determined by

$$Crystal\ Frequency = \frac{RF\ Frequency\,(MHz)}{24} \tag{1}$$

$$Crystal\ Frequency = \frac{433.92\,MHz}{24} = 18.08\,MHz \tag{2}$$

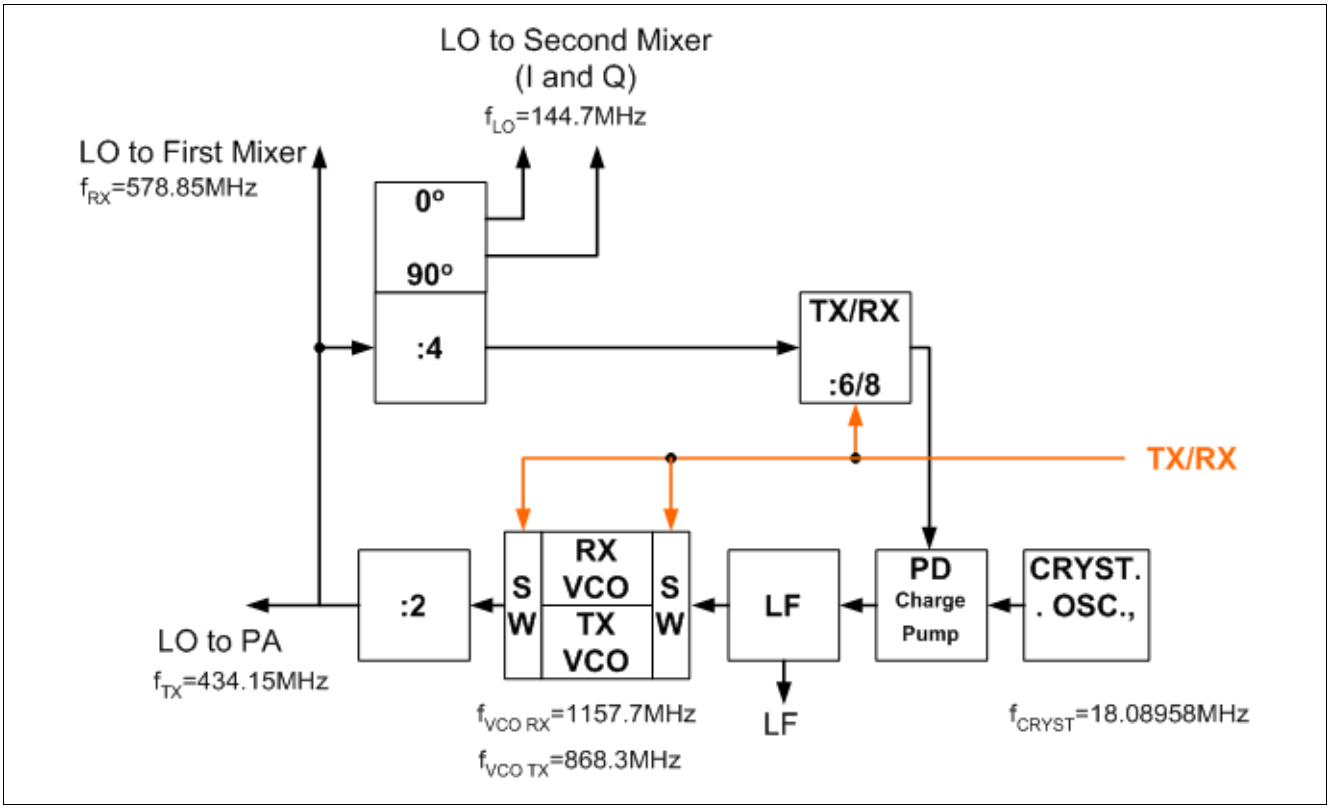

Figure 2 PLL Architecture and local Oscillator Signals

3 CLKDIV Sources

The clock sources from the CLKDIV block are all based upon an integer divider ratio from the reference oscillator (crystal oscillator) clock which is running around 18 MHz. Thus in the condition when there is an un-symmetrical clock source the even harmonics of the clock source, will then have a harmonic that falls in band if the clock source is derived from the reference oscillator. For instance, when using the TDA5255 or TDA7255V, and operating at 433.92 MHz the crystal oscillator would be 18.08 MHz. If a clock source from the CLKDIV is programmed to be 2.26 MHz, and there is a variation in the duty cycle then the 192nd harmonic falls directly in band. This is because the quasi direct conversion receiver is also locked to the same 18.08 MHz crystal clock via the PLL loop.

The CLKDIV source can be programmed to provide clock signals from 18 MHz to 32 kHz. Clock signals that are derived from the reference oscillator range from 18 MHz to 560 kHz.

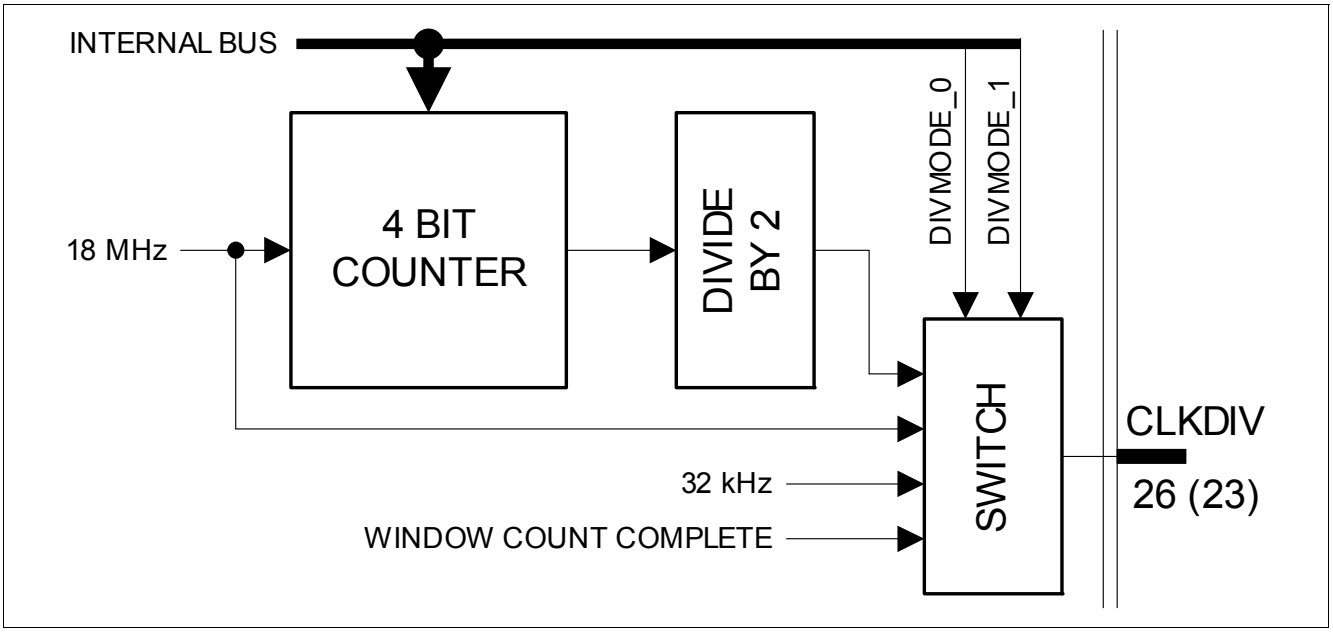

Figure 3 Programmable CLKDIV Blocks

4 CLKDIV Register Settings

The source of the CLKDIV is set via the Sub Address Register 0Dxh: CLK_DIV. The following default settings are seen in Table 1. These default settings provide the divider value of 18 for the CLKDIV output. This divider value yields a CLKDIV output that is approximately 1 MHz depending upon the crystal frequency used in the application.

Table 1 Sub Address Register 0Dxh: CLK_DIV

Bit	Function	Default
D7	Not used	0
D6	Not used	0
D5	DIVMODE_1	0
D4	DIVMODE_0	0
D3	CLKDIV_3	1
D2	CLKDIV_2	0
D1	CLKDIV_1	0
D0	CLKDIV_0	0

The bit settings in Table 2 determine the source of the CLKDIV output.

Table 2 CLK_DIV Output Selection

D5	D4	Output
0	0	Output from Divider (default)
0	1	Buffered Crystal Frequency
1	0	32 kHz
1	1	Window Count Complete

When using the clock divider the clock frequencies in Table 3 from the CLKDIV output can be programmed with the following bit settings.

Table 3 CLK_DIV Setting

D3	D2	D1	D0	Total Divider Ratio	Output Frequency (MHz)
0	0	0	0	2	9.0
0	0	0	1	4	4.5
0	0	1	0	6	3.0
0	0	1	1	8	2.25
0	1	0	0	10	1.80
0	1	0	1	12	1.50
0	1	1	0	14	1.28
0	1	1	1	16	1.125
1	0	0	0	18	1.00 (default)
1	0	0	1	20	0.90
1	0	1	0	22	0.82
1	0	1	1	24	0.75

Table 3 CLK_DIV Setting (cont'd)

D3	D2	D1	D0	Total Divider Ratio	Output Frequency (MHz)
1	1	0	0	26	0.69
1	1	0	1	28	0.64
1	1	1	0	30	0.60
1	1	1	1	32	0.56

5 Determining Harmonics with Respect to the CKLDIV Signal

The Nth harmonics that are in band can be calculated as follows

$$N^{th}\ Order\ Harmonics = \frac{RF\ Frequency}{CLKDIV\ Frequency} \tag{3}$$

The CLKDIV frequency is derived from programmable positive integer values from 2 to 32 (see Table 3)

$$CLKDIV\ = \frac{18.08\,MHz}{Clock\ Divider\ Ratio} = 560\,kHz\ to\ 9\,MHz \tag{4}$$

For example the ratio for a clock output of 2.26 MHz is

$$CLKDIV = \frac{18.08\,MHz}{8} = 2.26\,MHz \tag{5}$$

The crystal frequency is calculated as follows

$$Crystal\ Frequency = \frac{RF\ Frequency\ (MHz)}{24} \tag{6}$$

For example the TDA5255 transceiver is operating at 433.92 MHz, the crystal frequency is determined by

$$Crystal\ Frequency = \frac{433.92\,MHz}{24} = 18.08\,MHz \tag{7}$$

Then the in-band harmonic is determined by

$$N^{th}\ Order\ Harmonics = \frac{433.92\,MHz}{2.26\,MHz} = 192.00 \tag{8}$$

The in-band harmonic can also be calculated directly by

$$N^{th}\ OrderHarmonics = PLL\ DividerFactor \times CLK\ DividerFactor = 24 \times 8 = 192 \tag{9}$$

6 Direct Conversion Systems

Due to the architecture of a direct conversion system, or a quasi direct-conversion system the reference oscillator is the same clock source that is used for the clock output and for the down conversion to zero baseband. Having an integer divider ratio means that one harmonic is always exactly at the same frequency as the RF. Only when the clock signal is absolutely symmetrical will the amplitude of the even harmonics will be zero.

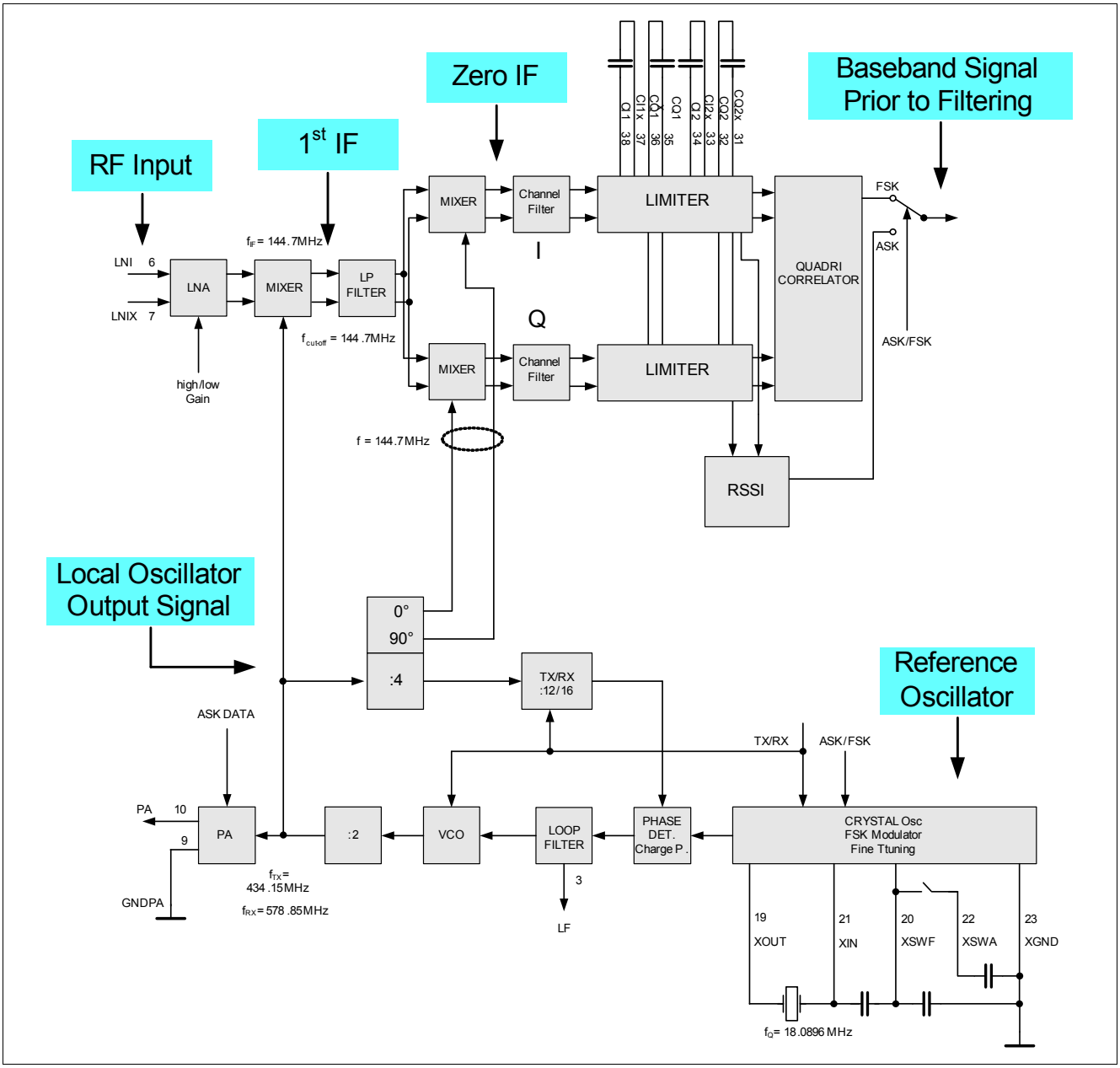

Figure 4 Down Conversion Blocks for the TDA525x/TDA7255V

Depending upon the frequency, the symmetry of the clock signal, the rising and falling edges of the clock signal, and PCB layout there could possibly cause a reduction in the sensitivity of the (direct-conversion) receiver. The sensitivity loss is usually only related to the higher frequency clock sources that are derived from the reference oscillator. The dependency associated to the PCB layout that can influence the coupling associated to long traces for the clock output signal, and poor ground plane under the transceiver and clock output circuits.

The loss in sensitivity occurs when in-band harmonics that are usually associated to the higher frequency clock signals that are derived from the reference oscillator are cross coupled to the front-end of the Low Noise Amplifier

(LNA) because of a poor PCB design. Depending upon the load and very slight variations in the duty cycle there can be a reduction in the sensitivity of the receiver section if higher frequencies clock sources are used. The slight change in the duty cycle will cause the even order harmonics, which are not present in the case of an absolutely symmetrical signal. When the PLL divider ratio is an even number, then it is only the even order clock harmonics that can act as a low energy interference source. The even order clock harmonics occur when there is a variation in the duty-cycle symmetry, and with variations in the rise and fall time associated to the clock edges. Normally the duty cycle is 50% for an ideal clock signal.

7 Analysis of Harmonics vs Duty Cycle of the CLKDIV Signal

Assuming the clock signal derived from the reference oscillator via the programmable clock divider (CLKDIV) is symmetrical there would theoretically be no even harmonics, and only odd harmonics. By describing a symmetrical clock signal this would be a clock signal with a duty cycle that is exactly 50%. This also infers that the rising and falling edges of the clock signal would be the same, or have the same time constant (**T**). In practice no clock signal will be absolutely symmetrical. One assumption is that even harmonics simply increase as a function of unsymmetry. This would consequently yield the demand of a design providing a clock signal as symmetrical as possible. Simulations show the real impact of a deviating duty-cycle from 50%, and how it impacts the harmonics. This simulations show that the correlations are not as simple as the assumption mentioned above.

The ideal clock signal would have a duty cycle of 50%, and spectral emission from the clock source would only consist of odd harmonics. For a perfectly symmetrical waveform, i.e. 50% duty cycle the amplitude of even order harmonics is theoretically zero. In practice these levels are well below the level of the odd-order harmonics, thus there is no interference issue associated to the even order harmonics that fall in-band.

The information in this section is simulated data based upon the following conditions

1. The RF Frequency = 433.92 MHz
2. Reference Oscillator = 18.08 MHz (due to a PLL-divider factor of 24)
3. CLK_DIV Setting = 8 (is the divider factor between the Reference Frequency and the Clock Output)
4. CLKDIV Frequency = 2.26 MHz (due to Clock Divider Factor of 8)
5. The Time Constant (**T**) is 8ns for the rising and falling edges. Consequently the **T** is equivalent to 1.808% of the period (T)
6. Harmonics plotted are from the 1st to the 250th harmonic.
7. The amplitude of the harmonics is in dB and relative to the 1st harmonic.

7.1 Duty Cycle of 50%

Figure 5 shows the amplitude of all harmonics from the 1st to the 250th harmonic. In this example the duty-cycle is exactly 50% and the time constant "τ" is the same for the rising and falling edges of the clock signal. The τ is set to 8 ns, which is 1.808% of the period (T).

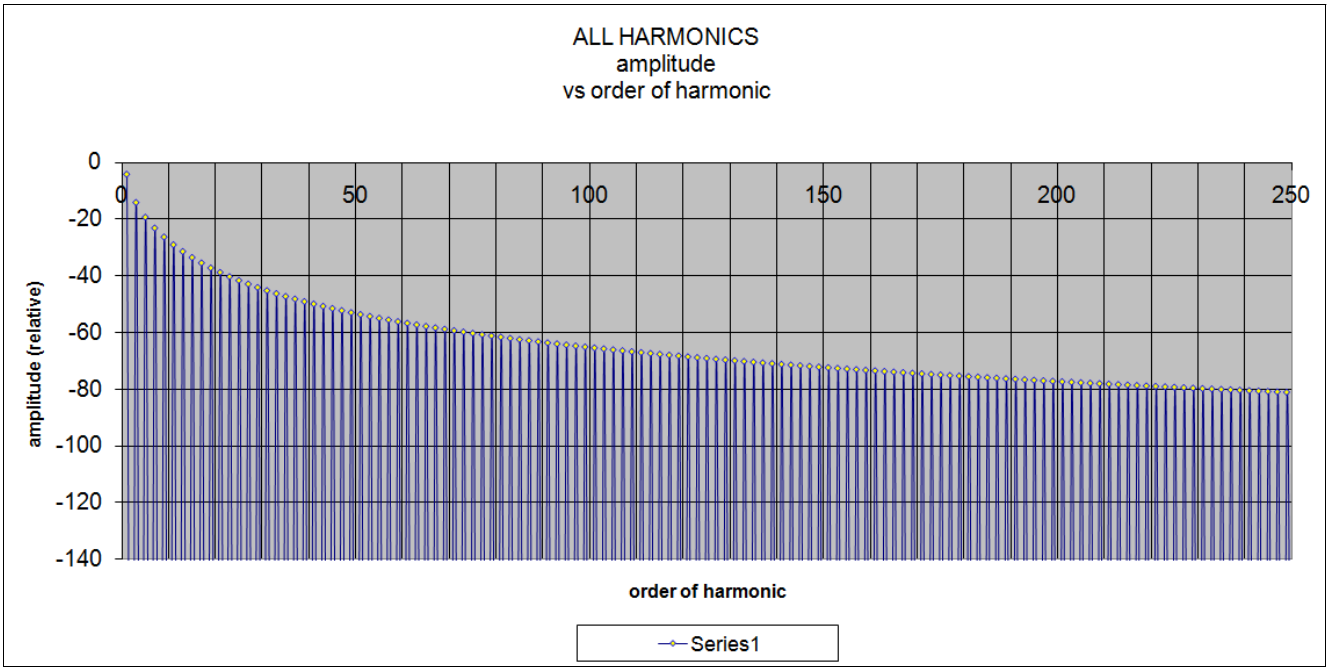

Figure 5 Harmonics of an Symmetrical Signal (τ of rise and fall time is 8ns)

Due to nature amplitude of the harmonic will decrease, as the order of the harmonic increases. One other noticeable factor is that the amplitude of the even harmonics is zero, which is to be expected for a symmetrical clock signal.

A more suitable way to demonstrate this effect is to split up the harmonics into plots of odd and even harmonics (see **Figure 6**: odd harmonics and **Figure 7**: even harmonics)

Note: In the case of total symmetry all EVEN HARMONICS are zero (-dB)!

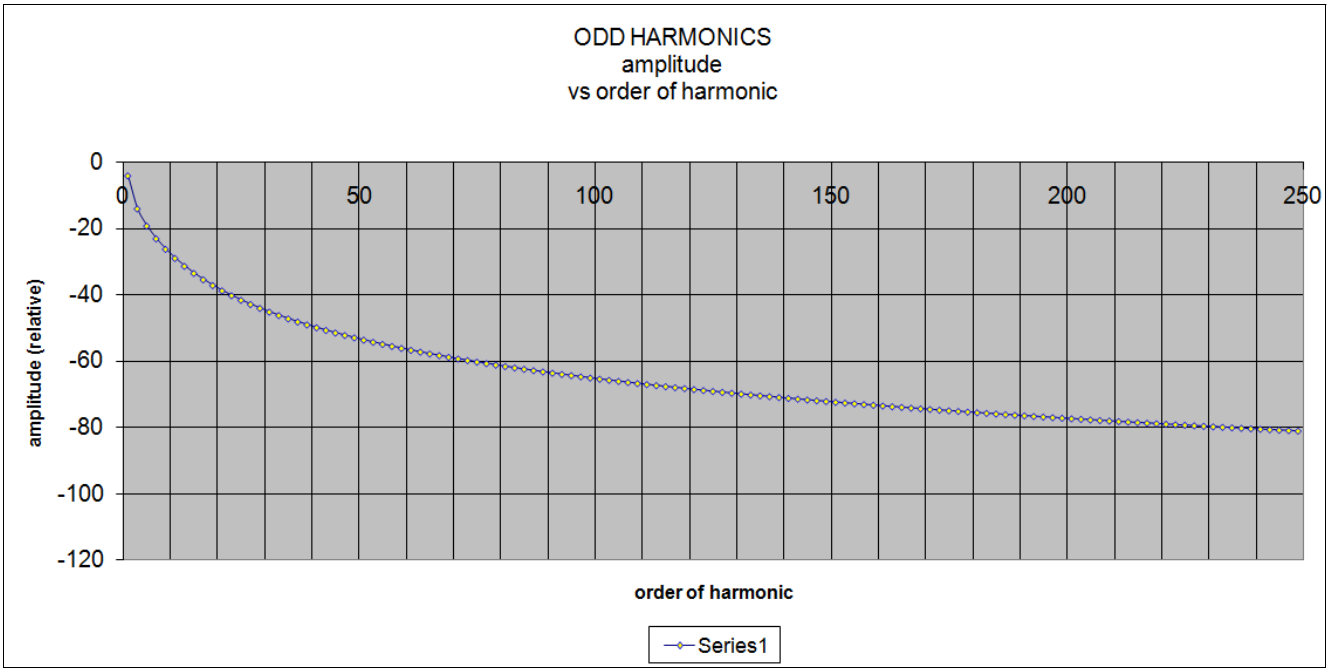

Figure 6 Symmetrical Signal odd Harmonics (τ of the rising and falling edge is 1.808% of T)

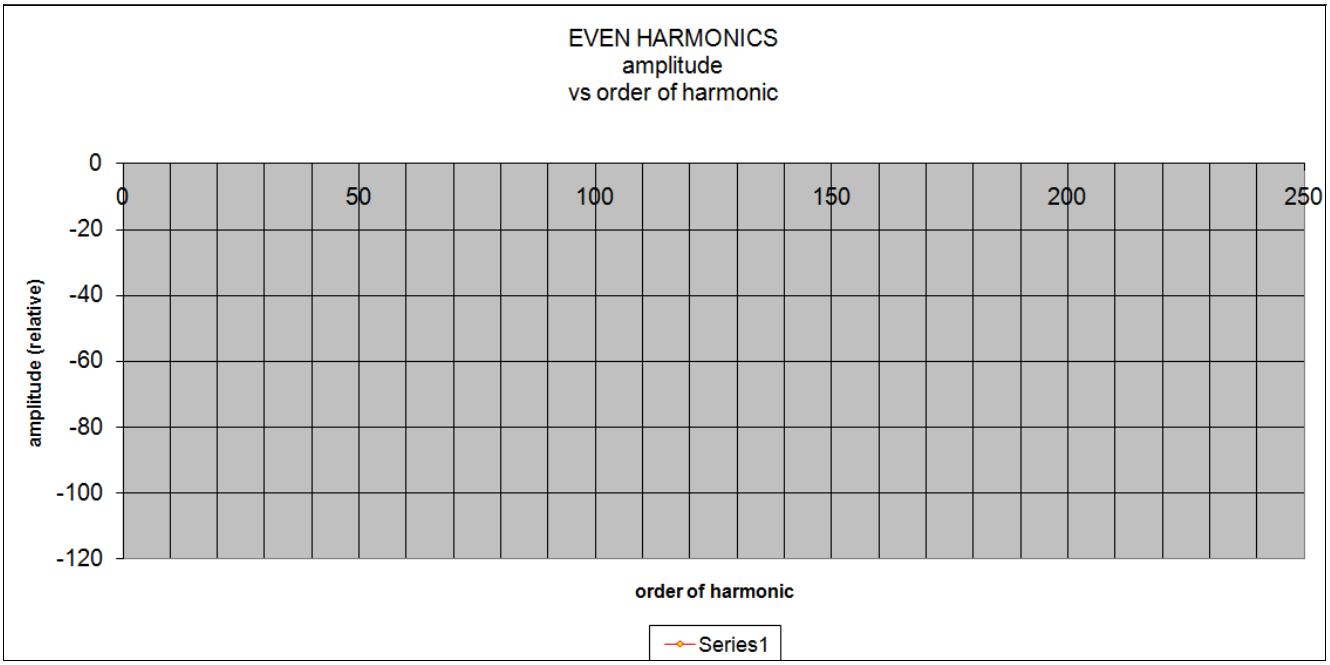

Figure 7 No even Harmonics appear in the Case of absolute Symmetry

7.2 Duty Cycle of 50.5%

Figure 8 shows both the calculated odd and even harmonics of a signal with a slight asymmetry, which means a duty-cycle of 50.5%. The T of the rising edge is again 8 ns and equal the T of the falling edge and thus the same as in the first example.

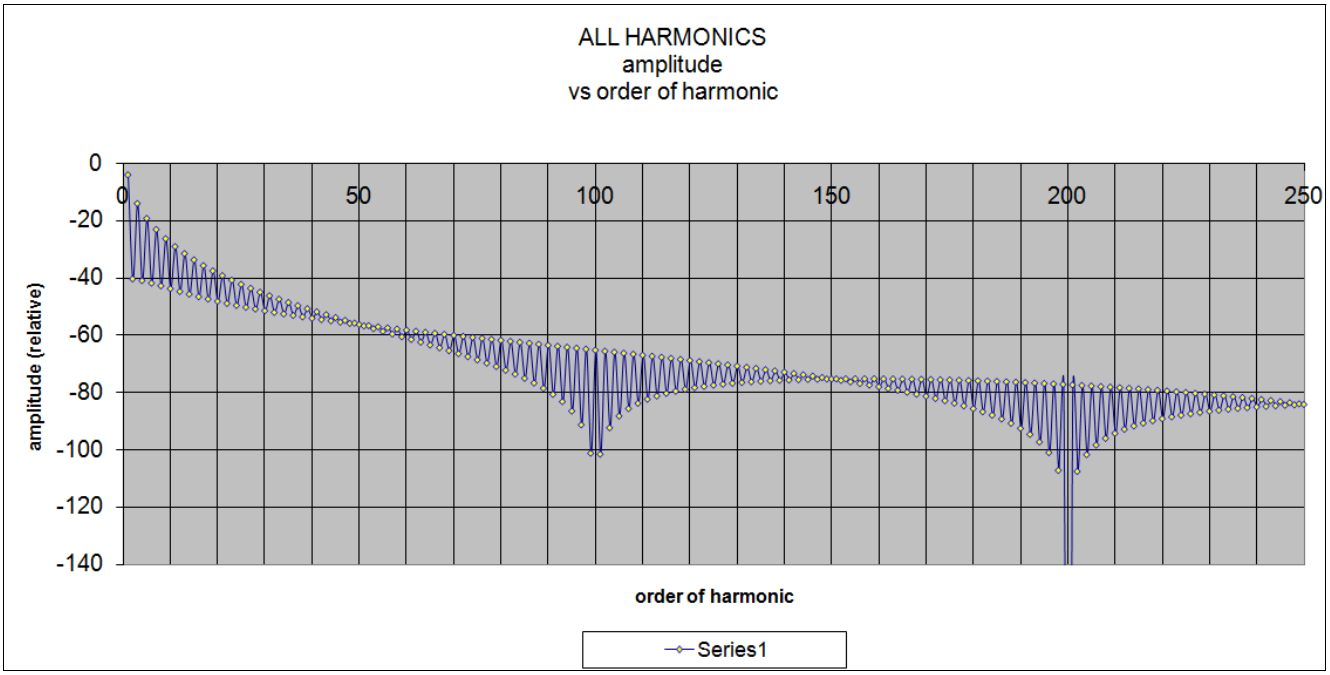

Figure 8 All Harmonics of a unsymmetrical Signal with a Duty-cycle of 50.5%

Now with the introduction of the asymmetry in the clock signal the even harmonics appear. One fundamental finding is that the amplitude of the even and odd harmonics do not simply decrease with the increasing order of the harmonics, but show a relative minima and maxima, with a certain periodicity. The periodicity is dependent on the unsymmetry of the clock signal. In fact the periodicity is the inverse value of the unsymmetry. Consequently the amplitude of a certain harmonic does not generally increase with the degree of unsymmetry, but show a certain periodicity depending on the unsymmetry.

- In the case of a slight asymmetry the even harmonics are generated. The amplitude is more dependent on the n^{th} order of the harmonic in relation to the asymmetry.
- Both, the odd and the even harmonics will show relative minima and maxima.
- The periodicity of the maxima and minima associated to the harmonics are influenced by the unsymmetry of the clock signal
- The periodicity is the inverse value of the asymmetry of the Duty-Cycle.
- Example: Duty-Cycle 50,5% => Asymmetry 0,5% ↔ 0,005
  ⟶ Periodicity = 200

This can be demonstrated even better by calculating and representing the amplitude of the harmonics relative to the average of the respective harmonic and the immediate adjacent harmonics (see Figure 9).

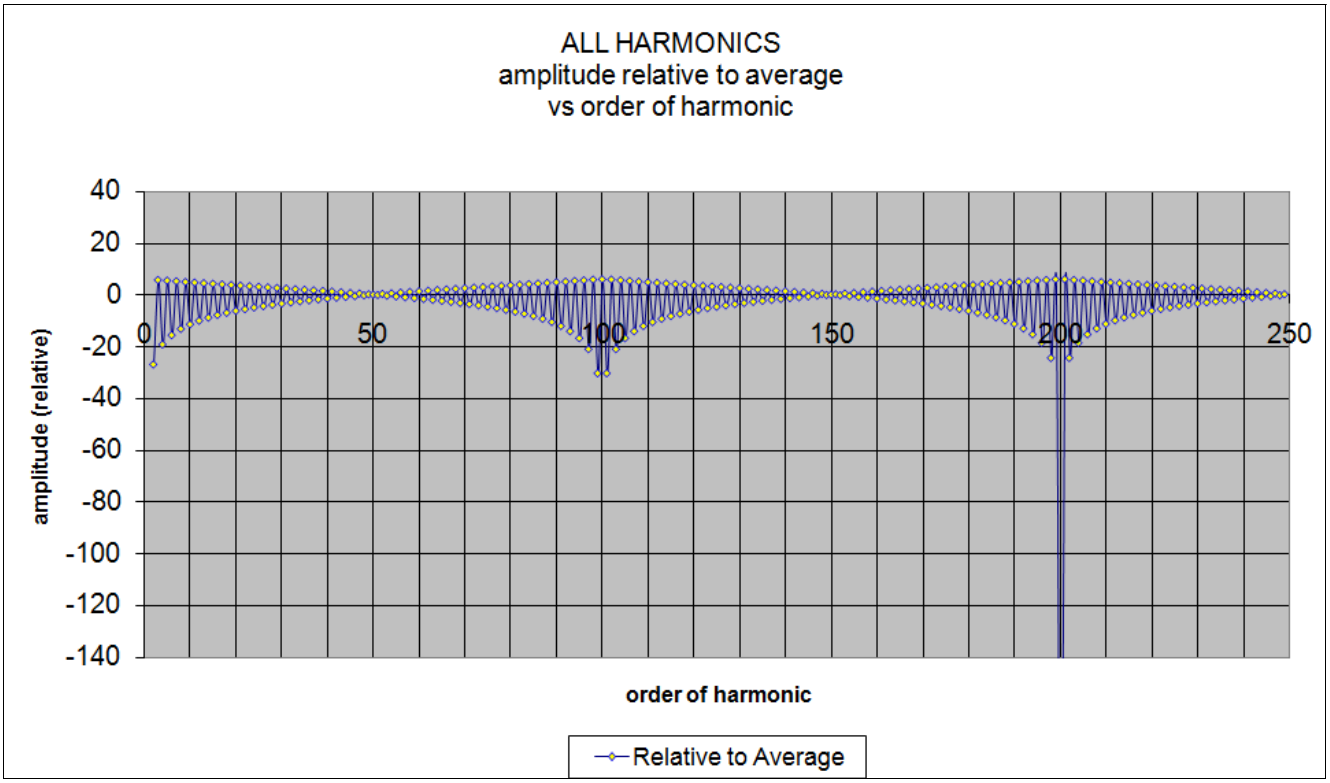

Figure 9 Minima and Maxima of the relative Average Value of each Harmonic

In this case the periodicity (cycle duration) of both the odd and even harmonics is 200 harmonics. As the asymmetry of a signal with a duty-cycle of 50.5% is 0.005 or 0.5%, we could expect that the periodicity is inverse value of the asymmetry. In fact this is the case and can be shown with the following examples.

For a better demonstration of the periodicity the odd harmonics are again plotted separately in **Figure 10** and **Figure 11**, and the even in **Figure 12** and **Figure 13**.

Figure 11 and **Figure 13** are additional emphasizing the relative minima and maxima of the harmonics relative to the average value as seen in **Figure 9**. **Figure 10** and especially **Figure 11** are showing clearly the first minimum of the odd harmonics at n=100 and the second maximum at n=200 (first at n=0), where “n” is the order of the respective harmonic. This condition is opposite for the even harmonics that are producing the first maximum at n=100 and second minimum at n=200 as seen in **Figure 12** and especially in **Figure 13**.

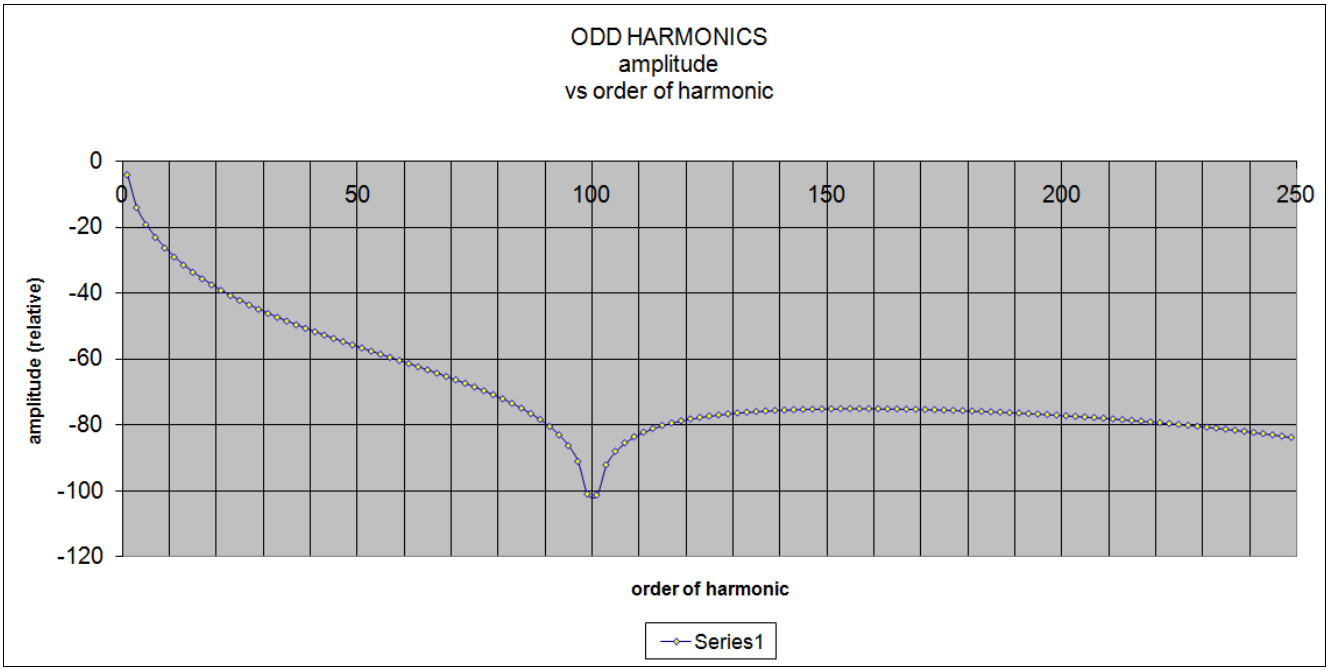

Figure 10 Odd Harmonics associated to a Duty-cycle of 50%

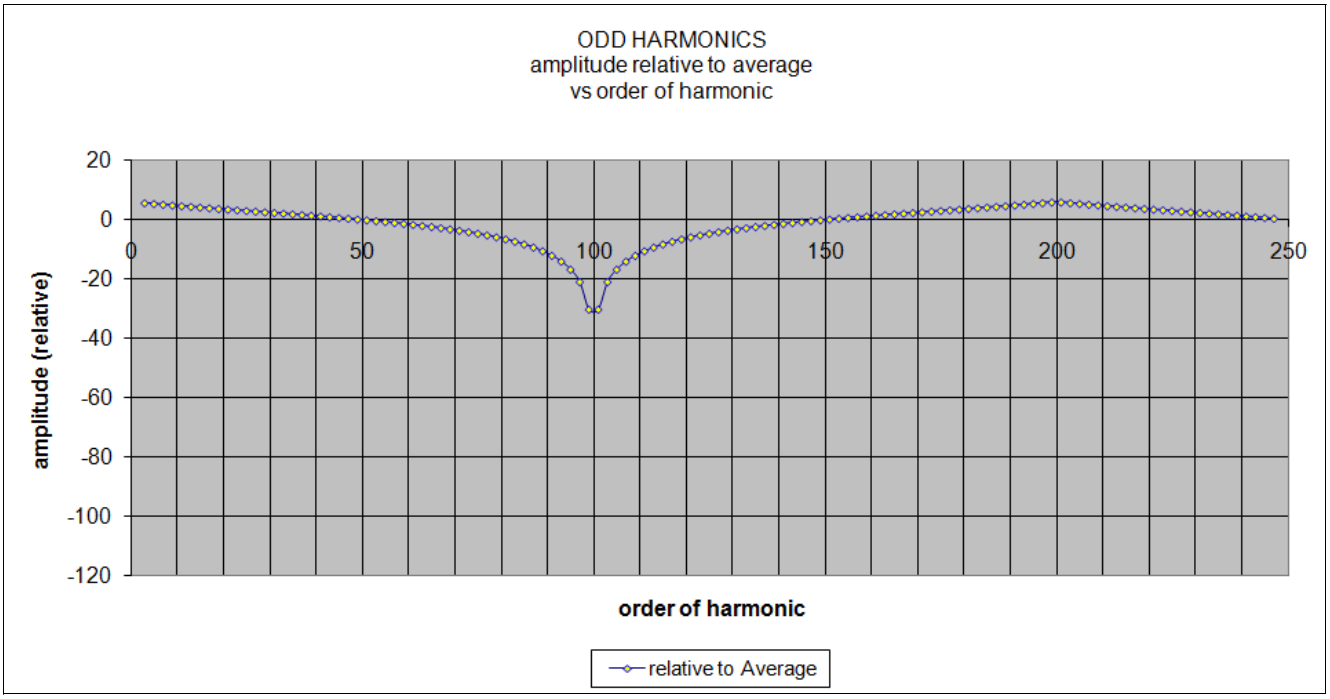

Figure 11 The relative Amplitude of the Odd Harmonics => Min at n=100; Max at n=200

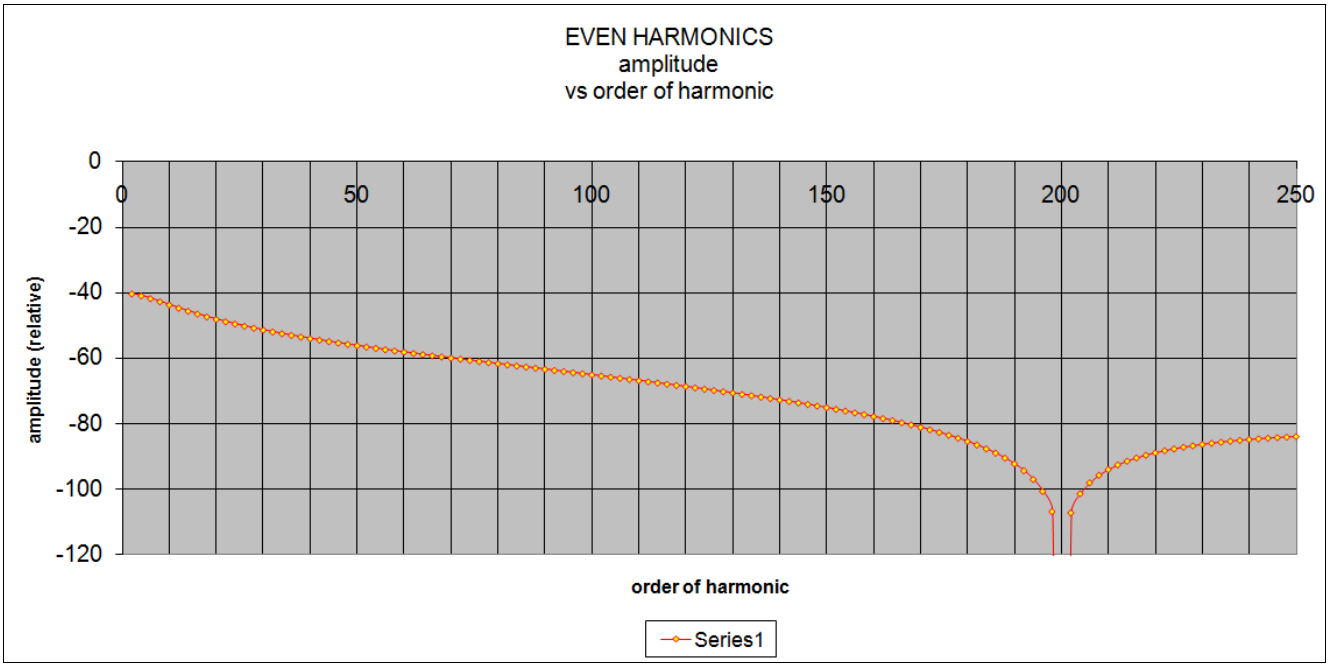

Figure 12 Even Harmonics associated to a Duty-cycle of 50.5%

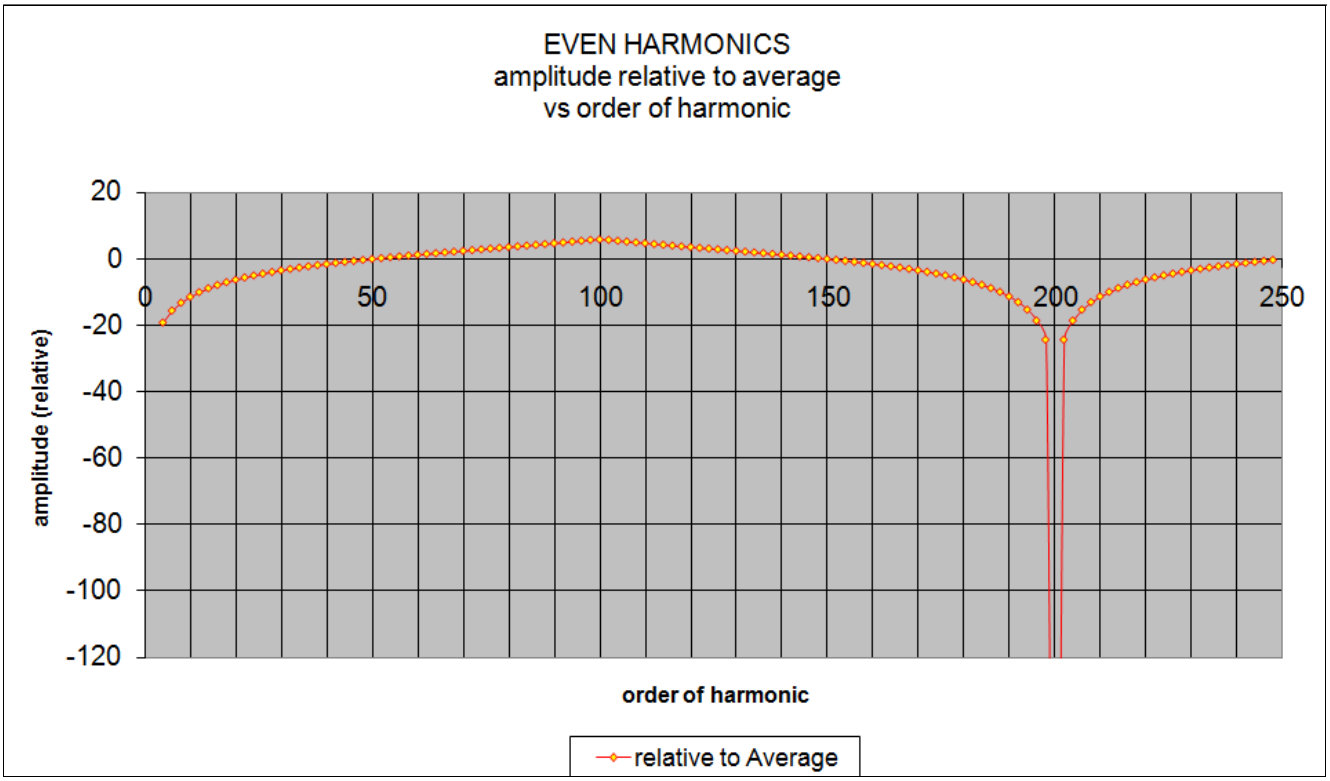

Figure 13 First Maxima at n=100 and the second Minima at n=200

7.3 Duty Cycle of 50.4%

Improving the symmetry of the clock signal by reducing the duty-cycle to 50.4% increases the periodicity of the maxima to the 240th harmonic. Although reducing the asymmetry yields a condition that is even worse for the example where the clock frequency is 2.26 MHz and RF frequency is 433.92 MHz. In case the second minima for the even harmonics is now located at the 250th harmonic, which is farther away from the interesting 192nd harmonic. This results yield a higher harmonic levels for the 192nd harmonic as compared to the condition when the duty cycle was 50.5%.

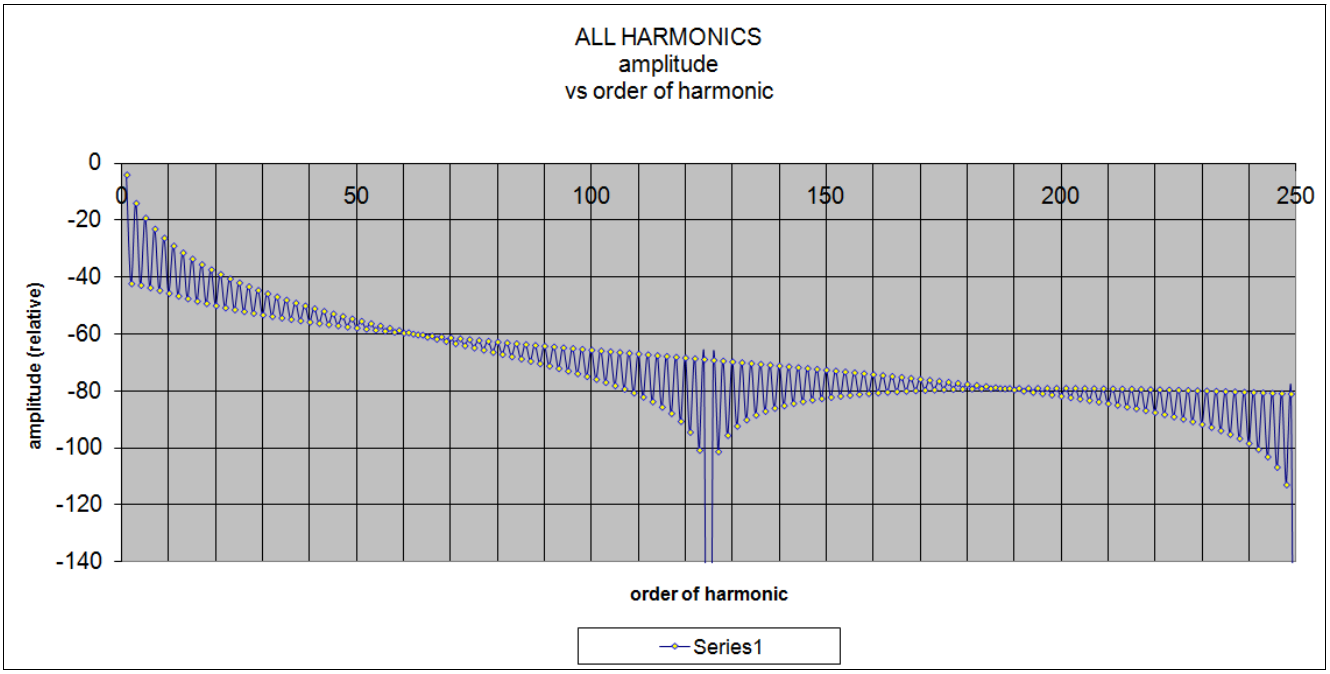

Figure 14 All Harmonics associated to a Duty-cycle of 50.4%

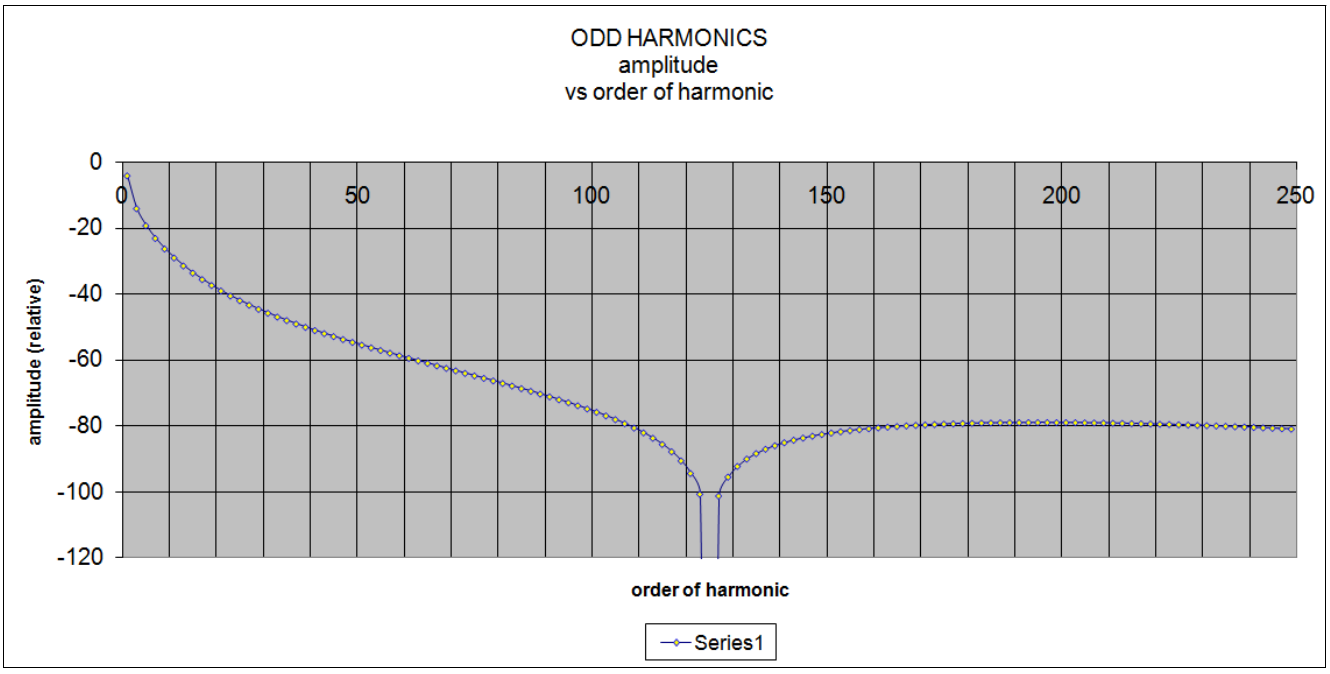

Figure 15 Odd Harmonics with a Minima at n=125

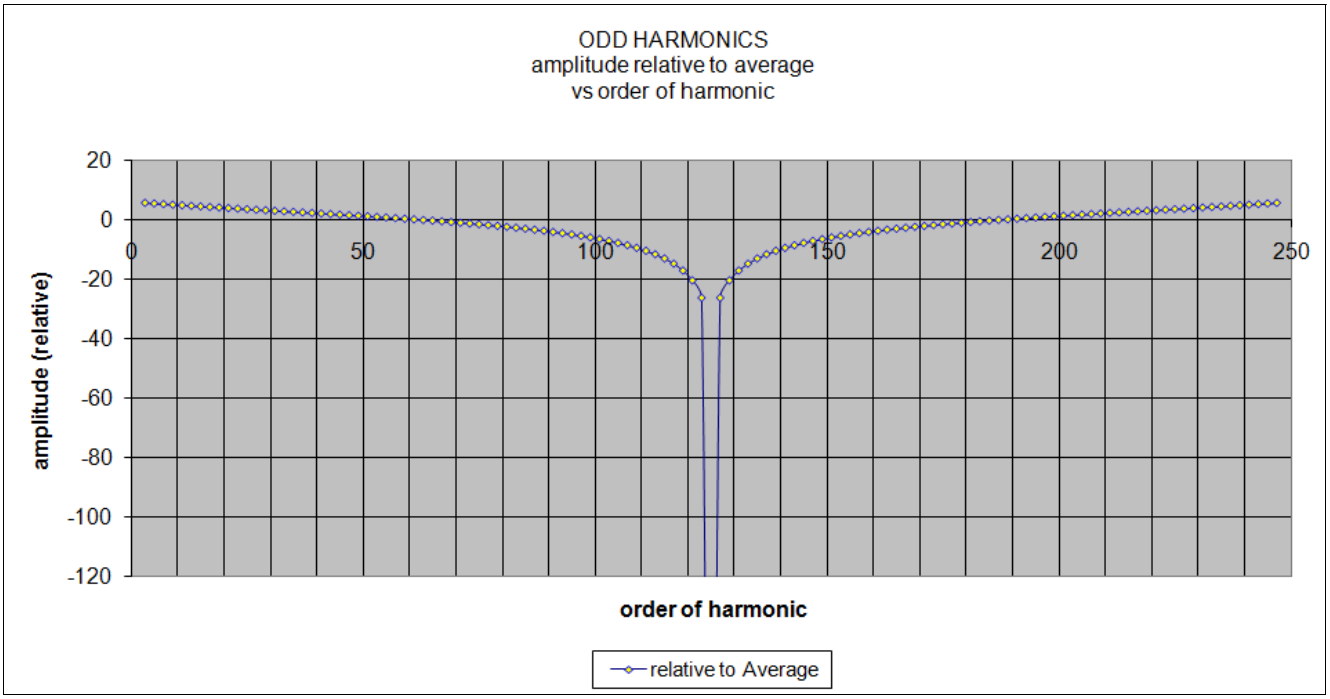

Figure 16 Relative Amplitude of odd Harmonics with a Periodicity of 250

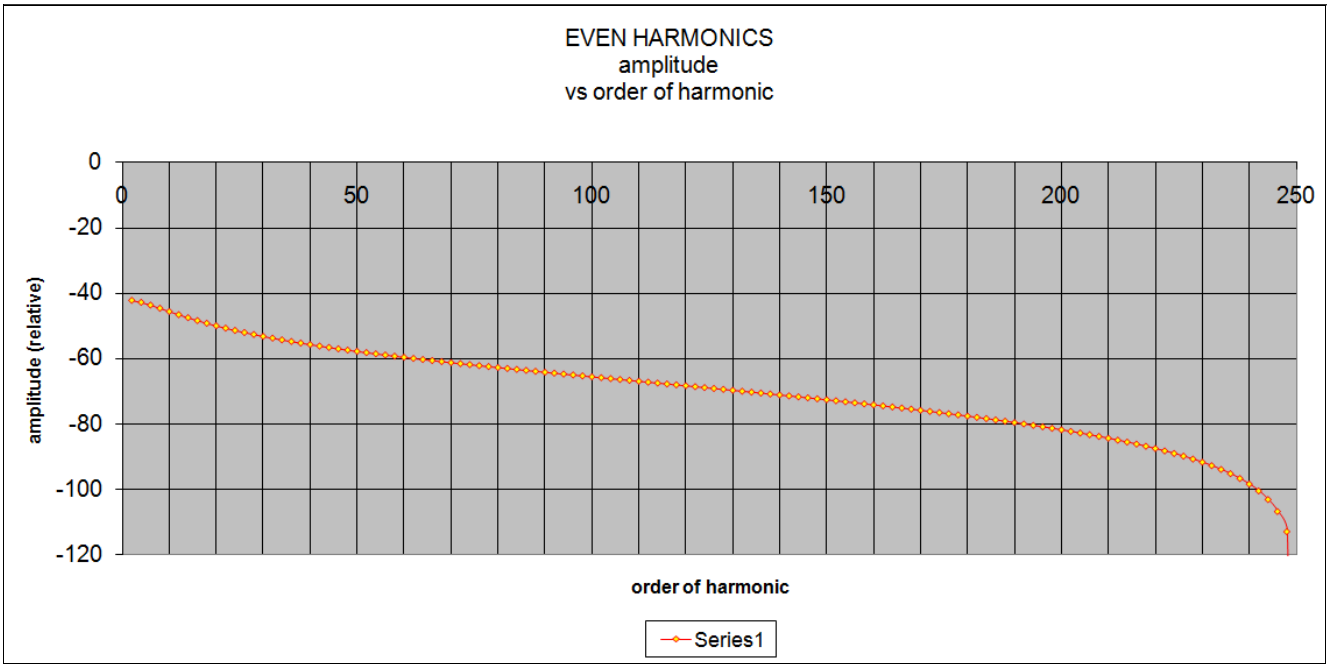

Figure 17 Even Harmonics with a clear Minimum at n=250

- In case of a slightly smaller asymmetry of 50.4% the even harmonics around the 192nd harmonic are even (~15 dB) higher than at the larger asymmetry of 50.5%.

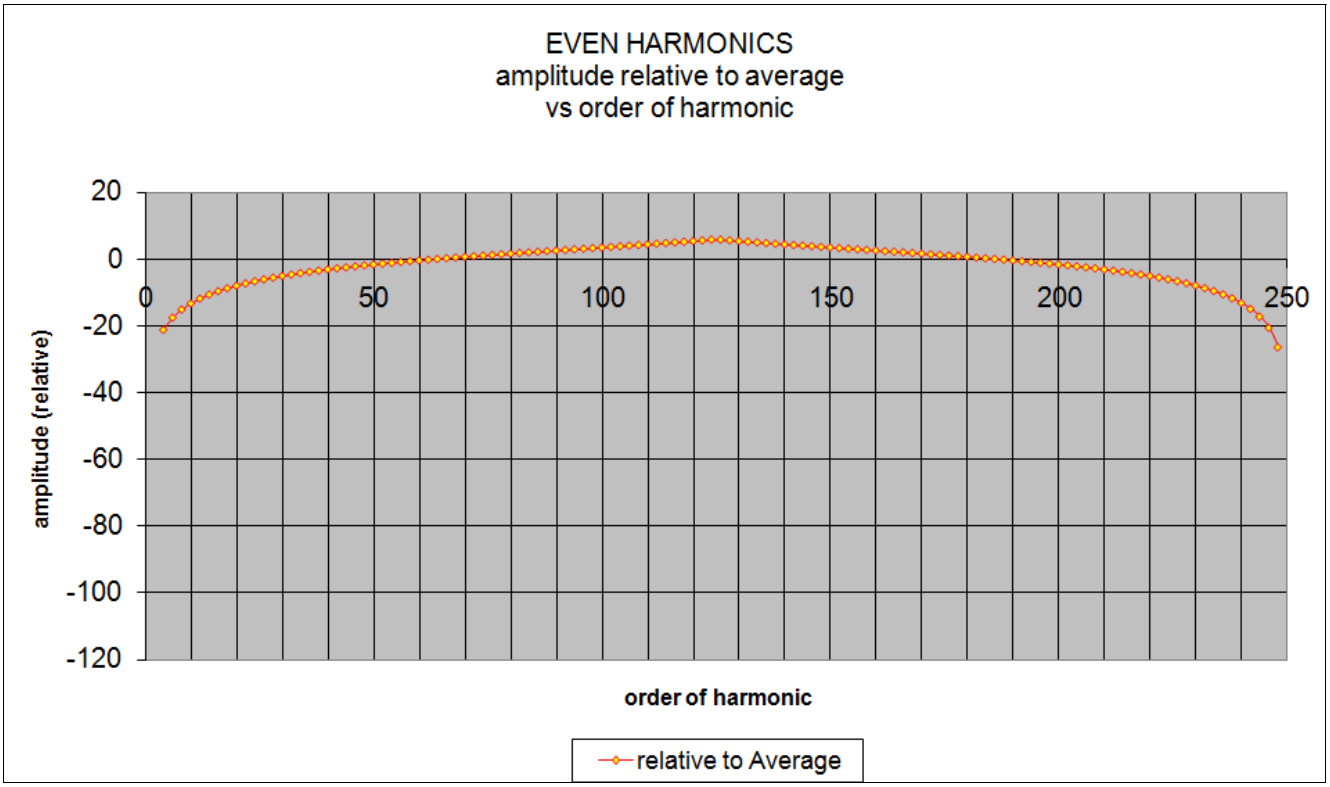

Figure 18 Relative Amplitude of even Harmonics, Periodicity of 250, first Maximum at n=125

7.4 Duty Cycle of 50.26% vs 50.52%

The periodicity is inversely proportional to the unsymmetry, and furthermore duty-cycle values that cause a minimum or maximum of the amplitude for any harmonic can be calculated (unsymmetry for max., of even harmonics 1/(2n)). In our example the 192nd harmonic is present at the same frequency as the RF. For this “even harmonic” it has been determined that the maximum level occurs when the duty-cycle is 50.2604%. It has also been identified that a maxima will occur at other duty-cycle values, but in the case of this example 0.2604% is the smallest unsymmetry that will produce a maxima at 192nd harmonic, or where n=192.

It has also been determined that 0,5208 is the smallest value of unsymmetry that yields a minima at the 192nd harmonic other than an unsymmetry of zero which is associated to a duty cycle of 50.00%.

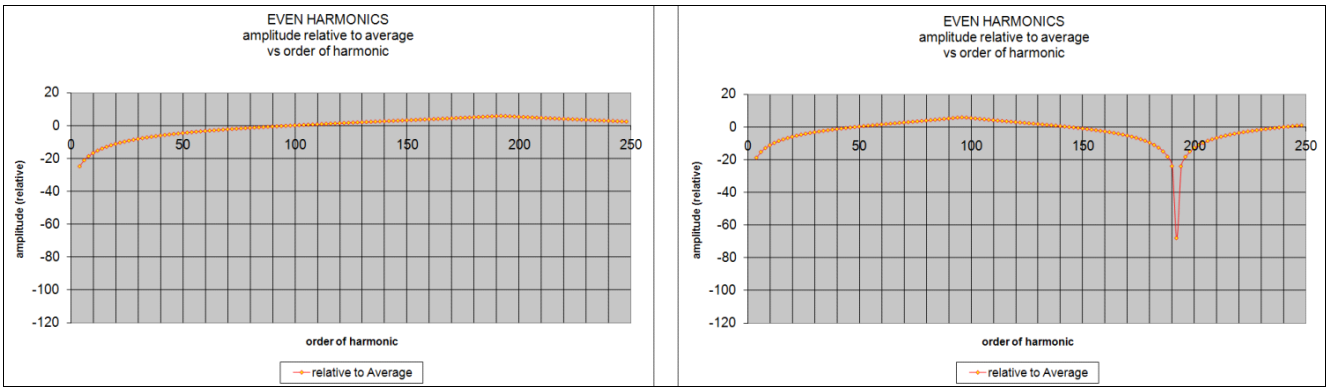

Figure 19 Relative Amplitude, even Harmonics, D.-C.= ~50.26% vs. D.-C.= ~50.52%

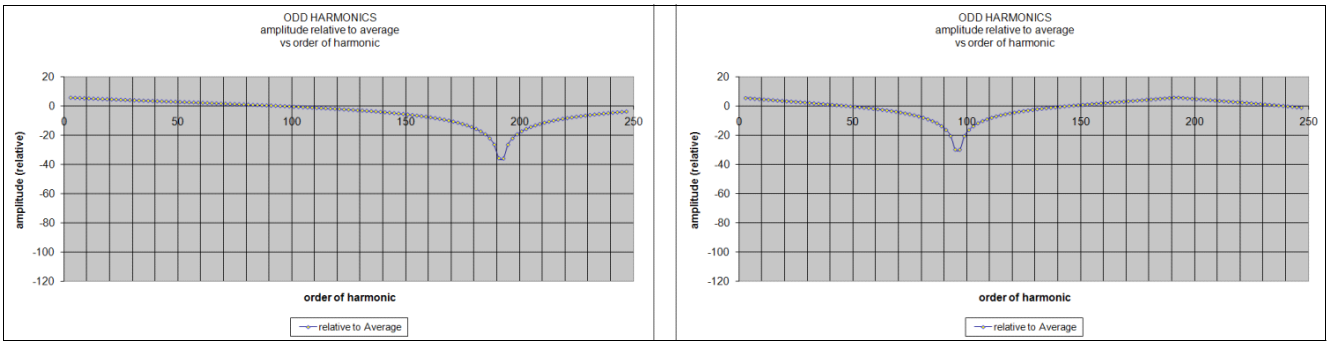

Figure 20 Relative Amplitude, odd Harmonics, D.-C.= ~50.26% vs. D.-C.= ~50.52%

8 When using Higher Frequency CLKDIV Sources

The architecture of the TDA525x/TDA7255V transceivers uses a quasi direct conversion system to down convert the wanted radio frequency (RF) to zero base band (see **Figure 21**). After the down conversion the I/Q signals are amplified via the Limiter Amplifier circuit (see **Figure 4**). The FSK I/Q signals are demodulated via Quadrature Correlator circuit. The signal path is selected for either the ASK or FSK demodulated signal and is further processed via the programmable base band filters with the Data Filter. The analogue signal is then converted to a digital signal via the Data Slicer circuit. The output of the Data Slicer is the processed signal which is then gated out via the Data pin 28 of the transceiver.

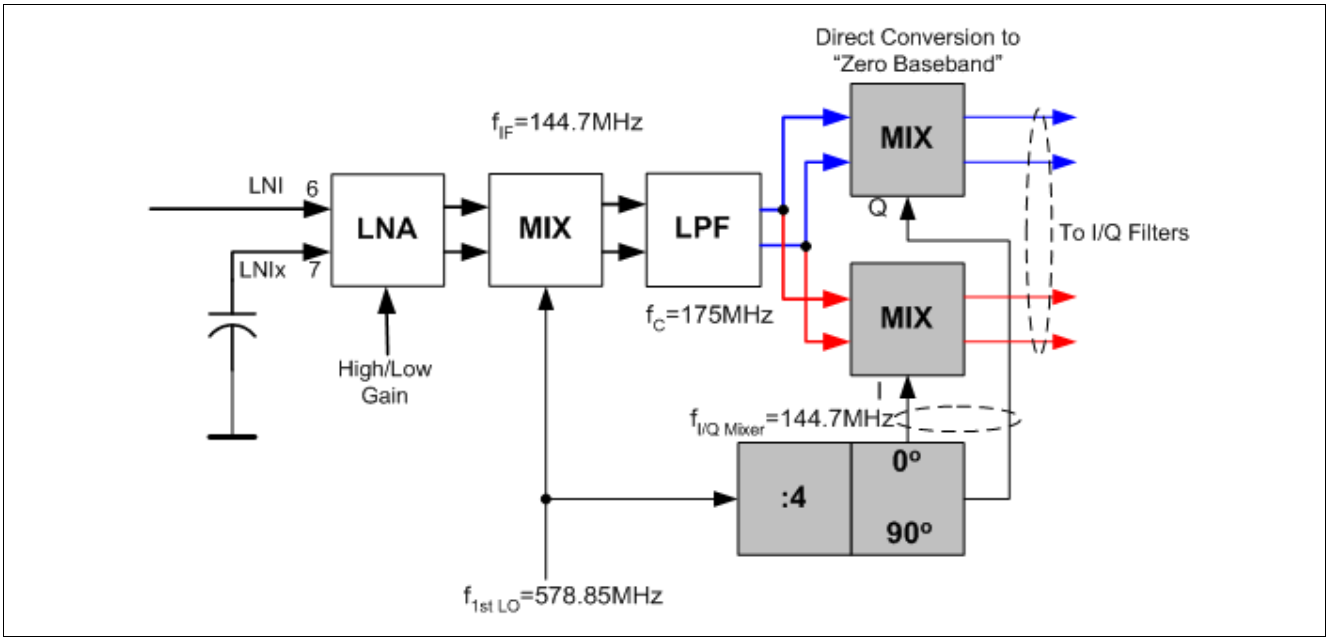

Figure 21 Quasi-Direct Conversion Receiver Front-End

Typically in-band harmonics associated to clock signals below 1.5 MHz do not have enough energy in the signal spectrum to cause any destructive interference to the wanted RF signal, but this is also dependent upon the application and layout. When using clock output frequencies that are higher than 1.5 MHz there is a chance of degradation in sensitivity that could be experienced while in the Receiver Mode. The degradation in sensitivity is due to harmonic emissions that have enough energy to generate an interferer signal on the LNA-input. This interferer signal must be in the range of the sensitivity level, or higher to cause any reduction in sensitivity. In general the higher the clock frequency the higher energy associated to the harmonic emissions that could fall in-band only if there are adverse variations in the duty cycle. Generally higher order harmonics from the clock signals, for instance, tends to result in less energy associated to them. When using the 32 kHz oscillator the spectral emission is dependent upon the exact RC clock frequency. The in band emissions for 433.92 MHz are at 13560th harmonic. These emissions are negligible, because these spectral components are well below thermal noise level of the receiver.

9 Solution to the Problem if Higher Clock Signal are used in the Application

The solution to reduce these emissions can be realized by adding a filter on the output of the CLKDIV pin 26 connected to ground. A low cost Low Pass Filter (LPF) can be implemented using a small value capacitor (2.7 pF to 47 pF) connected between the CLKDIV output and ground. The source impedance of the CLKDIV driver with the shunt capacitor will form the LPF. This connection should be between the node of the CLKDIV output and the load (i.e., micro clock input).

1. The capacitor should be located close to pin 26 of the TDA525x/TDA7255V transceiver as shown in **Figure 22**.
2. The ground connection should be made local to the ground pin 30.
3. In an ideal PCB design a complete ground plane is established on the bottom side of the PCB. This provides a very good solution for Electromagnetic Compatibility (EMC) and protection against Electromagnetic Interference (EMI).
4. The shunt capacitor should be sized to only reduce the high frequency content within the CLKDIV output signal.
5. For CLKDIV signal below 1.5 MHz, as well at the 32 kHz clock there is usually no need to implement a shunt capacitor across the CLKDIV pin 26 and ground.

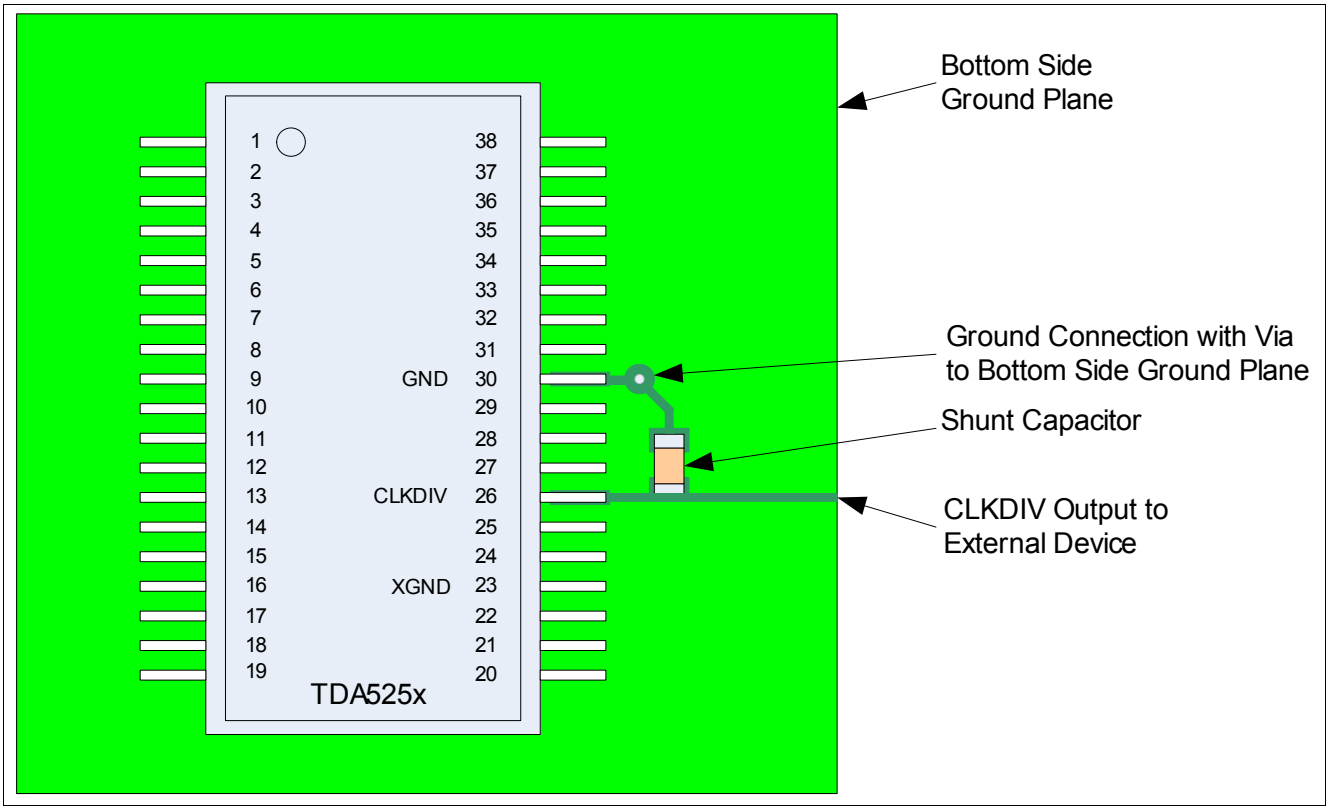

Figure 22 PCB Connection for Harmonic De-Coupling Capacitor

10 Conclusion

Facts

1. Generally the amplitude of any harmonic decreases with the order of the respective harmonic and increases with the steepness of the slope associated to the rising and falling edges of the clock signal.
2. The amplitude of the even harmonics does not simply increase with the degree of unsymmetry, but changes with the periodicity, whereas the amplitude of the odd harmonics does not simply decrease with the degree of unsymmetry. In fact the periodicity is the inverse value of the unsymmetry.
   a) Both odd and even harmonics show periodicity of relative minima and maxima.
   b) The cycle duration is inversely proportional to the value of unsymmetry for both odd and even harmonics
   c) The only difference is that the first maximum of the odd harmonics appear at n=0, whereas in case of the even harmonics the first minimum appears at n=0, assuming “n” is the order of harmonics. This is also the reason why odd harmonics and no even harmonics appear for an absolutely symmetrical signal.
3. Besides the unsymmetrical clock signal, other factors that can affect the amplitude of the N^{th} order harmonics are:
   a) The amplitude of the harmonics is strongly dependent upon the rise and fall time of the clock edges, and upon the amplitude of the clock signal. This is to say the emissions associated to the clock signals are lower for a lower supply voltage.
   b) The length of the PCB trance from the CLKDIV output (pin 26) to the load (micro).
   c) Variations in the load impedance that the CLKDIV driver is connected to.
   d) How the ground plane is implemented under the transceiver circuit and the clock output circuit.
   e) Temperature can cause load impedances to change thus have and influence on the symmetry of the clock signal.
   f) The other dependent factor is the frequency of the CLKDIV signal. Generally the amplitude of the in band interferer increases with a higher clock frequency from the CLKDIV output (greater than 1.5 MHz).

Consequences

1. As the periodicity (cycle duration) is the inverse of the unsymmetry the variation associated to the duty-cycle for a change of the amplitude from minimum to maximum is smaller for higher order harmonics than for lower order harmonics. For a harmonic of higher order a tiny change of the duty-cycle is sufficient for changing the amplitude of the respective harmonic from minimum to maximum.
2. Consequently only a slight change of the threshold of the output stage, or a tiny change of the symmetry of the load can yield considerable change associated to the amplitude for harmonics of the higher order.
3. This demonstrates that the amplitude of a higher order harmonic at the same frequency as the wanted channel (RF) could hardly be controlled by adjusting the symmetry, or unsymmetry of the clock signal.
   a) Therefore the selected clock frequency should be as low as possible. The higher the order of harmonic the lower the average of the amplitude for harmonics around the respective harmonic.
   b) Also the steepness of the slope of the rising and falling edge should be reduced to achieve the lowest acceptable value.
4. Higher clock signals can be used by implementing a simple LPF comprised of a shunt capacitor across the CLKDIV output at pin 26 to the ground of the transceiver local to pin 30. In this way the emissions associated to higher frequency clock signals can be easily reduced.
   a) To size up the capacitor one must consider parasitic capacitance associated to the PCB, and the tolerance of the device that is using the clock signal.
   b) The larger the capacitor value the greater the reduction in the high frequency energy that can be removed from the clock signal.
   c) The reduction of the rise and fall times of the clock signal must be verified in the application, such that the device using the clock signal has an acceptable edge to work with.
   d) Typical values can range from 2.7 pF to 47 pF, but should be evaluated in the PCB design.

Note: Both measures “3a.” and “3b.” will decrease the average value of the amplitude of the harmonics close to, or around the frequency of the RF.

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