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APPLICATION NOTE 6425

# THE BASICS OF USING THE MAX11254/MAX11259 24-BIT ADCS WITH INTEGRATED PGA FOR SENSOR-RICH APPLICATIONS

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*Abstract: Maxim's MAX11254 is a 24-bit ADC designed to tackle even the most challenging sensor designs by incorporating six differential channels, a 128x PGA, calibration functions, and three sequencing modes to automate any data acquisition system. This application note describes three application examples to help users maximize the MAX11254 functionality. For I<sup>2</sup>C systems, substitute the MAX11254 with the MAX11259.*

## Introduction

Sensors technology has recently exploded in the past couple years with the emergence of the Internet of Things (IoT). Bloomberg predicts the market for sensors integrated with processors will reach 2.8 trillion devices in 2019. Sensors are the next big thing and their integration requires an analog-to-digital converter (ADC) to convert the sensors' output into a digital format for processing. The improvement in sensor technology necessitates ADCs with higher functionality, incorporating high resolution, calibration abilities, embedded programmable gain amplifiers (PGAs), and multiple input channels to achieve one-chip solutions for sensor interfacing.

The [MAX11254/MAX11259](#) are highly integrated ADCs containing six differential analog inputs, a 6-channel multiplexer, a PGA, a delta-sigma modulator, and a digital filter. To accommodate applications that call for multiple inputs, three channel-sequencing modes are provided:

- **Mode 1** disables the sequencer and only permits single-channel conversions, allowing continuous sampling at the fastest sampling rate.
- **Mode 2** allows conversions on every channel in an automated user defined sequence.
- **Mode 3** simultaneously automates both the channel mux for conversion and the GPO/GPIO states.

This application note discusses the three sequencing modes to help designers maximize the full functionality of the MAX11254/MAX11259 ADCs. For systems requiring SPI communication, use the MAX11254. For systems using I<sup>2</sup>C communication, use the MAX11259. This application note will only show examples using the MAX11254, but the MAX11259 can be substituted in all applications given. **Figure 1** displays the MAX11254's functional diagram.

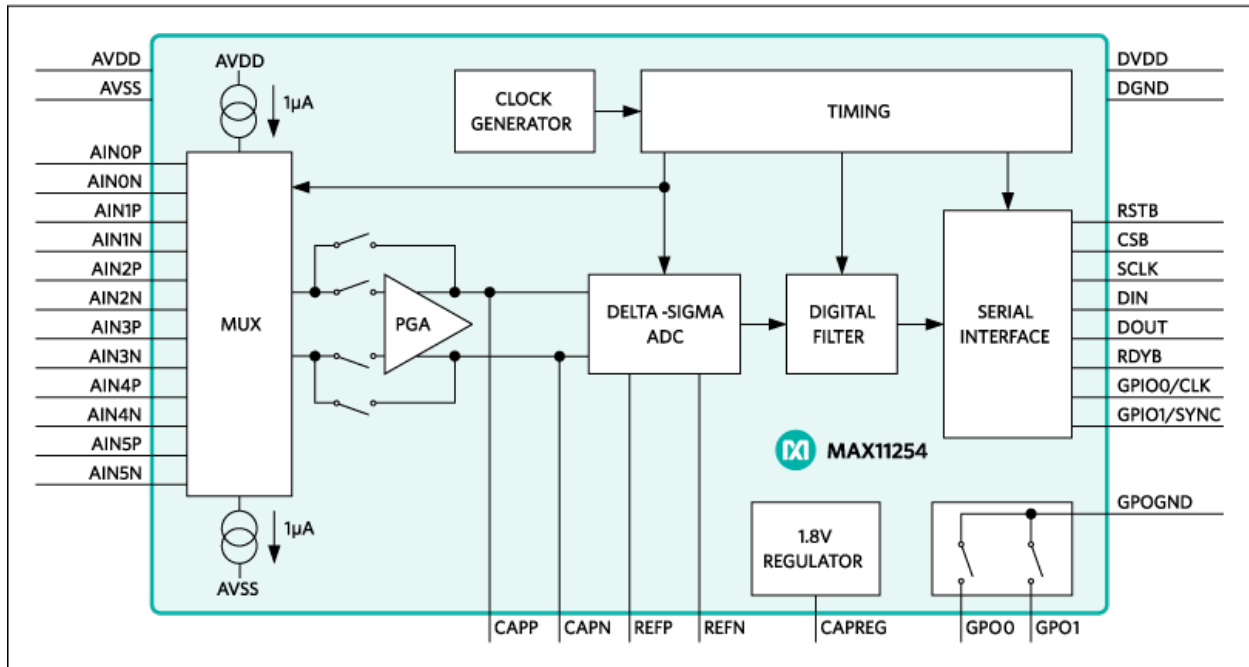


Figure 1. MAX11254 functional diagram.

### Application Example 1: Continuous Small-Signal Measurement

For situations where continuous sampling is necessary, the MAX11254 can be configured for sequencer mode 1, which supports continuous sampling of only one channel. If a single-channel ADC is desired, the MAX11214 has a similar architecture that incorporates a PGA and digital filter.

To demonstrate the continuous sampling capability of sequencer mode 1, an electrocardiogram (ECG) application is discussed. An ECG is an application example that requires continuous sampling of a pair, or several pairs, of differential leads placed on the human body. ECG signals measured from the body range from 100µV to 2-3mV maximum peak values, making them difficult to measure. The PGA and continuous sampling capability of the MAX11254 make it a good solution. For applications where simultaneous sampling of multiple channels is desired, the MAX11040K is an alternative. **Figure 2** displays one possible example of an ECG schematic using a single channel and the MAX11254.

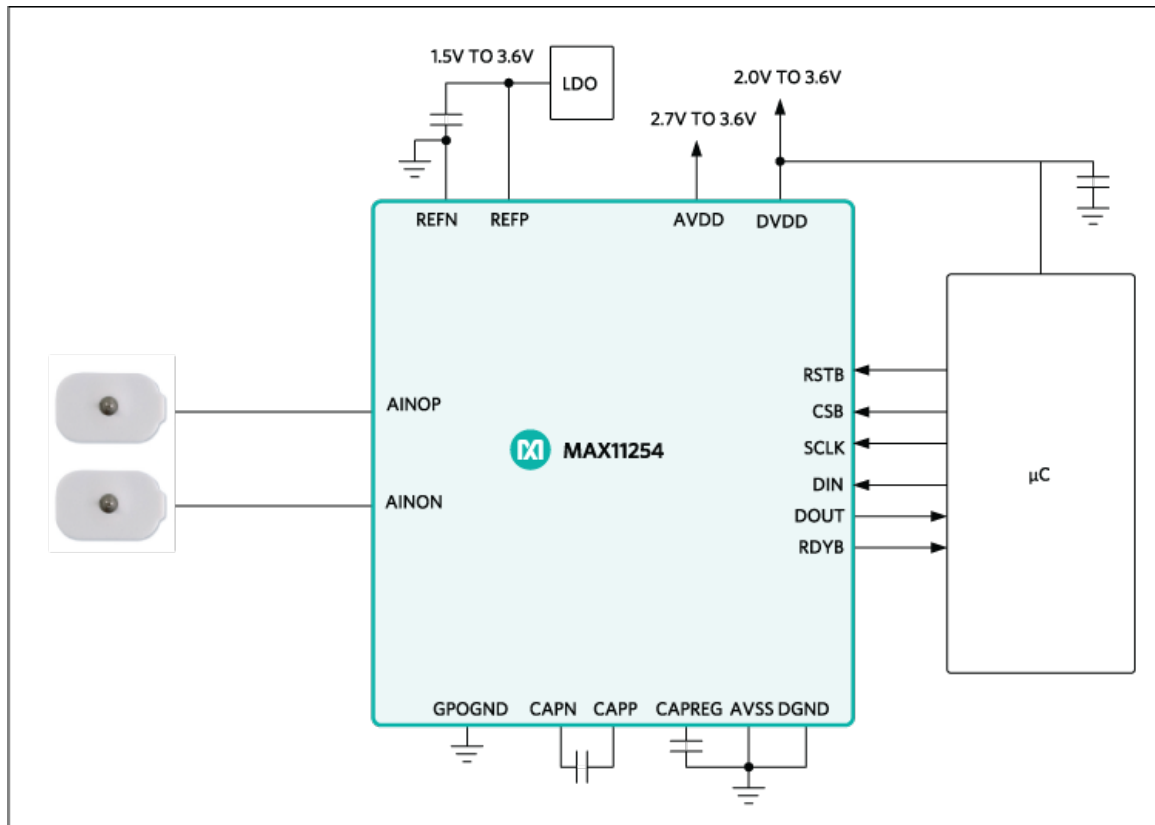


Figure 2. Basic ECG schematic using the MAX11254.

The MAX11254 requires a minimum differential voltage of 1.5V across the positive and negative reference inputs. Using the minimum voltage range produces the smallest detectable voltage step by the ADC. The following equation relates ADC bit resolution to the smallest measurable signal in a unipolar application. For bipolar operation, multiply the resulting step size by a factor of 2.

$$\text{STEP SIZE} = \frac{V_{\text{REF}}}{\text{GAIN} * 2^n}$$

where n equals the bit resolution of the ADC, Gain equals the gain of the internal PGA, and  $V_{\text{REF}}$  is the applied reference voltage. The maximum measurable input voltage equals the reference voltage divided by the gain of the PGA. Using the minimum  $V_{\text{REF}}$  of 1.5V and a maximum gain value of 128x equates to a minimum step size of 698.5pV and a full-scale measurement of 11.7mV. **Table 1** displays the maximum and minimum resolution obtainable by the MAX11254 with different configurations. Based on these settings, the MAX11254 can easily measure the voltage levels of an ECG signal.

Table 1. ADC Step Resolution Relative to Reference Voltage, Voltage Range, and PGA Gain

Mode	Reference Voltage (V)	PGA Gain	Step Resolution (nV)
Unipolar	1.5	1	89.4
		128	0.7
	3.6	1	214.6
		128	1.7
Bipolar	1.5	1	178.8

	128	1.4
3.6	1	429.2
	128	3.4

The second design criterion is the sampling rate. From Nyquist's theorem, the sampling rate of a signal must be at least twice the highest frequency content of the signal to prevent aliasing. ECG signals have frequency content ranging between 0 and 20Hz. The MAX11254 has sampling rates as high as 64ksps, well above the required 40Hz sampling rate. To confirm the MAX11254 could resolve an ECG signal, an ECG measurement was conducted using the MAX11254EVKIT. **Figure 3** shows a typical QRS curve from an ECG reading recorded using the MAX11254EVKIT with a 1x PGA setting. The electrode connected to the right wrist was connected to the negative input, and the electrode connected to the left wrist was connected to the positive input. **Figure 4** displays the recorded ECG signal using a 128x gain. The higher gain setting makes the QRS complex much easier to distinguish. For an integrated ECG analog front-end, the MAX30003 is a single-chip solution that can also detect heart rate.

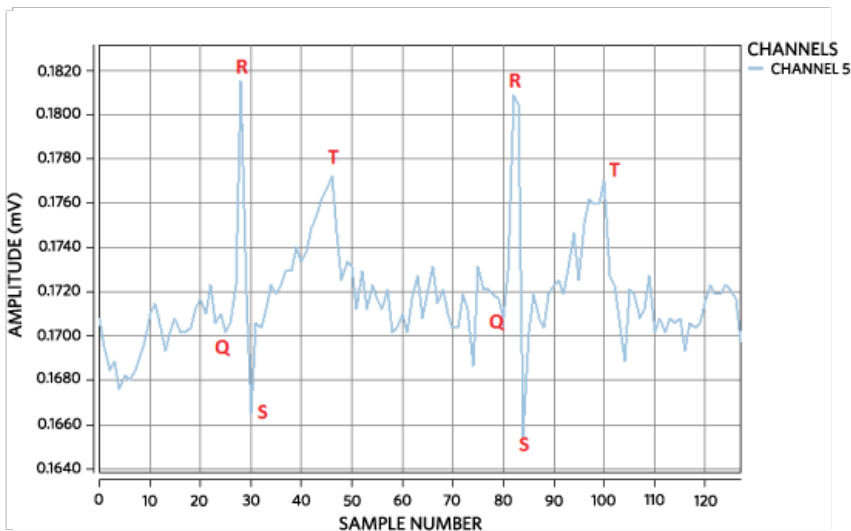


Figure 3. ECG waveform using 1x gain.

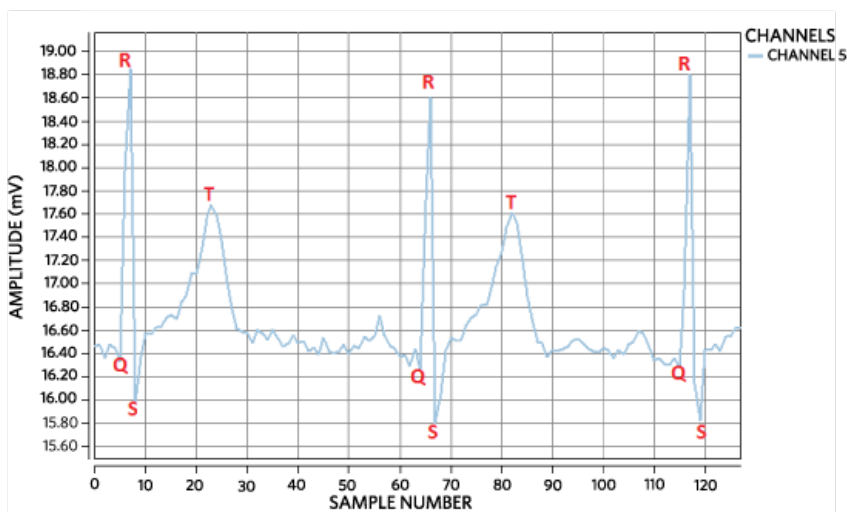


Figure 4. ECG waveform using 128x gain.

A designer might ask "What is the purpose of using a PGA gain of 1x when the MAX11254 has an option to bypass the PGA?" Even if gain is not needed, utilizing the PGA creates a unity gain buffer between the signal source and the ADC. Most ADCs require the signal source to have low output impedance. Delta-sigma ADCs typically use a switch capacitor input stage prior to the modulator. The high output impedance from the signal generator can disrupt the charging and discharging rates of the input capacitor, resulting in incorrect measurements.

### Selecting the Right Conversion Scheme in Sequencer Mode 1

Sequencer mode 1 incorporates two different schemes of continuous sampling along with the option to perform a single conversion. The three modes are broken into the following subject areas: single-cycle, single-cycle continuous, and continuous conversion.

Single-cycle conversion performs one conversion on the designated channel before transitioning into sleep mode. Single-cycle continuous and continuous conversion modes are similar but differ in available sampling rates. Single-cycle and single-cycle continuous both permit sample rates between 50sps and 12.8ksps; continuous conversion allows sample rates between 1.9sps and 64ksps. Continuous conversion mode was arbitrarily chosen for demonstrating the ECG application; single-cycle continuous conversion would have worked equally as well. There is one drawback to using the continuous conversion mode: latency. Latency is the startup delay of the first conversion once the command is issued to place the device into continuous conversion. Latency is measured from the rising edge of the chip-select bit after the command is issued to the falling edge of the data-ready bit, signaling there is a new conversion available. Latency duration is sample rate dependent and is documented in **Table 2**. Table 2 contains two latency factor columns. The first latency factor column compares the startup delay to the nominal sampling rate; the second latency factor column relates the startup delay to the measured sampling rate of subsequent conversions.

**Table 2. Latency Factor for Continuous Mode Sample Rates**

Nominal Sampling Rate (SPS)	Startup Delay (μs)	Latency Factor Relative to Nominal Sampling Rate	Latency Factor Relative to Measured Sampling Rate
1.9	509421.02	0.97	1.00
3.9	254787.34	0.99	1.00
7.8	127559.76	0.99	1.00
15.6	63924.78	1.00	1.00
31.2	32103.76	1.00	1.01
62.5	16173.1	1.01	1.02
125	8216.6	1.03	1.03
250	4242.24	1.06	1.07
500	2251.38	1.13	1.13
1000	1257.8	1.26	1.27
2000	760.3	1.52	1.53
4000	512.22	2.05	2.06
8000	387.42	3.10	3.12
17000	325.36	5.21	5.24
32000	170	5.44	5.47
64000	92.14	5.90	5.93

### Self-Calibration Procedure

Calibration is an important step in any measurement system and can be broken into two calibration types: self-calibration and system calibration. Self-calibration is specific to the ADC's modulator and ensures the voltage applied to the modulator inputs are scaled correctly relative to the reference voltage selected. Self-calibration excludes everything outside of the modulator including other functional blocks internal to the integrated circuit (IC) such as the PGA. System calibration includes the external blocks surrounding the modulator and

ensures that the voltage applied to the IC pins are scaled correctly relative to the reference voltage. Self-calibration must be performed prior to system calibration.

Running the self-calibration procedure prior to taking measurements ensures accurate measurements. Self-calibration should be implemented in every system architecture; without self-calibration, measurements can contain errors exceeding 400 mV. Self-calibration implements two separate calibrations: an offset and gain calibration. This is accomplished by taking a zero-scale and full-scale reading. The zero-scale measurement shorts the modulator inputs together internally and initiates a conversion. Processing the result generates the self-calibration offset coefficient (SCOC), which is saved to the SCOC register. The second stage of the calibration connects the reference voltage to the modulator inputs internally, initiates a conversion, processes the measurement to generate the self-calibration gain coefficient, and saves this value to the self-calibration gain coefficient (SCGC) register.

### Applying Calibration Coefficients

Once the self-calibration is complete, the calibration coefficients must be enabled before they are automatically applied to measurement results. There are two internal registers for each calibration coefficient: an internal register that stores the calibration coefficient generated from hardware calibration, and an SPI-writable register that the user can modify. The two different registers allow quick switching between user-programmed and hardware-generated calibration coefficients. If the user desires separate calibration coefficients for each channel, the user can conduct a calibration on each channel and then save those values to a microcontroller. When executing a conversion on a given channel, the user can edit the user-writable register with the desired calibration coefficient before initiating conversions. This type of calibration scheme is only possible in sequencer mode 1.

The least significant byte in register CTRL3 controls the implementation of calibration coefficients. Both the user-programmed and hardware-generated calibration registers use the same address. Bit CALREGSEL in CTRL3 controls the calibration register implemented in conversions. Both the user-programmed and hardware-generated calibration coefficients can be read at any time by issuing a read command of the system offset coefficient (SOC), system gain coefficient (SGC), SCOC, and SCGC registers, while appropriately selecting the value of CALREGSEL. CALREGSEL with a value of 1 returns the user-programmed values, while a value of 0 returns the hardware-generated values.

Applying calibration coefficients consumes time and thus decreases the sampling rate; the more calibrations performed, the slower the sampling rate. **Table 3** documents the measured conversion time for single-cycle and single-cycle continuous modes in sequencer mode 1 relative to the three calibration schemes. **Table 4** documents the measured conversion time for continuous mode in sequencer mode 1 relative to the three calibration schemes. In continuous conversion mode, the ADC consistently achieves a higher sampling rate than the nominal sampling rate in all calibration schemes. It should be noted that there is some variability in the conversion time during all conversions. The values in the tables should be considered nominal values and the user should expect some variation.

**Table 3. Measured Conversion Time for Single-Cycle and Single-Cycle Continuous Sampling for Different Calibration Implementations**

Nominal (SPS)	Single-Cycle Sample Rates			Single-Cycle Continuous Sample Rates		
	No Calibration (SPS)	Self-Calibration (SPS)	Self- and System Calibration (SPS)	No Calibration (SPS)	Self-Calibration (SPS)	Self- and System Calibration (SPS)
50	50.24	50.24	50.17	50.25	50.21	50.2
62.5	62.78	62.77	62.72	62.82	62.79	62.75
100	100.43	100.35	100.29	100.47	100.41	100.33
125	125.47	125.3	125.27	125.55	125.45	125.34
200	200.54	200.21	200.02	200.73	200.47	200.21
250	250.43	249.95	249.7	250.74	250.39	249.99
400	399.38	398.38	398.01	400.1	399.63	398.74
500	498.72	496.78	496.25	499.88	498.65	497.4
800	794.89	789.52	788.48	797.85	794.3	791.38
1000	988.72	980.21	966.3	993.37	987.7	983.51

1600	1566.02	1545.09	1542.22	1576.86	1563.55	1553.22
2000	1951.93	1914.65	1901.21	1969.33	1947.7	1932.27
3200	3050.74	2969.89	2961.95	3096.07	3040.73	3003.31
4000	3792.05	3668.47	3656.07	3856.94	3777.64	3719.74
6400	5866.93	5573.53	5547.98	6029.03	5830.06	5697.08
12800	10786.54	9842.52	9468.52	11389.2	10629.2	10235.35

**Table 4. Measured Conversion Time for Continuous Sampling for Different Calibration Implementations**

<b>Continuous Sample Rates</b>			
<b>Nominal (SPS)</b>	<b>No Calibrations (SPS)</b>	<b>Self-Calibration (SPS)</b>	<b>Self- and System Calibration (SPS)</b>
1.9	1.97	1.96	1.96
3.9	3.93	3.93	3.93
7.8	7.86	7.86	7.86
15.6	15.72	15.72	15.72
31.2	31.45	31.43	31.28
62.5	62.90	62.87	62.84
125	125.79	125.74	125.67
250	251.57	251.49	251.31
500	503.09	502.41	502.74
1000	1006.06	1005.88	1005.52
2000	2011.99	2011.18	2010.86
4000	4024.04	4024.14	4023.34
8000	8048.29	8044.41	8043.76
16000	16096.15	16092.69	16084.93
32000	32199.21	32185.39	32175.03
64000	64391.50	64391.50	64377.69

### Application Example 2: Multiple Channel Measurements

Pressure sensors and strain gauges, which are often used in weigh scales, provide different resolutions depending on the sensing range of the scale. For example, a consumer scale measuring body weight will not provide the same resolution as a scientific scale measuring the mass of chemicals destined for a reaction. Chemical Material Polishing (CMP) is another application that requires very precise measurements of the pressure applied to a wafer during polishing. Regardless of the application, pressure sensors all revolve around the basic principle of converting mechanical energy into electrical energy.

There are several possible configurations for making a scale; the example shown uses four load sensors to convert mechanical strain into an electrical signal. A typical design for a load sensor uses a Wheatstone bridge configuration incorporating two resistors constructed from piezoresistive material and two standard resistors. Two parallel resistor networks are formed with a differential voltage forming at the center. One piezoresistive resistor is in each parallel string in opposite orientation. Applied pressure creates varying differential voltage between the two center points of the two parallel resistor networks. The differential voltage is measured by an ADC and processed to calculate the pressure applied to the sensor. **Figure 5** displays the block diagram of the [MAXREFDES82#](#), a reference design that incorporates the MAX11254 ADC to construct a smart force sensor.

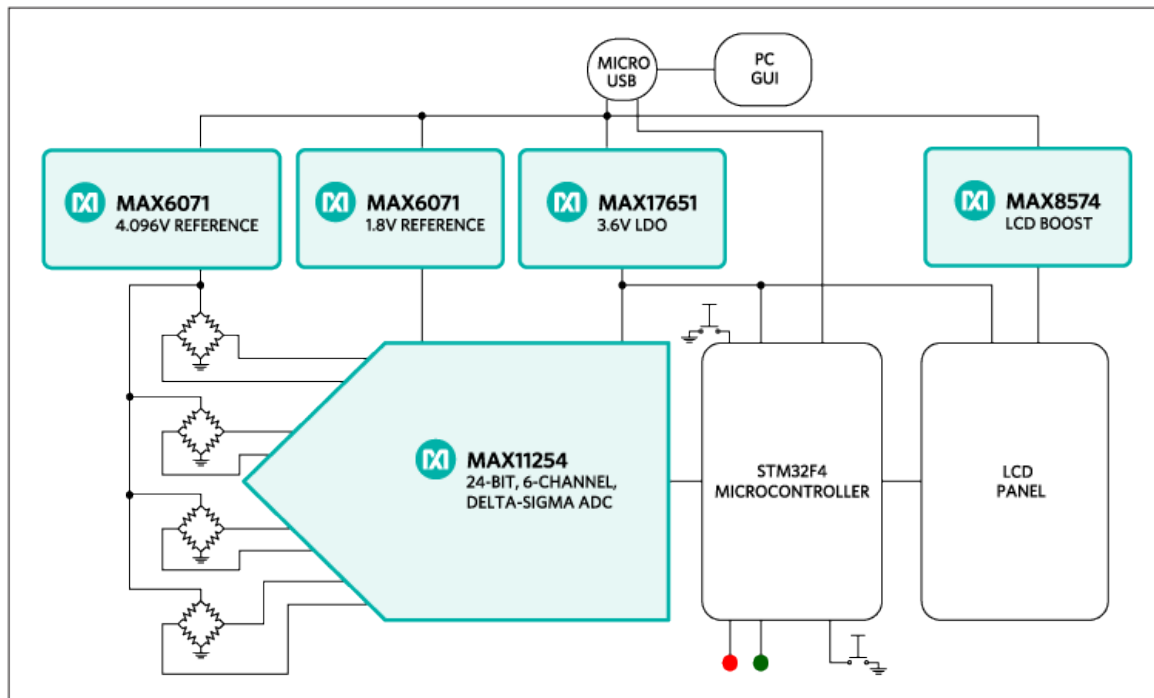


Figure 5. MAXREFDES82# block diagram.

The MAXREFDES82# uses sequencer mode 2 to wake up, cycle through the four analog inputs, and re-enter sleep mode. Using four load sensors allows estimation of the center of mass and position of an applied force.

The MAX11254 includes several GPIO pins, which have various uses including synchronization of devices, external clock input, or digital output. Sequencer mode 1 and 2 require the user to manually control the state of the GPO/GPIO pins using the GPO\_DIR and GPIO\_CTRL registers, whereas sequencer mode 3 can automate the control of the GPO/GPIO pins. The GPO pins are analog switches that connect their inputs to the GPOGND pin. This allows the user to disconnect the sensor ground path while the sensor is not needed, which saves power in any of the three sequencing modes.

### Application Example 3: Power Efficiency

To obtain the most power efficient system, the system can be set up to automatically wake up, enable the sensors, perform the signal conversions, and then disable the sensors and go back to sleep. This can all be accomplished with sequencer mode 3. By using the GPIO pins as digital outputs, they can be used to control the sensor itself or the device powering the sensor, such as an LDO. Alternatively, the sensor ground return nodes can be connected to the GPO pins so that the user can "break" the circuit path while the sensor is not needed. **Figure 6** emphasizes the connection of two Wheatstone bridge ground nodes connected to the GPO pins.



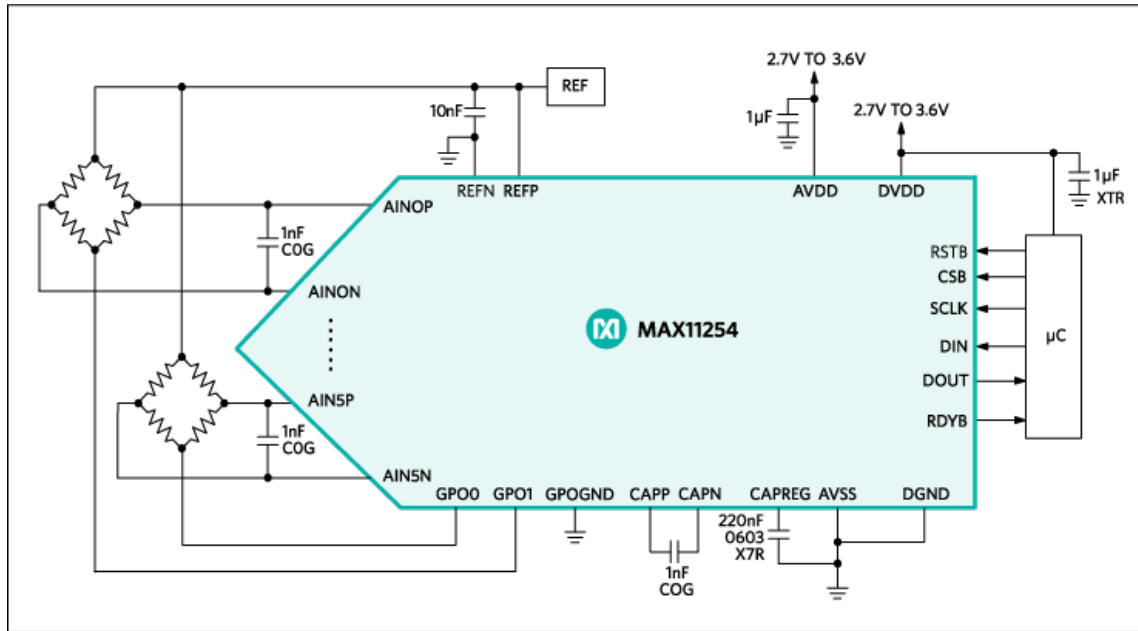


Figure 6. Circuit example showing the Wheatstone bridge ground nodes connected to the GPO pins of the MAX11254.

One issue with turning the sensors on and off is that the sensor could be in a transient state during the measurements of that channel. The MAX11254 features a delay register that allows both the delay of the conversion and the delay of the GPO/GPIOs so that appropriate timing restraints can be respected. By using the GPO/GPIO pins effectively, a system can operate even more efficiently.

## Conclusion

The MAX11254 is a highly-integrated ADC that has tremendous functionality suitable for almost any application. The 24-bit resolution and PGA allow measurements of signals from pV to V. The three sequencing modes provide high flexibility in the timing of channel conversions, and can save system power by limiting processor intervention. The calibration schemes ensure reliable and consistent measurements, and the GPO/GPIO features can be utilized to create smarter and more power efficient sensor systems.

## Related Parts

<a href="#">MAX11254</a>	24-Bit, 6-Channel, 64ksps, 6.2nV/√Hz PGA, Delta-Sigma ADC with SPI Interface	<a href="#">Free Samples</a>
<a href="#">MAX11259</a>	24-Bit, 6-Channel, 16ksps, 6.2nV/√Hz PGA, Delta-Sigma ADC with I <sup>2</sup> C Interface	<a href="#">Free Samples</a>

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