Product Document

TSL2771

Light-to-Digital Converter with Proximity Sensing

General Description

The TSL2771 family of devices provides both ambient light sensing (ALS) and proximity detection (when coupled with an external IR LED). The ALS approximates human eye response to light intensity under a variety of lighting conditions and through a variety of attenuation materials. The proximity detection feature allows a large dynamic range of operation for use in short distance detection behind dark glass such as in a cell phone or for longer distance measurements for applications such as presence detection for monitors or laptops. The programmable proximity detection enables continuous measurements across the entire range. In addition, an internal state machine provides the ability to put the device into a low power mode in between ALS and proximity measurements providing very low average power consumption.

While useful for general purpose light sensing, the device is particularly useful for display management with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Display panel and keyboard backlighting can account for up to 30 to 40 percent of total platform power. The ALS features are ideal for use in tablets, notebook PCs, LCD monitors, flat-panel televisions, and cell phones.

The proximity function is targeted specifically towards cell phone, LCD monitor, laptop, and flat-panel television applications. In cell phones, the proximity detection can detect when the user positions the phone close to their ear. The device is fast enough to provide proximity information at a high repetition rate needed when answering a phone call. It can also detect both close and far distances so the application can implement more complex algorithms to provide a more robust interface. In laptop or monitor applications, the product is sensitive enough to determine whether a user is in front of the laptop using the keyboard or away from the desk. This provides both improved *green* power saving capability and the added security to lock the computer when the user is not present.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of TSL2771, Light-to-Digital Converter with Proximity Sensing are listed below:

Figure 1:
Added Value of Using TSL2771

Benefits	Features
• Enables Operation in IR Light Environments	• Patented Dual-Diode Architecture
• Enables Operation in 10k Lux Sunlight and Accurate Sensing Behind Spectrally Distorting Materials	• 1M:1 Dynamic Range
• Allows Multiple Power-Level Selection Without External Passives	• Programmable LED Drive Current
• Reduces Micro-Processor Interrupt Overhead	• Programmable Interrupt Function
• Reduces board Space Requirements while Simplifying Designs	• Area Efficient 2mm x 2mm Dual Flat No-Lead (FN) Package

- Ambient Light Sensing and Proximity Detection in a Single Device
- Ambient Light Sensing (ALS)
  - Approximates Human Eye Response
  - Programmable Analog Gain
  - Programmable Integration Time
  - Programmable Interrupt Function with Upper and Lower Threshold
  - Resolution Up to 16 Bits
  - Very High Sensitivity — Operates Well Behind Darkened Glass
  - Up to 1,000,000:1 Dynamic Range
- Proximity Detection
  - Programmable Number of IR Pulses
  - Programmable Current Sink for the IR LED — No Limiting Resistor Needed
  - Programmable Interrupt Function with Upper and Lower Threshold
  - Covers a 2000:1 Dynamic Range
- Programmable Wait Timer
  - Programmable from 2.72 ms to > 8 Seconds
  - Wait State — 65 mA Typical Current
- I^2C Interface Compatible
  - Up to 400 kHz (I^2C Fast Mode)
  - Dedicated Interrupt Pin
- Sleep Mode – 2.5 mA Typical Current

Applications

TSL2771, Light-to-Digital Converter with Proximity Sensing is ideal for:

- Cell Phone Backlight Dimming
- Cell Phone Touch Screen Disable
- Notebook/Monitor Security
- Automatic Speakerphone Enable
- Automatic Menu Popup

Functional Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TSL2771 Block Diagram
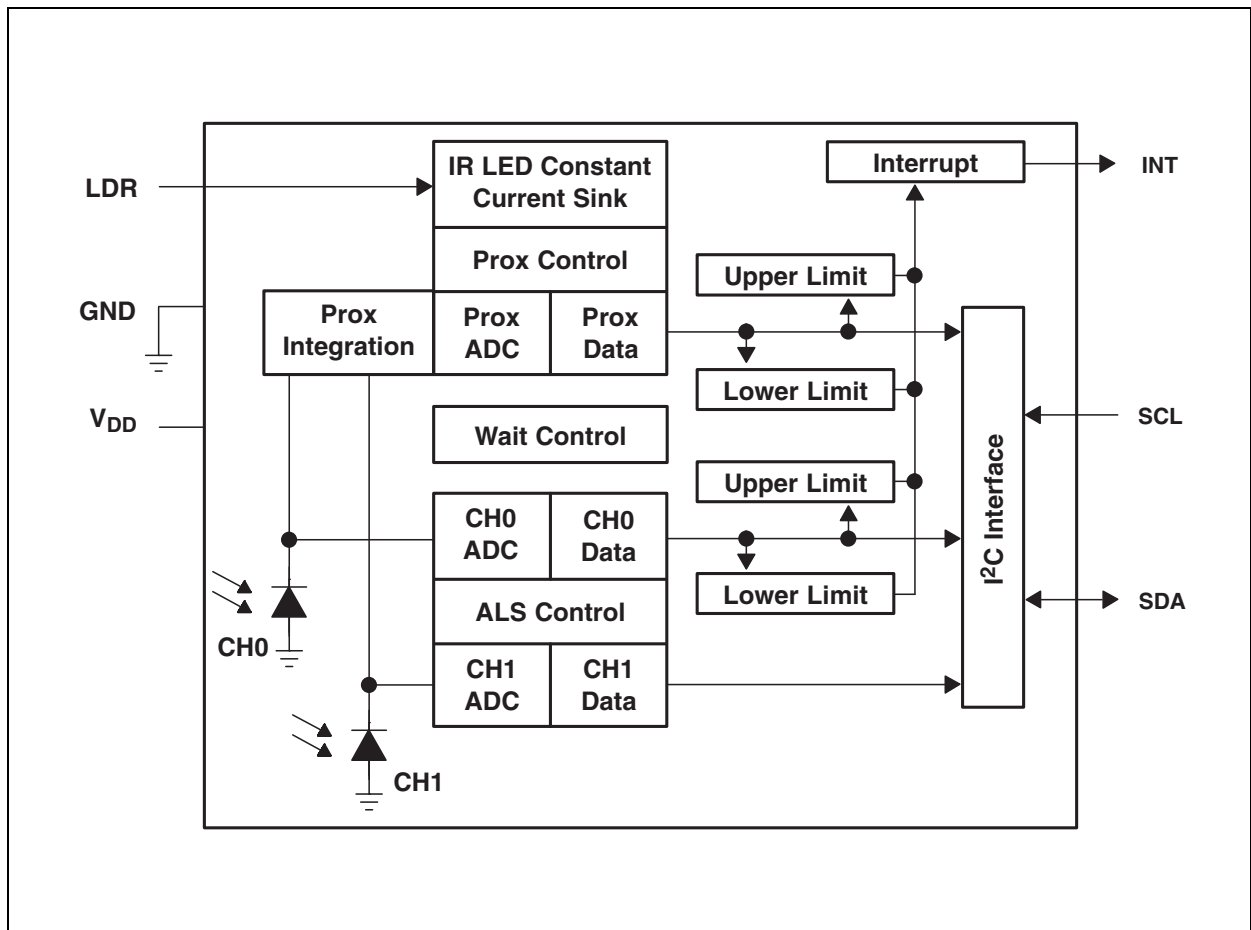
Detailed Description

The TSL2771 light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I²C interface. Each device combines a Channel 0 photodiode (CH0), which is responsive to both visible and infrared light, and a channel 1 photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents into a digital value providing up to 16 bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the data registers. This digital output can be read by a microprocessor through which the illuminance (ambient light level) in Lux is derived using an empirical formula to approximate the human eye response.

Communication to the device is accomplished through a fast (up to 400 kHz), two-wire I²C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

Proximity detection requires only a single external IR LED. An internal LED driver can be configured to provide a constant current sink of 12.5 mA, 25 mA, 50 mA, or 100 mA of current. No external current limiting resistor is required. The number of proximity LED pulses can be programmed from 1 to 255 pulses. Each pulse has a 16-µs period. This LED current, coupled with the programmable number of pulses, provides a 2000:1 contiguous dynamic range.

Pin Assignments

The TSL2771 pin assignments are described below:

Figure 3:
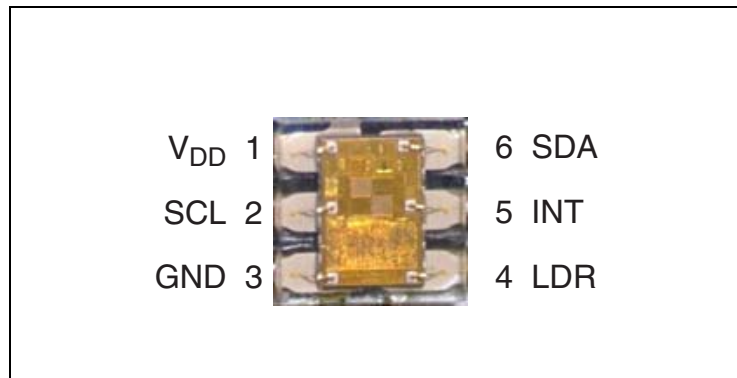**Package FN Dual Flat No-Lead (Top View)**

Figure 4:
Terminal Functions

Terminal		Type	Description
Name	**No**		
V_{DD}	1		Supply voltage.
SCL	2	I	I²C serial clock input terminal — clock signal for I²C serial data.
GND	3		Power supply ground. All voltages are referenced to GND.
LDR	4	O	LED driver for proximity emitter — up to 100 mA, open drain.
INT	5	O	Interrupt — open drain (active low).
SDA	6	I/O	I²C serial data I/O terminal — serial data I/O for I²C

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Symbol	Parameter	Min	Max	Units
V_{DD}[1]	Supply voltage		3.8	V
V_O	Digital output voltage range	-0.5	3.8	V
I_O	Digital output current	-1	20	mA
T_{stg}	Storage temperature range	-40	85	°C
ESD_{HBM}	ESD tolerance, human body model	±2000		V

Note(s):

1. All voltages are with respect to GND.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	2.6	3	3.6	V
T_A	Operating free-air temperature	-30		70	°C

Figure 7:
Operating Characteristics; V$_{DD}$ = 3 V, T$_A$ = 25ºC (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I$_{DD}$	Supply current	Active — LDR pulse OFF		175	250	µA
		Wait mode		65		
		Sleep mode - no I²C activity		2.5	4	
V$_{OL}$	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I$_{LEAK}$	Leakage current, SDA, SCL, INT pins		−5		5	µA
I$_{LEAK}$	Leakage current, LDR pin			±10		µA
V$_{IH}$	SCL, SDA input high voltage	TSL27711, TSL27715	0.7 V$_{DD}$			V
		TSL27713, TSL27717	1.25			
V$_{IL}$	SCL, SDA input low voltage	TSL27711, TSL27715			0.3 V$_{DD}$	V
		TSL27713, TSL27717			0.54	

Figure 8:

ALS Characteristics; V_{DD} = 3 V, T_A = 25ºC, Gain = 16, AEN = 1 (unless otherwise noted) [1] [2] [3]

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Dark ADC count value	$E_e = 0$, AGAIN = 120x, ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ADC integration time step size	ATIME = 0xFF		2.58	2.72	2.9	ms
ADC Number of integration steps			1		256	steps
ADC counts per step	ATIME = 0xFF		0		1024	counts
ADC count value	ATIME = 0xC0		0		65535	counts
ADC count value	$\lambda_p = 625$ nm, $E_e = 171.6$ µW/cm^2, ATIME = 0xF6 (27 ms) [2]	CH0	4000	5000	6000	counts
		CH1		790		
	$\lambda_p = 850$ nm, $E_e = 219.7$ µW/cm^2 ATIME = 0xF6 (27 ms) [3]	CH0	4000	5000	6000	
		CH1		2800		
ADC count value ratio: CH1/CH0	$\lambda_p = 625$ nm, ATIME 0xF6 (27 ms) [2]		10.8	15.8	20.8	%
	$\lambda_p = 850$ nm, ATIME 0xF6 (27 ms) [3]		41	56	68	
R_e Irradiance responsivity	$\lambda_p = 625$ nm, ATIME = 0xF6 (27 ms) [2]	CH0		29.1		counts/ (µW/cm^2)
		CH1		4.6		
	$\lambda_p = 850$ nm, ATIME = 0xF6 (27 ms) [3]	CH0		22.8		
		CH1		12.7		
Gain scaling, relative to 1x gain setting	8x		−10		10	%
	16x		−10		10	
	120x		−10		10	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible 625 nm LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.

2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 625$ nm and spectral halfwidth $\Delta\lambda_{1/2} = 20$ nm.

3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength $\lambda_p = 850$ nm and spectral halfwidth $\Delta\lambda_{1/2} = 42$ nm.

Figure 9:
Proximity Characteristics; V$_{DD}$ = 3 V, T$_A$ = 25°C, PEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Condition	Min	Typ	Max	Unit
I$_{DD}$ Supply current	LDR pulse ON			3		mA
ADC conversion time step size	PTIME = 0xFF		2.58	2.72	2.9	ms
ADC number of integration steps			1		256	steps
ADC counts per step	PTIME = 0xFF		0		1023	counts
IR LED pulse count			0		255	pulses
pulse period	Two or more pulses			16		µs
LED pulse width — LED ON time				7.3		µs
LED drive current	I$_{SINK}$ sink current @ 600 mV, LDR pin	PDRIVE=0	75	100	125	mA
		PDRIVE=1		50		
		PDRIVE=2		25		
		PDRIVE=3		12.5		
Operating distance [1]				18		inches

Note(s):

1. Proximity Operating Distance is dependent upon emitter properties and the reflective properties of the proximity surface. The nominal value shown uses an IR emitter with a peak wavelength of 850nm and a 20° half angle. The proximity surface used is a 90% reflective (white surface) 16 × 20-inch Kodak Gray Card. 60 mw/SR, 100 mA, 64 pulses, open view (no glass). **Note:** Greater distances are achievable with appropriate system considerations.

Figure 10:
Wait Characteristics; V$_{DD}$ = 3 V, T$_A$ = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Test Conditions	Channel	Min	Typ	Max	Unit
Wait step size	WTIME = 0xFF		2.58	2.72	2.9	ms
Wait number of integration steps			1		256	steps

Figure 11:
AC Electrical Characteristics; V$_{DD}$ = 3 V, T$_A$ = 25°C, (unless otherwise noted)

Symbol	Parameter [1]	Test Conditions	Min	Typ	Max	Unit
f$_{(SCL)}$	Clock frequency (I^{2}C only)		0		400	kHz
t$_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
t$_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
t$_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
t$_{(SUSTO)}$	Stop condition setup time		0.6			µs
t$_{(HDDAT)}$	Data hold time		0			µs
t$_{(SUDAT)}$	Data setup time		100			ns
t$_{(LOW)}$	SCL clock low period		1.3			µs
t$_{(HIGH)}$	SCL clock high period		0.6			µs
t$_F$	Clock/data fall time				300	ns
t$_R$	Clock/data rise time				300	ns
C$_i$	Input pin capacitance				10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Parameter Measurement Information

Figure 12:
Timing Diagrams
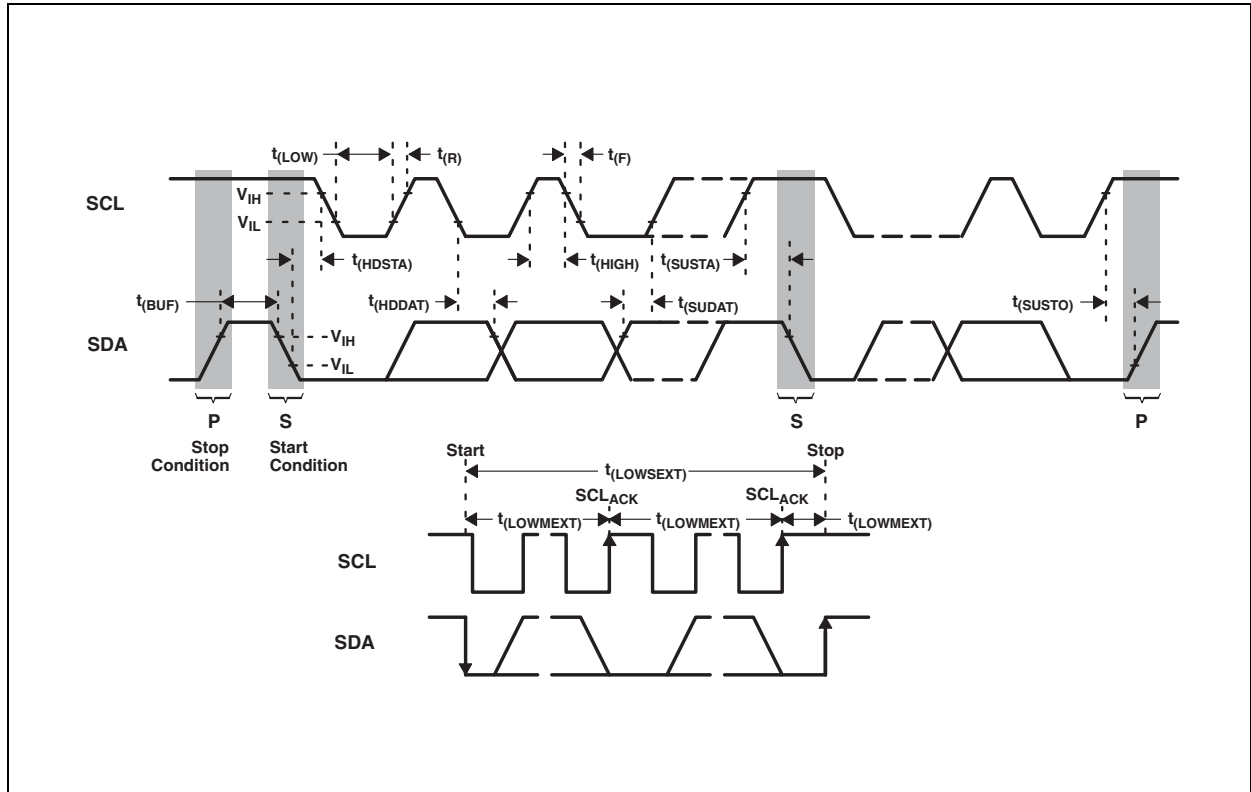
Typical Operating Characteristics

Figure 13:
Spectral Responsivity
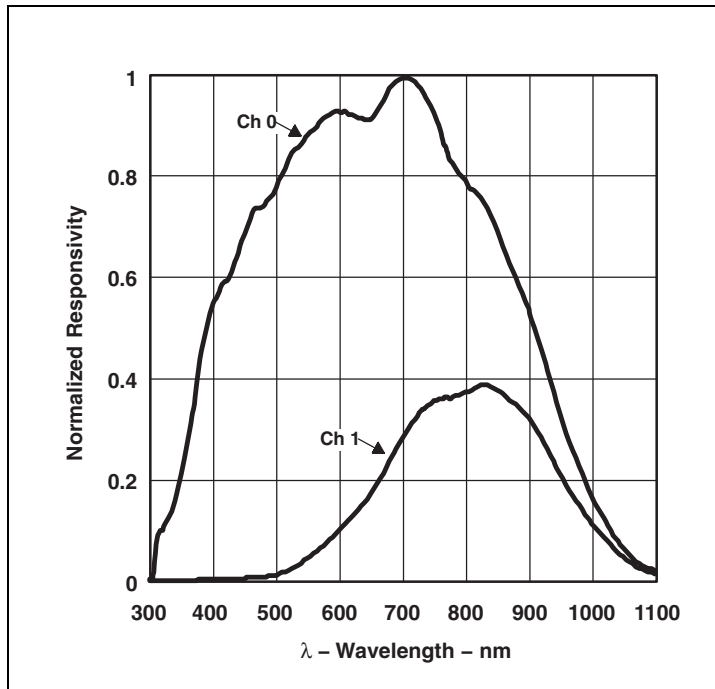
Figure 14:
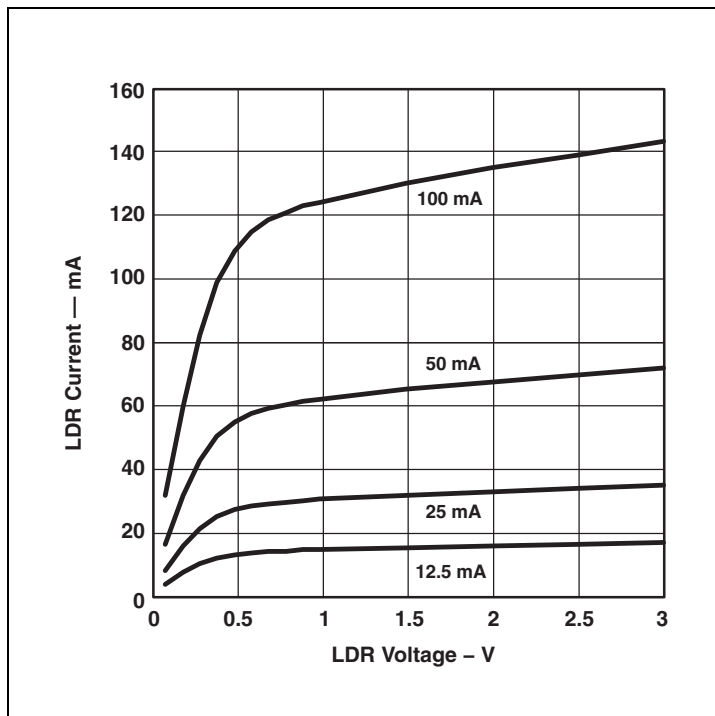**Typical LDR Current vs. Voltage**

Figure 15:
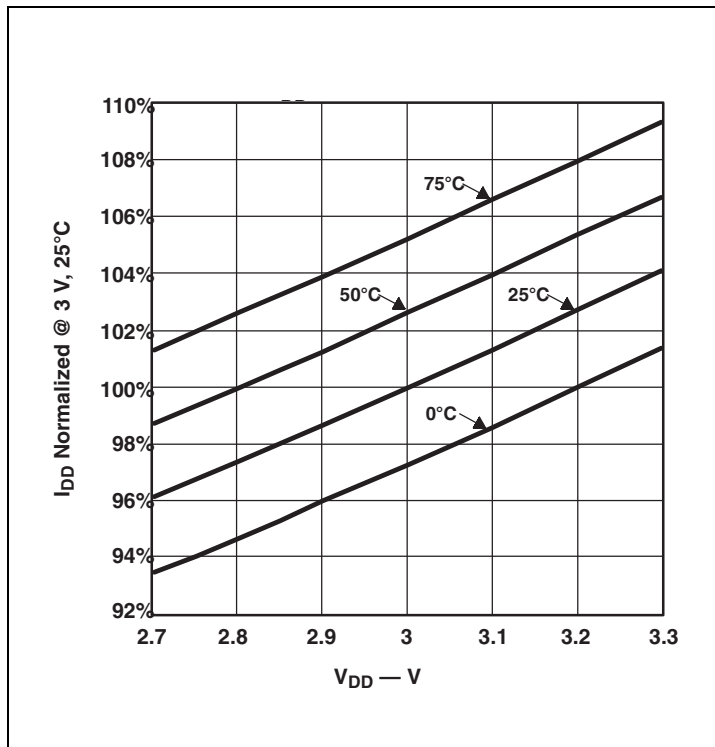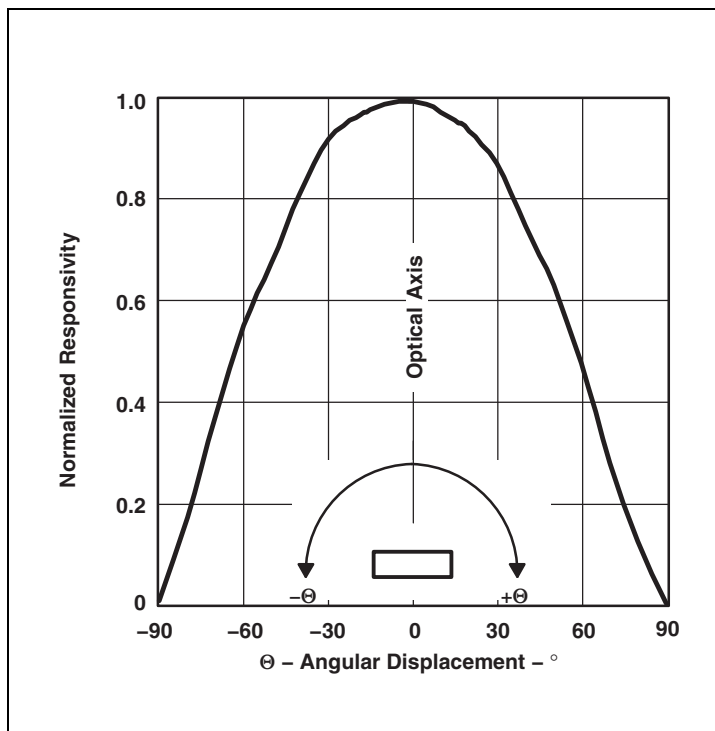**Normalized I$_{DD}$ vs.V$_{DD}$ and Temperature**


Figure 16:
Normalized Responsivity vs. Angular Displacement

Principles Of Operation

System State Machine

The device provides control of ALS, proximity detection, and power management functionality through an internal state machine (Figure 17). After a power-on-reset, the device is in the sleep mode. As soon as the PON bit is set, the device will move to the start state. It will then continue through the Prox, Wait, and ALS states. If these states are enabled, the device will execute each function. If the PON bit is set to 0, the state machine will continue until all conversions are completed and then go into a low power sleep mode.

Figure 17:
Simplified State Diagram
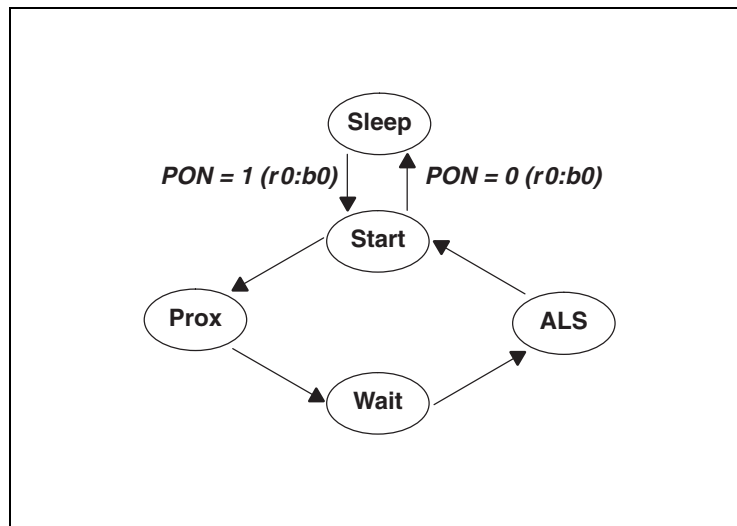
Note(s): In this document, the nomenclature uses the bit field name in italics followed by the register number and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power ON (PON) is in register 0, bit 0. This is represented as *PON (r0:b0)*.

Photodiodes

Conventional silicon detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting) due to the difference between the silicon detector response and the brightness perceived by the human eye.

This problem is overcome through the use of two photodiodes. The Channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the Channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC) for the Channel 0 and Channel 1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel *count*. The transfers are double-buffered to ensure data integrity.

Figure 18:
ALS Operation
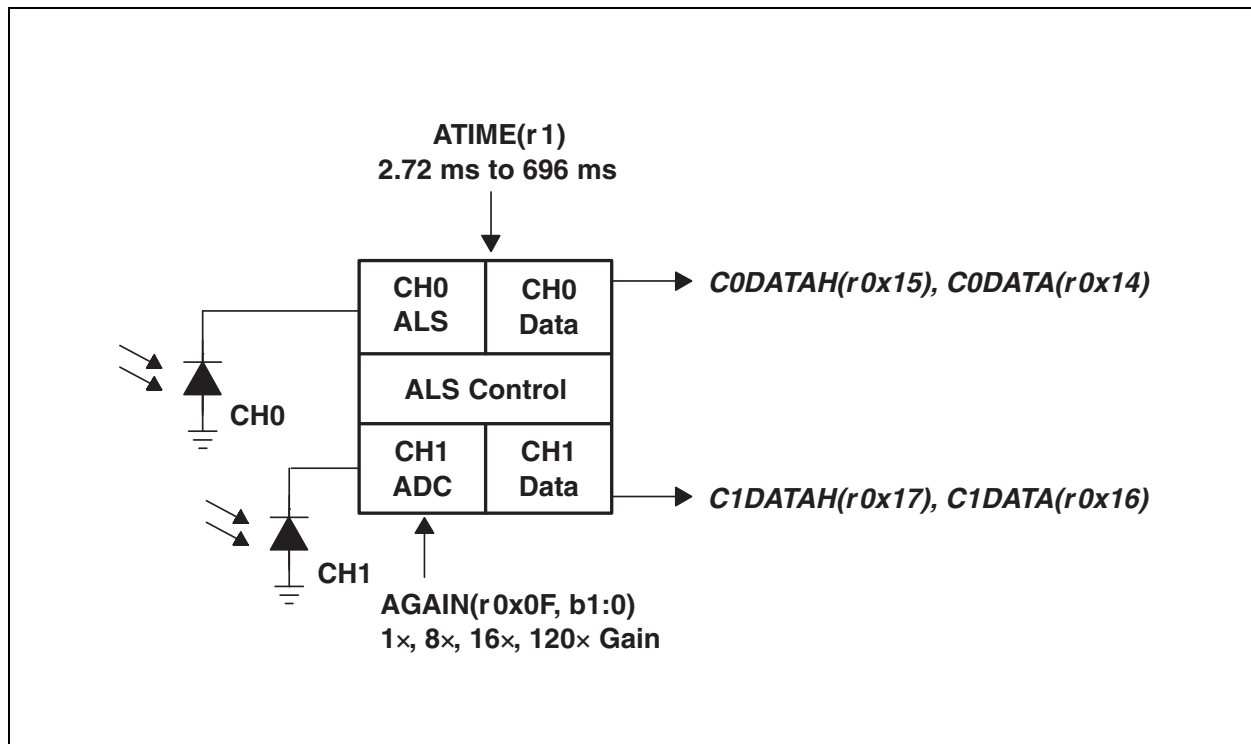
The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 - Integration Time / 2.72 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.72 ms × (256 - ATIME)

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See **ams** application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

CPL = (ATIME_ms × AGAINx) / (GA × 53)

Lux1 = (C0DATA - 2 × C1DATA) / CPL

Lux2 = (0.6 × C0DATA - C1DATA) / CPL

Lux = MAX(Lux1, Lux2, 0)

Proximity Detection

Proximity sensing uses an external light source (generally an infrared emitter) to emit light, which is then viewed by the integrated light detector to measure the amount of reflected light when an object is in the light path (Figure 19). The amount of light detected from a reflected surface can then be used to determine an object's proximity to the sensor.

Figure 19:
Proximity Detection
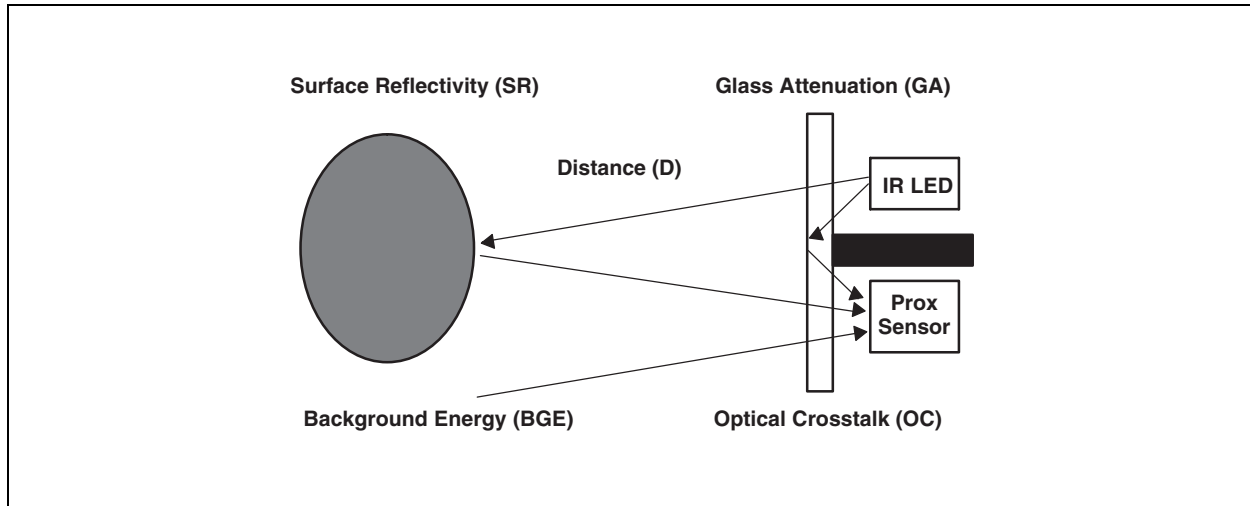
The device has controls for the number of IR pulses (PPCOUNT), the integration time (PTIME), the LED drive current (PDRIVE), and the photodiode configuration (PDIODE) (Figure 20). The photodiode configuration can be set to CH1 diode (recommended), CH0 diode, or a combination of both diodes. At the end of the integration cycle, the results are latched into the proximity data (PDATA) register.

Figure 20:
Proximity Detection Operation
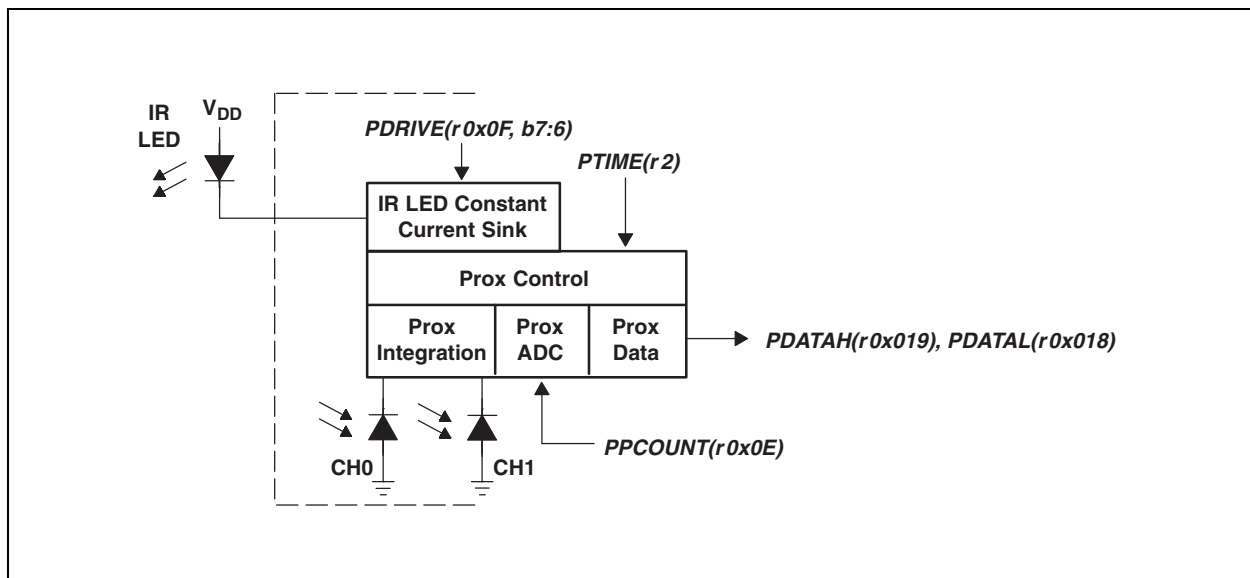
The LED drive current is controlled by a regulated current sink on the LDR pin. This feature eliminates the need to use a current limiting resistor to control LED current. The LED drive current can be configured for 12.5 mA, 25 mA, 50 mA, or 100 mA. For higher LED drive requirements, an external P type transistor can be used to control the LED current.

The number of LED pulses can be programmed to any value between 1 and 255 pulses as needed. Increasing the number of LED pulses at a given current will increase the sensor sensitivity. Sensitivity grows by the square root of the number of pulses. Each pulse has a 16-μs period.

Figure 21:
Proximity IR LED Waveform
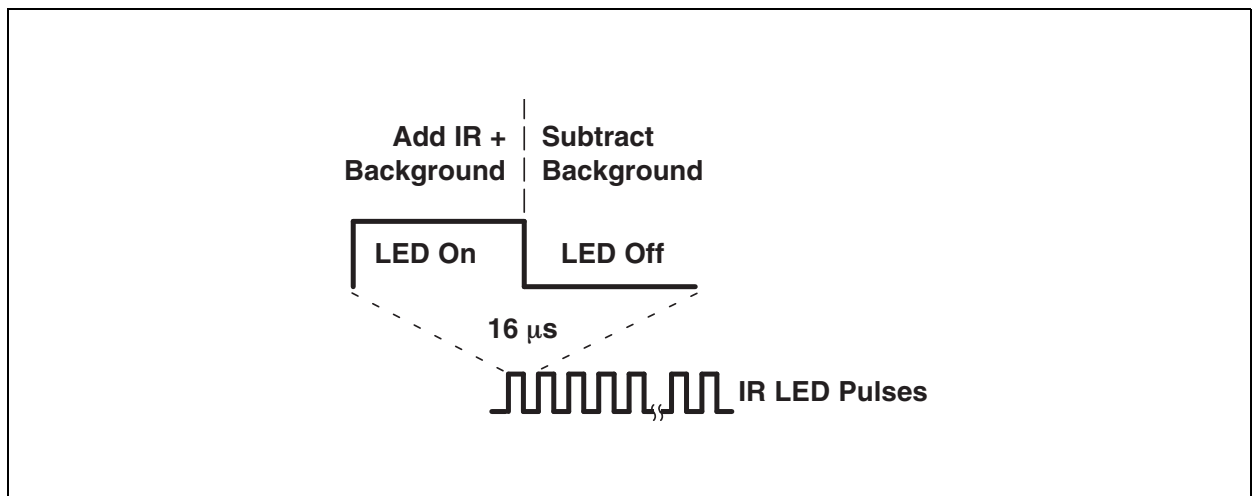
The proximity integration time (PTIME) is the period of time that the internal ADC converts the analog signal to a digital count. It is recommend that this be set to a minimum of PTIME = 0xFF or 2.72 ms.

The combination of LED power and number of pulses can be used to control the distance at which the sensor can detect proximity. Figure 22 shows an example of the distances covered with settings such that each curve covers 2x the distance. Counts up to 64 pulses provide a 16x range.

Figure 22:
**Proximity ADC Count vs. Relative Distance**
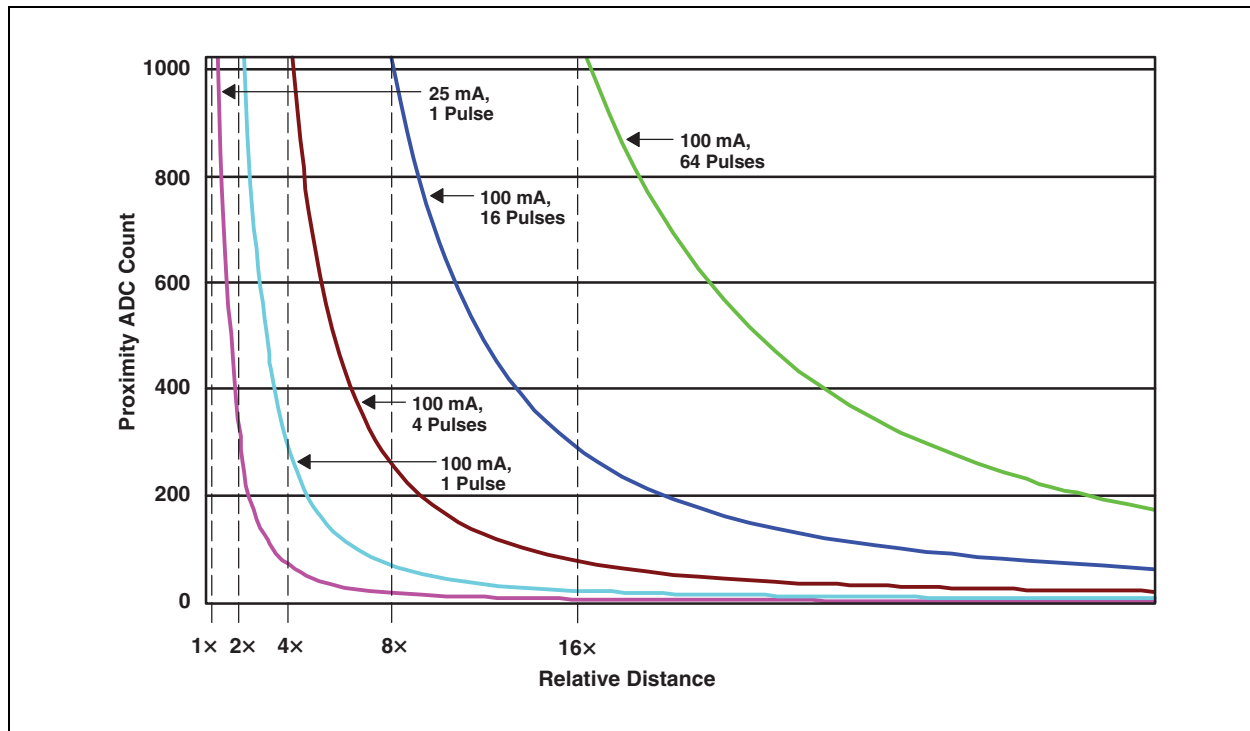
Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and it's status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or ALS interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the ALS CH0 data (C0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx). It is important to note that the low threshold value must be less than the high threshold value for proper operation.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS or proximity occurrences before an interrupt is generated. The persistence register (0x0C) allows the user to set the ALS persistence (APERS) and the proximity persistence (PPERS) values. See the persistence register for details on the persistence filter values. Once the persistence filter generates

an interrupt, it will continue until a special function interrupt clear command is received (seeCommand Register).

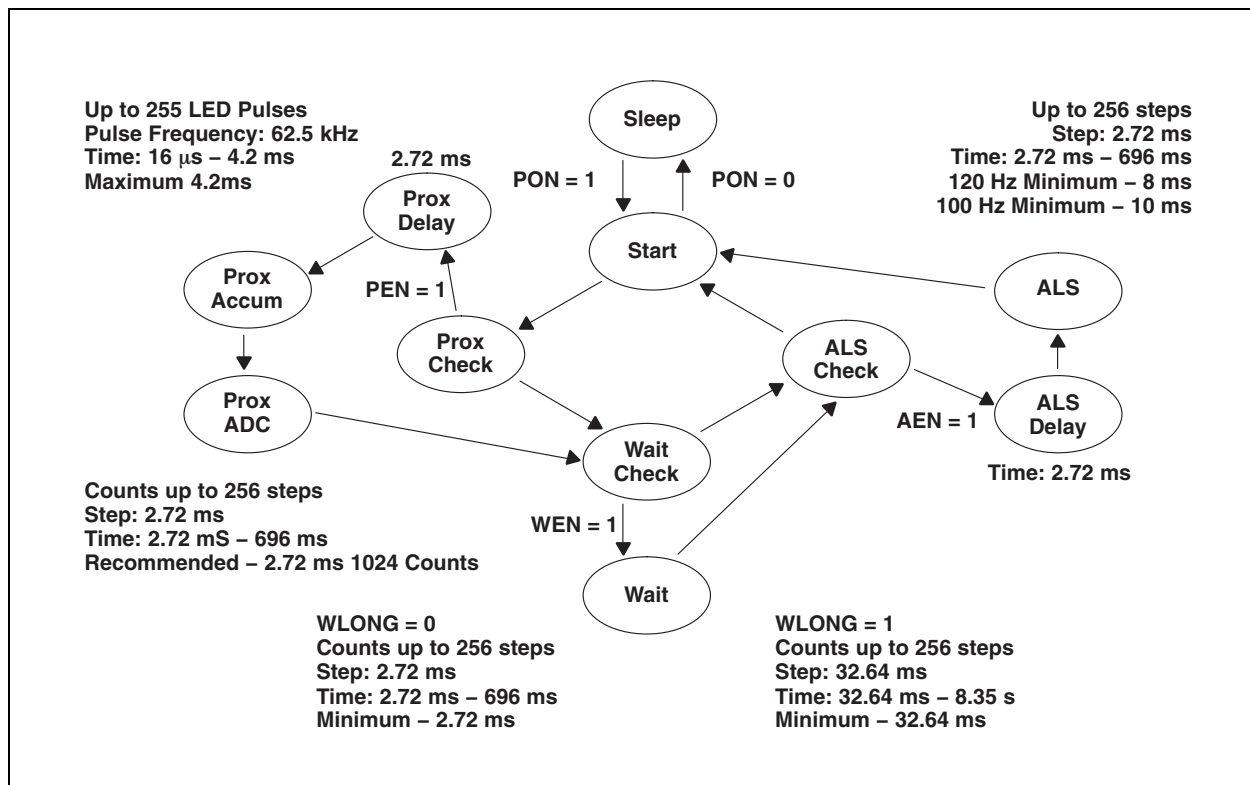**Figure 23:**
Programmable Interrupt
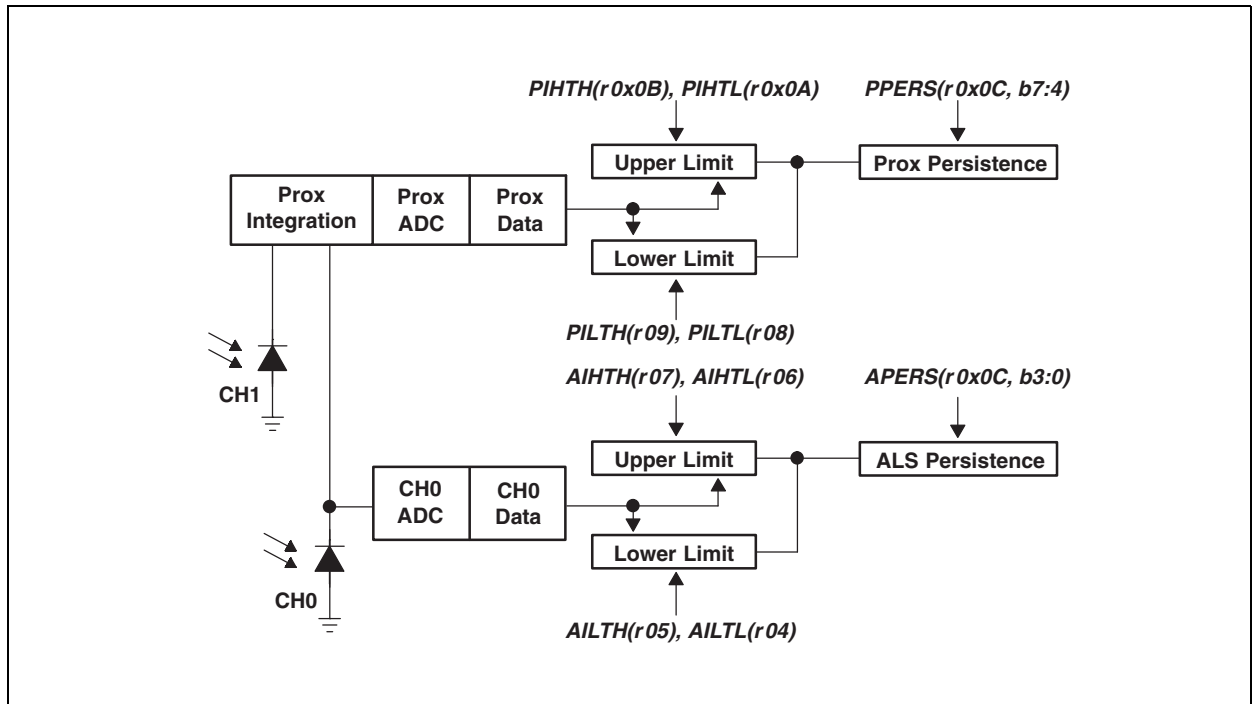
State Diagram

Figure 24 shows a more detailed flow for the state machine. The device starts in the sleep mode. The PON bit is written to enable the device. A 2.72-ms delay will occur before entering the start state. If the PEN bit is set, the state machine will step through the proximity states of proximity accumulate and then proximity ADC conversion. As soon as the conversion is complete, the state machine will move to the following state.

If the WEN bit is set, the state machine will then cycle through the wait state. If the WLONG bit is set, the wait cycles are extended by 12× over normal operation. When the wait counter terminates, the state machine will step to the ALS state.

The AEN should always be set, even in proximity-only operation. In this case, a minimum of 1 integration time step should be programmed. The ALS state machine will continue until it reaches the terminal count at which point the data will be latched in the ALS register and the interrupt set, if enabled.
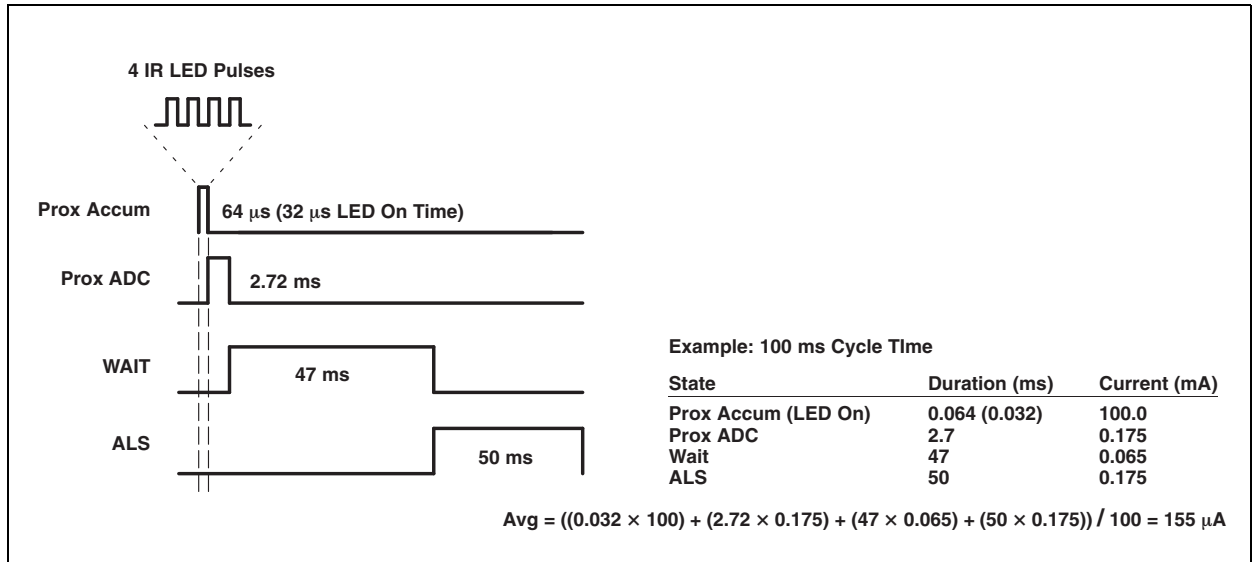
Figure 24:
Expanded State Diagram

Power Management

Power consumption can be controlled through the use of the wait state timing because the wait state consumes only 65 µA of power. Figure 25 shows an example of using the power management feature to achieve an average power consumption of 155 µA current with four 100-mA pulses of proximity detection and 50 ms of ALS detection.

Figure 25:
Power Consumption Calculations

State	Duration (ms)	Current (mA)
Prox Accum (LED On)	0.064 (0.032)	100.0
Prox ADC	2.7	0.175
Wait	47	0.065
ALS	50	0.175

Avg = ((0.032 × 100) + (2.72 × 0.175) + (47 × 0.065) + (50 × 0.175)) / 100 = 155 µA

I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 26). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c-bus.org/references/.

A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
S	Repeated Start Condition
W	Write (0)
...	Continuation of protocol
☐	Master-to-Slave
▨	Slave-to-Master

Figure 26:
I²C Protocols

I²C Write Protocol

I²C Read Protocol

I²C Read Protocol — Combined Format

ams
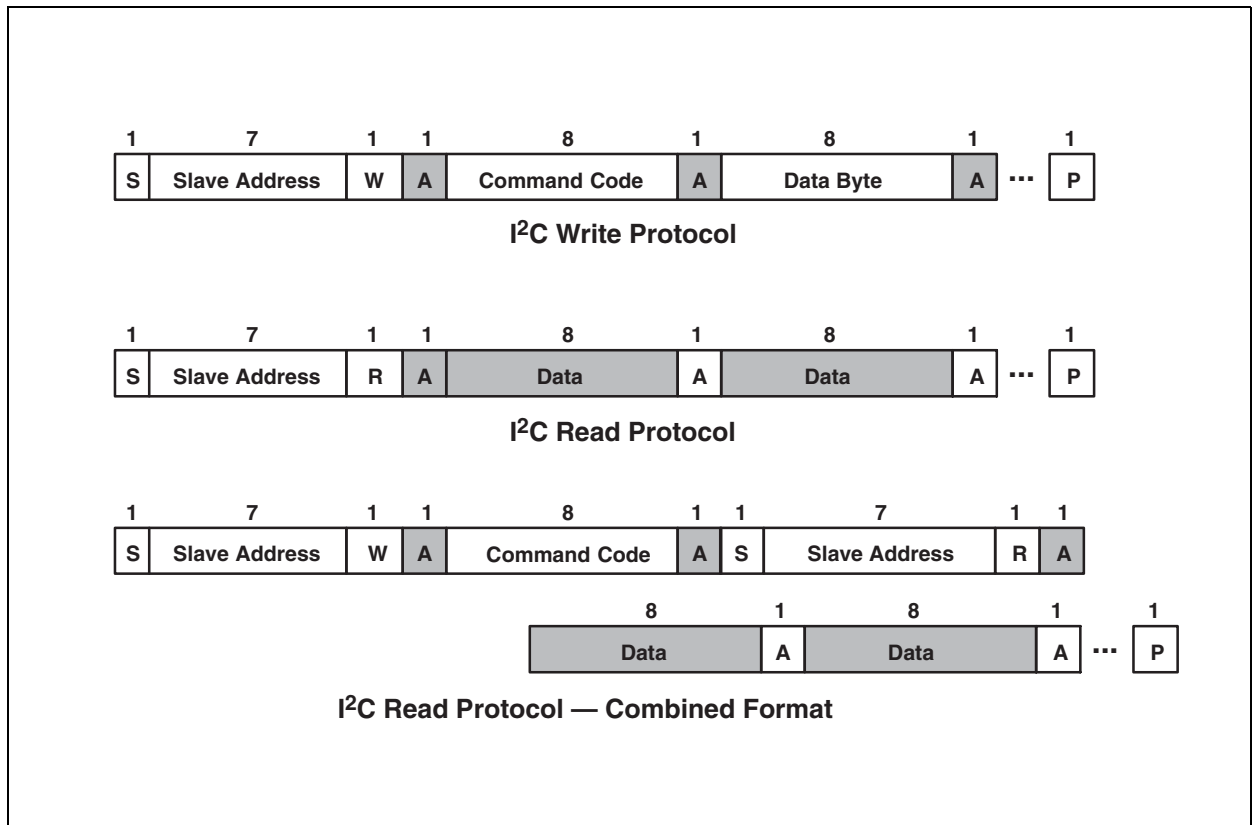
Register Set

The TSL2771 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 27.

Figure 27:
Register Address

Address	Register Name	R/W	Register Function	Reset Value
−−	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS ADC time	0xFF
0x02	PTIME	R/W	Proximity ADC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPCOUNT	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	CH0 ADC low data register	0x00
0x15	C0DATAH	R	CH0 ADC high data register	0x00
0x16	C1DATA	R	CH1 ADC low data register	0x00
0x17	C1DATAH	R	CH1 ADC high data register	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x18	PDATA	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I²C Protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

Command Register

The command registers specifies the address of the target register for future read and write operations.

Figure 28:
Command Register

7	6	5	4	3	2	1	0
COMMAND	TYPE		ADD				

Field	Bits	Description
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers: | FIELD VALUE	DESCRIPTION
---	---
00	Repeated byte protocol transaction
01	Auto-increment protocol transaction
10	Reserved — Do not use
11	Special function — See description below	 Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.
ADD	4:0	Address register/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for the following write and read transactions. The field values listed below apply only to special function commands: | FIELD VALUE	DESCRIPTION
---	---
00000	Normal - no action
00101	Proximity interrupt clear
00110	ALS interrupt clear
00111	Proximity and ALS interrupt clear
other	Reserved — Do not write	 ALS/Proximity Interrupt Clear clears any pending ALS/Proximity interrupt. This special function is self clearing.

Enable Register (0x00)

The ENABLE register is used to power the device ON/OFF, enable functions, and interrupts.

Figure 29:
Enable Register

7	6	5	4	3	2	1	0
Reserved		PIEN	AIEN	WEN	PEN	AEN	PON

Field	Bits	Description
Reserved	7:6	Reserved. Write as 0.
PIEN	5	Proximity interrupt mask. When asserted, permits proximity interrupts to be generated.
AIEN	4	ALS interrupt mask. When asserted, permits ALS interrupts to be generated.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	ALS Enable. This bit actives the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON[1][2]	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Note(s):

1. See Power Management section for more information.

2. A minimum interval of 2.72 ms must pass after PON is asserted before either a proximity or ALS can be initiated. This required time is enforced by the hardware in cases where the firmware does not provide it.

ALS Timing Register (0x01)

The ALS timing register controls the internal integration time of the ALS channel ADCs in 2.72 ms increments.

Figure 30:
ALS Timing Register

Field	Bits	Description			
ATIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.72 ms	1024
		0xF6	10	27.2 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	174 ms	65535
		0x00	256	696 ms	65535

Proximity Time Control Register (0x02)

The proximity timing register controls the integration time of the proximity ADC in 2.72 ms increments. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Figure 31:
Proximity Time Control Register

Field	Bits	Description			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.72 ms	1023

Wait Time Register (0x03)

Wait time is set 2.72 ms increments unless the WLONG bit is asserted in which case the wait times are 12x longer. WTIME is programmed as a 2's complement number.

Figure 32:
Wait Time Register

Field	Bits	Description			
WTIME	7:0	**REGISTER VALUE**	**WAIT TIME**	**TIME (WLONG = 0)**	**TIME (WLONG = 1)**
		0xFF	1	2.72 ms	0.032 s
		0xB6	74	201 ms	2.4 s
		0x00	256	696 ms	8.3 s

Note(s):

1. The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

ALS Interrupt Threshold Registers (0x04 - 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Figure 33:
ALS Interrupt Threshold Register

Register	Address	Bits	Description
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Registers (0x08 - 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Figure 34:
Proximity Interrupt Threshold Registers

Register	Address	Bits	Description
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTH	0x0B	7:0	Proximity high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions. ALS interrupts are generated using C0DATA.

Figure 35:
Persistence Register

7	6	5	4	3	2	1	0
PPERS				APERS			
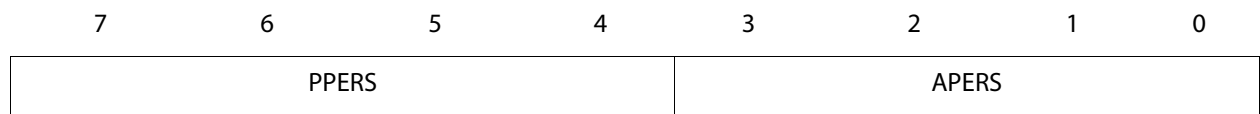
Field	Bits	Description
PPERS	7:4	Proximity interrupt persistence. Controls rate of proximity interrupt to the host processor <table><tr><th>FIELD VALUE</th><th>MEANING</th><th>INTERRUPT PERSISTENCE FUNCTION</th></tr><tr><td>0000</td><td>-----</td><td>Every proximity cycle generates an interrupt</td></tr><tr><td>0001</td><td>1</td><td>1 proximity value out of range</td></tr><tr><td>0010</td><td>2</td><td>2 consecutive proximity values out of range</td></tr><tr><td>…</td><td>…</td><td>…</td></tr><tr><td>1111</td><td>15</td><td>15 consecutive proximity values out of range</td></tr></table>

Field	Bits	Description		
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every proximity cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Figure 36:
Configuration Register

7	6	5	4	3	2	1	0
Reserved						WLONG	Reserved
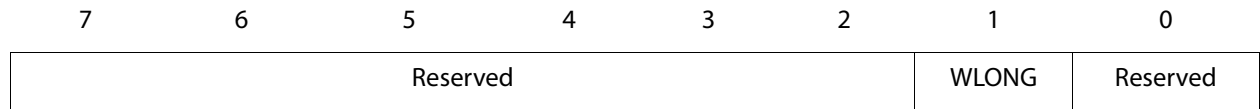
Field	Bits	Description
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12x from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that will be transmitted. When proximity detection is enabled, a proximity detect cycle occurs after each ALS cycle. PPULSE defines the number of pulses to be transmitted at a 62.5-kHz rate.

Note(s): The ATIME register will be used to time the interval between proximity detection events even if the ALS function is disabled.

Figure 37:
Proximity Pulse Count Register

7	6	5	4	3	2	1	0
PPULSE							
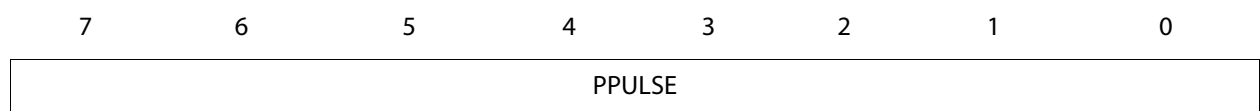
Field	Bits	Description
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Figure 38:
Control Register

7	6	5	4	3	2	1	0
PDRIVE		PDIODE		Reserved		AGAIN	
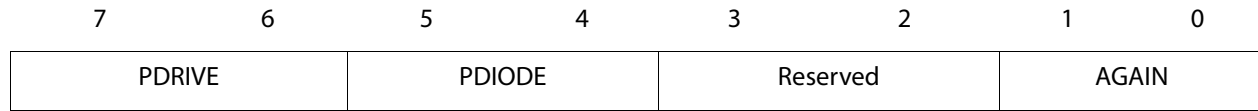
Field	Bits	Description	
PDRIVE	7:6	LED Drive Strength.	
		FIELD VALUE	**LED STRENGTH**
		00	100 mA
		01	50 mA
		10	25 mA
		11	12.5 mA
PDIODE	5:4	Proximity Diode Select.	
		FIELD VALUE	**DIODE SELECTION**
		00	Reserved
		01	Proximity uses the CH0 diode
		10	Proximity uses the CH1 diode
		11	Proximity uses both diodes
Reserved	3:2	Reserved. Write bits as zero (0:0)	
AGAIN	1:0	ALS Gain Control.	
		FIELD VALUE	**ALS GAIN VALUE**
		00	1x gain
		01	8x gain
		10	16x gain
		11	120x gain

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Figure 39:
ID Register

7	6	5	4	3	2	1	0
			ID				
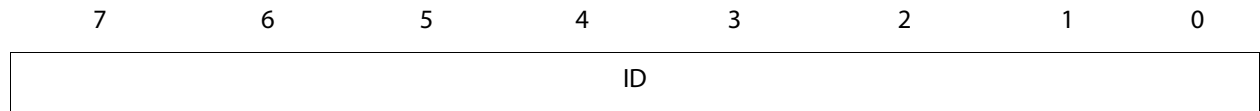
Field	Bits	Description	
ID	7:0	Part number identification	0x00 = TSL27711 & TSL27715
			0x09 = TSL27713 & TSL27717

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Figure 40:
Status Register

7	6	5	4	3	2	1	0
Reserved		PINT	AINT	Reserved			AVALID
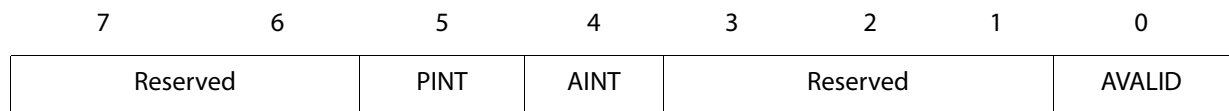
Field	Bit	Description
Reserved	7:6	Reserved.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:1	Reserved.
AVALID	0	ALS Valid. Indicates that the ALS channel has completed an integration cycle.

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ADC Channel Data Registers (0x14 - 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I²C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Figure 41:
ADC Channel Data Registers

Register	Address	Bits	Description
C0DATA	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATA	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Proximity Data Registers (0x18 - 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I²C transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

Figure 42:
PDATA Registers

Register	Address	Bits	Description
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Application Information Hardware

LED Driver Pin with Proximity Detection

In a proximity sensing system, the IR LED can be pulsed by the TSL2771 with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LED, the key goal can be meet. Place a 1-μF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LED anode, and a 22-μF capacitor at the output of the LED voltage regulator to supply the 100-mA current surge.

Figure 43:
Proximity Sensing Using Separate Power Supplies
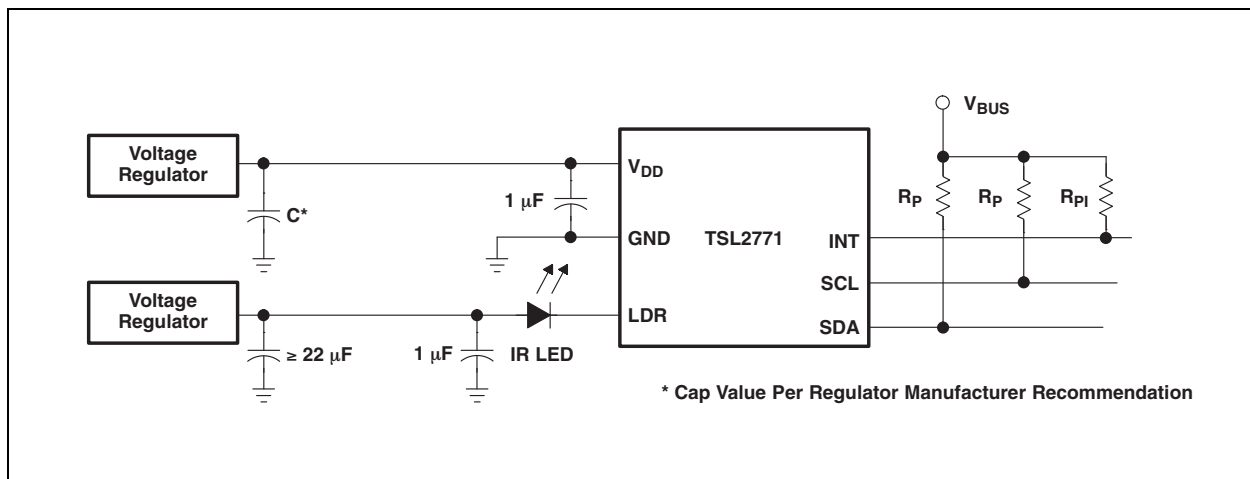
If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-μF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

Figure 44:
Proximity Sensing Using Single Power Supply

* Cap Value Per Regulator Manufacturer Recommendation
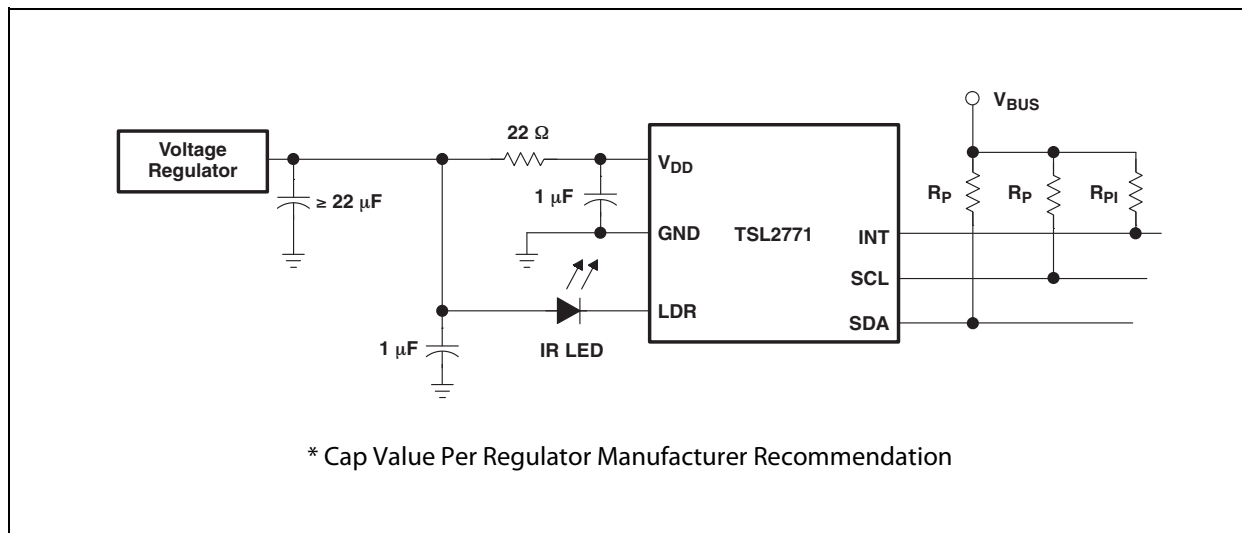
V_{BUS} in the above figures refers to the I²C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I²C bus voltage shown in the Ordering Information for the specific device being used.

The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_P) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The **ams** EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

PCB Pad Layouts

Suggested PCB pad layout guidelines for the Dual Flat No-Lead (FN) surface mount package are shown in Figure 45.

Note(s): Pads can be extended further if hand soldering is needed.

Figure 45:
Suggested FN Package PCB Layout
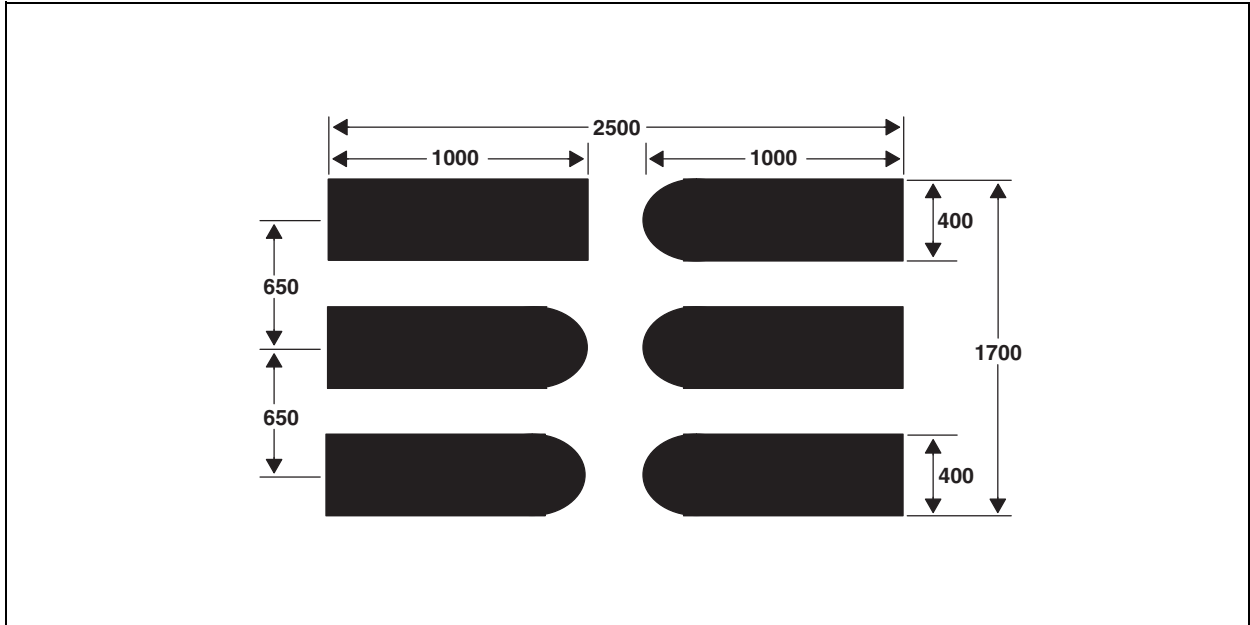
Note(s):

1. All linear dimensions are in micrometers.

2. This drawing is subject to change without notice.

Mechanical Data

Figure 46:
Package FN — Dual Flat No-Lead Packaging Configuration
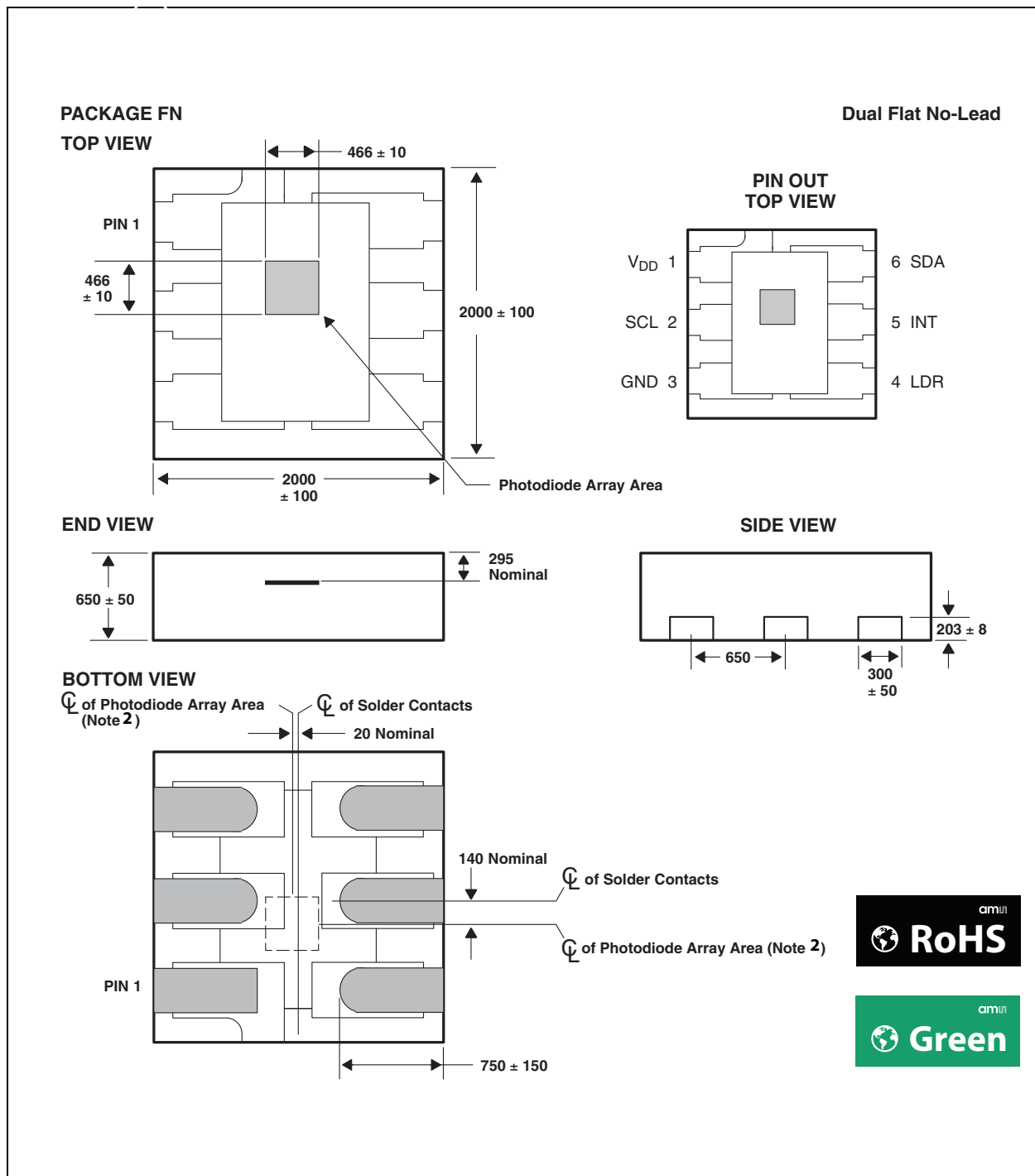
Note(s):

1. All linear dimensions are in micrometers. Dimension tolerance is ± 20µm unless otherwise noted.

2. The die is centered within the package within a tolerance of ±3 mils.

3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.

4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.

5. This package contains no lead (Pb).

6. This drawing is subject to change without notice.

Figure 47:
Package FN Carrier Tape

TOP VIEW

2.00 ± 0.05

4.00

4.00

1.75

∅ 1.50

8.00 $^{+\,0.30}_{-\,0.10}$

B

3.50 ± 0.05

∅ 1.00 ± 0.25

A   A

B

DETAIL A

DETAIL B

5° Max

0.254 ± 0.02

2.18 ± 0.05
A_O

5° Max

0.83 ± 0.05
K_O

2.18 ± 0.05
B_O
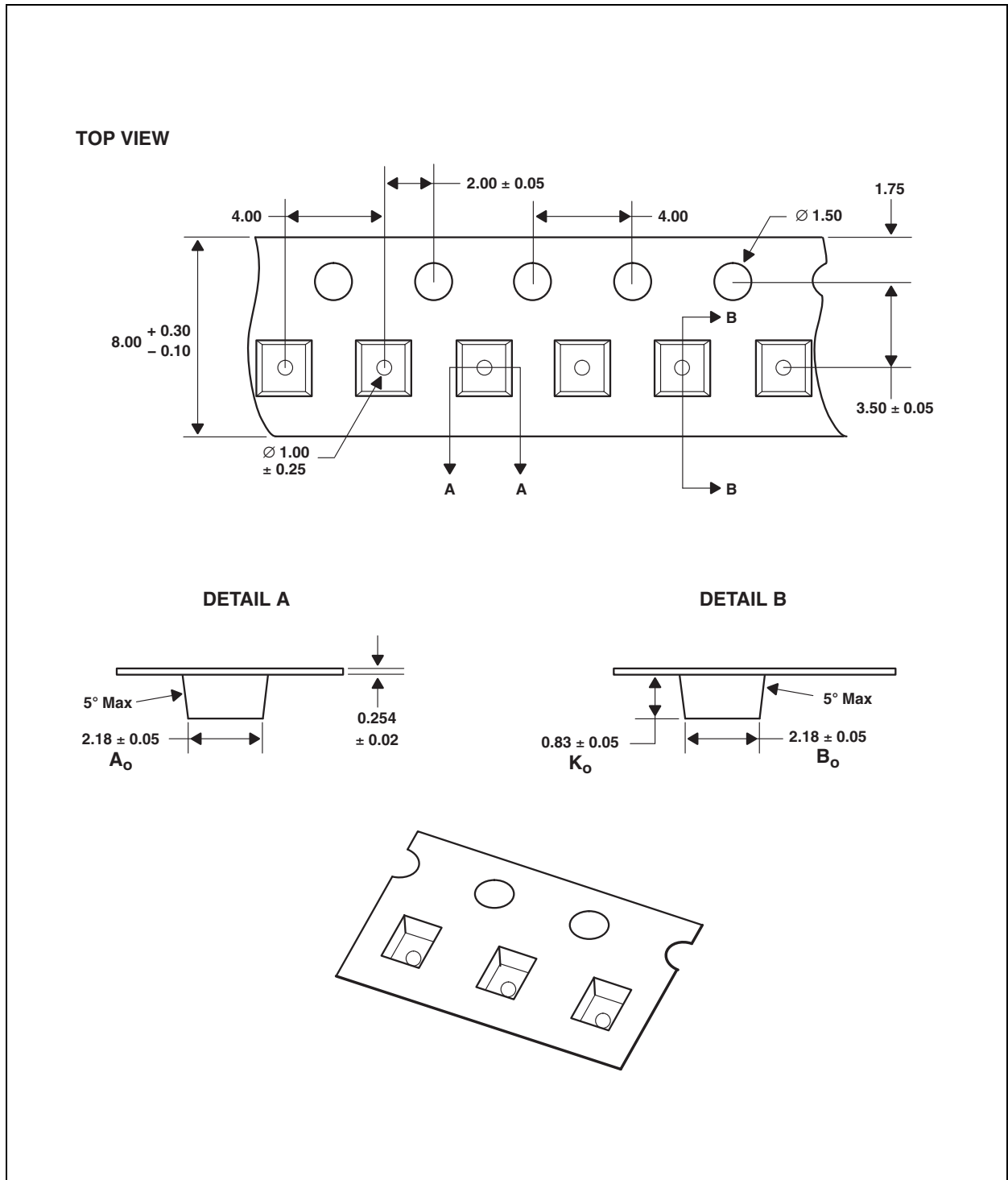
Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10 mm unless otherwise noted.

2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.

3. Symbols on drawing A_O, B_O, and K_O are defined in ANSI EIA Standard 481-B 2001.

4. Each reel is 178 millimeters in diameter and contains 3500 parts.

5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.

6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.

7. This drawing is subject to change without notice.

Manufacturing Information

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 48:
Soldier Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5°C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 s
Time above 230°C (T_2)	t_2	Max 50 s
Time above T_{peak} −10°C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max −5°C/s

Figure 49:
Solder Reflow Profile Graph
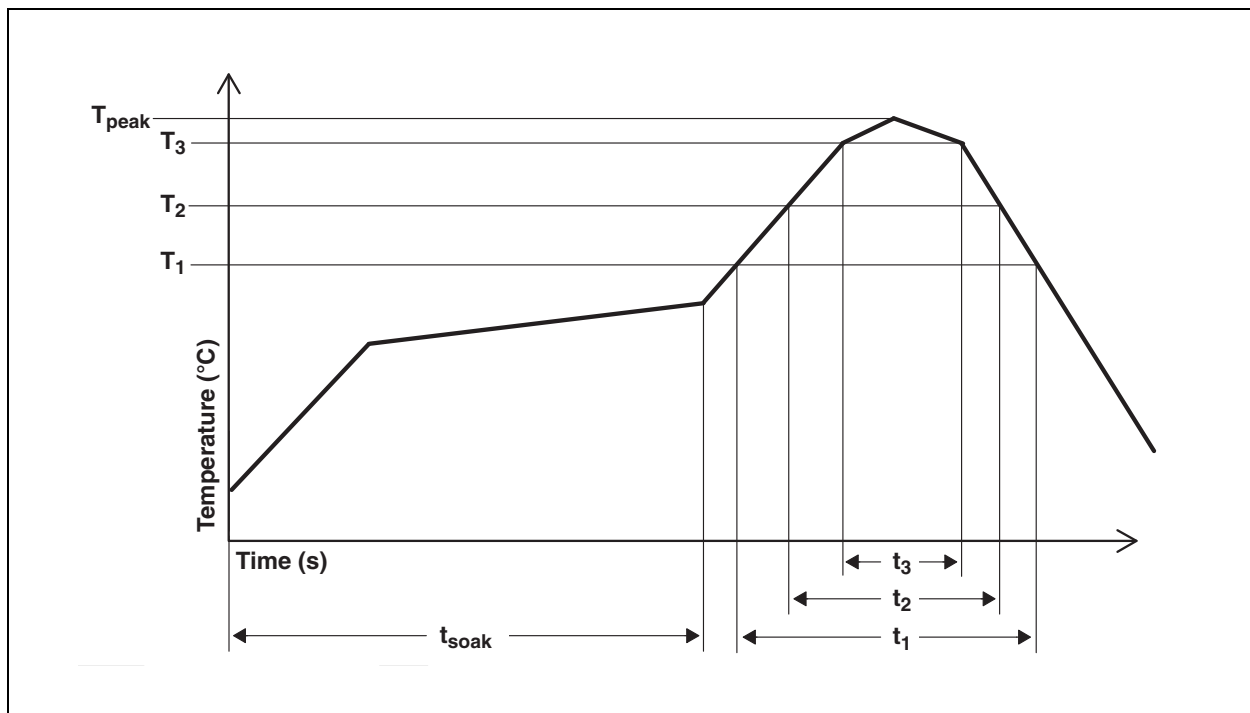
Note(s):

1. Note to scale – for reference only.

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is dry-baked prior to being packed for shipping. Devices are packed in a sealed aluminized envelope called a moisture barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

The FN package has been assigned a moisture sensitivity level of MSL 3 and the devices should be stored under the following conditions:

- Temperature Range: 5°C to 50°C

- Relative Humidity: 60% maximum

- Total Time: 12 months from the date code on the aluminized envelope — if unopened

- Opened Time: 168 hours or fewer

Rebaking will be required if the devices have been stored unopened for more than 12 months or if the aluminized envelope has been open for more than 168 hours. If rebaking is required, it should be done at 50°C for 12 hours.

Ordering & Contact Information

Figure 50:
Ordering Information

Ordering Code	Device	Address	Package - Leads	Interface Description
TSL27711FN	TSL27711	0x39	FN−6	I^{2}C Vbus = V$_{DD}$ Interface
TSL27713FN	TSL27713	0x39	FN−6	I^{2}C Vbus = 1.8 V Interface
TSL27715FN	TSL27715 [1]	0x29	FN−6	I^{2}C Vbus = V$_{DD}$ Interface
TSL27717FN	TSL27717 [1]	0x29	FN−6	I^{2}C Vbus = 1.8 V Interface

Note(s):

1. Contact **ams** for availability.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 100B (2011-Feb) to current revision 1-00 (2016-Mar-22)	Page
Content of TAOS datasheet was updated to latest **ams** design	

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision

2. Correction of typographical errors is not explicitly mentioned.

Content Guide