

# LM392

## Low Power Operational Amplifier and Comparator

The LM392 contains two functions: an op amp and a comparator. Both devices can operate on single-supply power and both have a common-mode range down to ground. Operation from split power supplies is also possible. Low power-supply current is independent of the supply voltage level. The output of the comparator interfaces directly with either TTL or CMOS logic. Low quiescent current makes the LM392 ideal for portable equipment.

### Features

- Wide Power-Supply Range: 3 V to 32 V
- Low Input Offset Voltage: 2 mV
- Low Quiescent Current: 600  $\mu$ A
- Input CMV Range includes GND
- Op Amp is Unity Gain Stable
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Level Detectors
- Voltage Controlled Oscillators
- Transducer Amplifiers



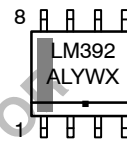
ON Semiconductor®

<http://onsemi.com>



SOIC-8 NB  
CASE 751

### MARKING DIAGRAM



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
• = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

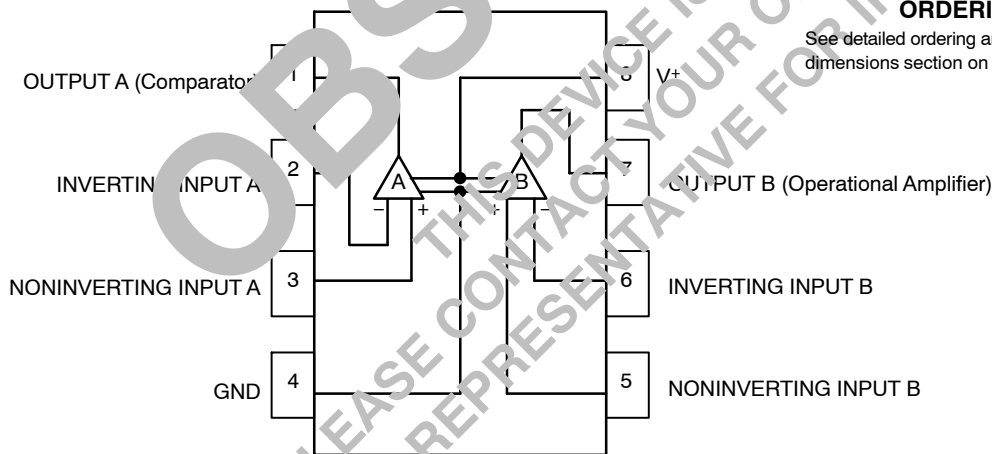


Figure 1. Logic Diagram and Pinout

## LM392

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_S$	32 or $\pm 16$	V
Differential Input Voltage	$V_{IDR}$	32	V
Input Voltage	$V_I$	0.3 to 32	V
Output Short – Circuit to Ground	$t_{SO}$	Continuous	
Thermal Impedance	$\theta_{JA}$	160	$^{\circ}\text{C}/\text{W}$
Storage Temperature Range	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$
Lead Temperature (Soldering, 10 Seconds)		260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**OBSOLETE**  
THIS DEVICE IS OBSOLETE  
PLEASE CONTACT YOUR ON SEMICONDUCTOR  
REPRESENTATIVE FOR INFORMATION

# LM392

## ELECTRICAL CHARACTERISTICS (Both Amplifiers) ( $V^+ = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Conditions	$T_A$	LM392			Unit
			Min	Typ	Max	
Input Offset Voltage	At output switch point, $V_O = 1.4\text{ V}$ , $R_S = 0\ \Omega$ , $V^+ = 5\text{ V}$ to $30\text{ V}$ , $V_{CM} = 0$ to $(V^+ - 1.5\text{ V})$	$25^\circ\text{C}$		$\pm 2$	$\pm 5$	mV
		$0^\circ\text{C}$ to $70^\circ\text{C}$			$\pm 7$	
Input Bias Current	IN(+) or IN(-), $V_{CM} = 0\text{ V}$	$25^\circ\text{C}$		50	205	nA
	IN(+) or IN(-)	$0^\circ\text{C}$ to $70^\circ\text{C}$			400	
Input Offset Current	IN(+) or IN(-)	$25^\circ\text{C}$		$\pm 5$	$\pm 50$	nA
		$0^\circ\text{C}$ to $70^\circ\text{C}$			$\pm 150$	
Input Common-Mode Voltage Range	$V^+ = 30\text{ V}$ (Note 1)	$25^\circ\text{C}$	0		$V^+ - 1.5$	V
		$0^\circ\text{C}$ to $70^\circ\text{C}$	0		$V^+ - 2$	
Supply Current	No Load	$V^+ = 30\text{ V}$		1	2	mA
		$V^+ = 5\text{ V}$		0.5	1	
Amplifier-to-Amplifier Coupling	$f = 1\text{ kHz}$ to $20\text{ kHz}$ , Input Referred	$25^\circ\text{C}$		-78		dB
Differential Input Voltage	All $V_{IN} \geq V$ (or $V^-$ , if Unclamped)	$0^\circ\text{C}$ to $70^\circ\text{C}$			32	V

## ELECTRICAL CHARACTERISTICS ( $V^+ = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Conditions	$T_A$	LM392			Unit
			Min	Typ	Max	
<b>OP AMP ONLY</b>						
Large Signal Voltage Gain	$V^+ = 5\text{ V}$ , $V_O$ Swing = $1\text{ V}$ to $11\text{ V}$ , $R_L = 2\text{ k}\Omega$	$25^\circ\text{C}$	20	100		V/mV
Output Voltage Swing, High ( $V_{OH}$ )	$R_L = 2\text{ k}\Omega$	$25^\circ\text{C}$		$V^+ - 1.7$		V
Output Voltage Swing, Low ( $V_{OL}$ )	$R_L = 2\text{ k}\Omega$	$25^\circ\text{C}$			20	mV
Common-Mode Rejection Ratio	$V_{CM} = 0$ to $V^+ - 1.5\text{ V}$	$25^\circ\text{C}$	65	70		dB
Power Supply Rejection Ratio		$25^\circ\text{C}$	65	100		dB
Output Current Source	$V_{IN(+)} = 1\text{ V}$ , $V_{IN(-)} = 0\text{ V}$ , $V^+ = 15\text{ V}$ , $V_O = 2\text{ V}$	$25^\circ\text{C}$	20	40		mA
Output Current Sink	$V_{IN(-)} = 1\text{ V}$ , $V_{IN(+)} = 0\text{ V}$ , $V^+ = 15\text{ V}$ , $V_O = 2\text{ V}$	$25^\circ\text{C}$	10	20		mA
	$V_{IN(-)} = 1\text{ V}$ , $V_{IN(+)} = 0\text{ V}$ , $V^+ = 15\text{ V}$ , $V_O = 200\text{ mV}$	$25^\circ\text{C}$	12	50		$\mu\text{A}$
Input Offset Voltage Drift	$R_S = 0\ \Omega$ ( $0^\circ\text{C}$ to $70^\circ\text{C}$ )	$0^\circ\text{C}$ to $70^\circ\text{C}$		7		$\mu\text{V}/^\circ\text{C}$
Input Offset Current Drift	$R_S = 0\ \Omega$ ( $0^\circ\text{C}$ to $70^\circ\text{C}$ )	$0^\circ\text{C}$ to $70^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$
<b>COMPARATOR ONLY</b>						
Voltage Gain	$R_L \geq 15\text{ k}\Omega$ , $V^+ = 15\text{ V}$	$25^\circ\text{C}$	50	200		V/mV
Large Signal Response Time	$V_{IN} = \text{TTL Logic Swing}$ , $V_{REF} = 1.4\text{ V}$ , $V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$	$25^\circ\text{C}$		200		ns
Response Time	$V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$	$25^\circ\text{C}$		600		ns
Output Sink Current	$V_{IN(-)} = 1\text{ V}$ , $V_{IN(+)} = 0\text{ V}$ , $V_O \geq 1.5\text{ V}$	$25^\circ\text{C}$	6	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4\text{ mA}$	$25^\circ\text{C}$		250	400	mV
	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4\text{ mA}$	$0^\circ\text{C}$ to $70^\circ\text{C}$			700	mV
Output Leakage Current	$V_{IN(-)} = 0$ , $V_{IN(+)} \geq 1\text{ V}$ , $V_O = 5\text{ V}$	$25^\circ\text{C}$		0.1		nA
	$V_{IN(-)} = 0$ , $V_{IN(+)} \geq 1\text{ V}$ , $V_O = 30\text{ V}$	$25^\circ\text{C}$			1.0	$\mu\text{A}$

1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V^+ - 1.5\text{ V}$ , but either or both inputs can go to 32 V without damage.

# LM392

## ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping <sup>†</sup>
LM392DR2G	0°C to +70°C	SOIC-8 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**OBSOLETE**  
THIS DEVICE IS OBSOLETE  
PLEASE CONTACT YOUR ON SEMICONDUCTOR  
REPRESENTATIVE FOR INFORMATION

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/> PIN 1. EMITTER<br/> 2. COLLECTOR<br/> 3. COLLECTOR<br/> 4. EMITTER<br/> 5. EMITTER<br/> 6. BASE<br/> 7. BASE<br/> 8. EMITTER</p>   | <p>STYLE 2:<br/> PIN 1. COLLECTOR, DIE, #1<br/> 2. COLLECTOR, #1<br/> 3. COLLECTOR, #2<br/> 4. COLLECTOR, #2<br/> 5. BASE, #2<br/> 6. EMITTER, #2<br/> 7. BASE, #1<br/> 8. EMITTER, #1</p>               | <p>STYLE 3:<br/> PIN 1. DRAIN, DIE #1<br/> 2. DRAIN, #1<br/> 3. DRAIN, #2<br/> 4. DRAIN, #2<br/> 5. GATE, #2<br/> 6. SOURCE, #2<br/> 7. GATE, #1<br/> 8. SOURCE, #1</p>                            | <p>STYLE 4:<br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. ANODE<br/> 4. ANODE<br/> 5. ANODE<br/> 6. ANODE<br/> 7. ANODE<br/> 8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/> PIN 1. DRAIN<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. DRAIN<br/> 5. GATE<br/> 6. GATE<br/> 7. SOURCE<br/> 8. SOURCE</p>   | <p>STYLE 6:<br/> PIN 1. SOURCE<br/> 2. DRAIN<br/> 3. DRAIN<br/> 4. SOURCE<br/> 5. SOURCE<br/> 6. GATE<br/> 7. GATE<br/> 8. SOURCE</p>  | <p>STYLE 7:<br/> PIN 1. INPUT<br/> 2. EXTERNAL BYPASS<br/> 3. THIRD STAGE SOURCE<br/> 4. GROUND<br/> 5. DRAIN<br/> 6. GATE 3<br/> 7. SECOND STAGE Vd<br/> 8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/> PIN 1. COLLECTOR, DIE #1<br/> 2. BASE, #1<br/> 3. BASE, #2<br/> 4. COLLECTOR, #2<br/> 5. COLLECTOR, #2<br/> 6. EMITTER, #2<br/> 7. EMITTER, #1<br/> 8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/> PIN 1. EMITTER, COMMON<br/> 2. COLLECTOR, DIE #1<br/> 3. COLLECTOR, DIE #2<br/> 4. EMITTER, COMMON<br/> 5. EMITTER, COMMON<br/> 6. BASE, DIE #2<br/> 7. BASE, DIE #1<br/> 8. EMITTER, COMMON</p> | <p>STYLE 10:<br/> PIN 1. GROUND<br/> 2. BIAS 1<br/> 3. OUTPUT<br/> 4. GROUND<br/> 5. GROUND<br/> 6. BIAS 2<br/> 7. INPUT<br/> 8. GROUND</p>  | <p>STYLE 11:<br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. DRAIN 2<br/> 7. DRAIN 1<br/> 8. DRAIN 1</p>   | <p>STYLE 12:<br/> PIN 1. SOURCE<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p>STYLE 13:<br/> PIN 1. N.C.<br/> 2. SOURCE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>  | <p>STYLE 14:<br/> PIN 1. N-SOURCE<br/> 2. N-GATE<br/> 3. P-SOURCE<br/> 4. P-GATE<br/> 5. P-DRAIN<br/> 6. P-DRAIN<br/> 7. N-DRAIN<br/> 8. N-DRAIN</p>   | <p>STYLE 15:<br/> PIN 1. ANODE 1<br/> 2. ANODE 1<br/> 3. ANODE 1<br/> 4. ANODE 1<br/> 5. CATHODE, COMMON<br/> 6. CATHODE, COMMON<br/> 7. CATHODE, COMMON<br/> 8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/> PIN 1. EMITTER, DIE #1<br/> 2. BASE, DIE #1<br/> 3. EMITTER, DIE #2<br/> 4. BASE, DIE #2<br/> 5. COLLECTOR, DIE #2<br/> 6. COLLECTOR, DIE #2<br/> 7. COLLECTOR, DIE #1<br/> 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/> PIN 1. VCC<br/> 2. V2OUT<br/> 3. V1OUT<br/> 4. TXE<br/> 5. RXE<br/> 6. VEE<br/> 7. GND<br/> 8. ACC</p>  | <p>STYLE 18:<br/> PIN 1. ANODE<br/> 2. ANODE<br/> 3. SOURCE<br/> 4. GATE<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. CATHODE<br/> 8. CATHODE</p>   | <p>STYLE 19:<br/> PIN 1. SOURCE 1<br/> 2. GATE 1<br/> 3. SOURCE 2<br/> 4. GATE 2<br/> 5. DRAIN 2<br/> 6. MIRROR 2<br/> 7. DRAIN 1<br/> 8. MIRROR 1</p>   | <p>STYLE 20:<br/> PIN 1. SOURCE (N)<br/> 2. GATE (N)<br/> 3. SOURCE (P)<br/> 4. GATE (P)<br/> 5. DRAIN<br/> 6. DRAIN<br/> 7. DRAIN<br/> 8. DRAIN</p>   |
| <p>STYLE 21:<br/> PIN 1. CATHODE 1<br/> 2. CATHODE 2<br/> 3. CATHODE 3<br/> 4. CATHODE 4<br/> 5. CATHODE 5<br/> 6. COMMON ANODE<br/> 7. COMMON ANODE<br/> 8. CATHODE 6</p>  | <p>STYLE 22:<br/> PIN 1. I/O LINE 1<br/> 2. COMMON CATHODE/VCC<br/> 3. COMMON CATHODE/VCC<br/> 4. I/O LINE 3<br/> 5. COMMON ANODE/GND<br/> 6. I/O LINE 4<br/> 7. I/O LINE 5<br/> 8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/> PIN 1. LINE 1 IN<br/> 2. COMMON ANODE/GND<br/> 3. COMMON ANODE/GND<br/> 4. LINE 2 IN<br/> 5. LINE 2 OUT<br/> 6. COMMON ANODE/GND<br/> 7. COMMON ANODE/GND<br/> 8. LINE 1 OUT</p> | <p>STYLE 24:<br/> PIN 1. BASE<br/> 2. EMITTER<br/> 3. COLLECTOR/ANODE<br/> 4. COLLECTOR/ANODE<br/> 5. CATHODE<br/> 6. CATHODE<br/> 7. COLLECTOR/ANODE<br/> 8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/> PIN 1. VIN<br/> 2. N/C<br/> 3. REXT<br/> 4. GND<br/> 5. IOUT<br/> 6. IOUT<br/> 7. IOUT<br/> 8. IOUT</p>   | <p>STYLE 26:<br/> PIN 1. GND<br/> 2. dv/dt<br/> 3. ENABLE<br/> 4. ILIMIT<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. VCC</p>  | <p>STYLE 27:<br/> PIN 1. ILIMIT<br/> 2. OVLO<br/> 3. UVLO<br/> 4. INPUT+<br/> 5. SOURCE<br/> 6. SOURCE<br/> 7. SOURCE<br/> 8. DRAIN</p>  | <p>STYLE 28:<br/> PIN 1. SW_TO_GND<br/> 2. DASIC_OFF<br/> 3. DASIC_SW_DET<br/> 4. GND<br/> 5. V_MON<br/> 6. VBULK<br/> 7. VBULK<br/> 8. VIN</p>  |
| <p>STYLE 29:<br/> PIN 1. BASE, DIE #1<br/> 2. EMITTER, #1<br/> 3. BASE, #2<br/> 4. EMITTER, #2<br/> 5. COLLECTOR, #2<br/> 6. COLLECTOR, #2<br/> 7. COLLECTOR, #1<br/> 8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/> PIN 1. DRAIN 1<br/> 2. DRAIN 1<br/> 3. GATE 2<br/> 4. SOURCE 2<br/> 5. SOURCE 1/DRAIN 2<br/> 6. SOURCE 1/DRAIN 2<br/> 7. SOURCE 1/DRAIN 2<br/> 8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)