

Low Voltage 1.2V/1.8V/2.5V CML 2:1 MUX 6.4 Gbps with Equalization

Features

- 1.2V/1.8V/2.5V CML 2:1 MUX
- Equalizes 9, 18, 27 inches of FR4
- Guaranteed AC Performance over Temperature and Voltage:
 - DC-to >6.4 Gbps Throughput
 - DC-to >4.5 GHz Clock Throughput
 - <280 ps Propagation Delay (IN-to-Q)
 - <20 ps Input Skew
 - <80 ps Rise/Fall Times
- Ultra-Low Jitter Design
 - 1 ps_{RMS} Cycle-to-Cycle Jitter
- High-Speed CML Outputs
- 2.5V ±5% V_{CC}, 1.2/1.8V/2.5V ±5% V_{CCO} Power Supply Operation
- Industrial Temperature Range: -40°C to +85°C
- Available In 16-Lead (3 mm x 3 mm) QFN Package

Applications

- Data Distribution
- SONET Clock and Data Distribution
- Fibre Channel Clock and Data Distribution
- Gigabit Ethernet Clock And Data Distribution

Markets

- Storage
- ATE
- Test and Measurement
- Enterprise Networking Equipment
- High-End Servers
- Metro Area Network Equipment

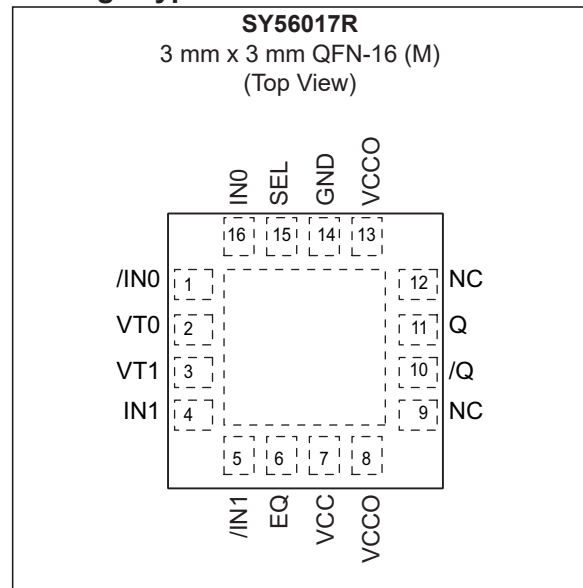
General Description

The SY56017R is a fully differential, low voltage 1.2V/1.8V/2.5V CML 2:1 MUX with input equalization. The SY56017R can process clock signals as fast as 4.5 GHz or data patterns up to 6.4 Gbps.

The differential input includes Microchip's unique, 3-pin input termination architecture that interfaces to CML differential signals, without any level-shifting or termination resistor networks in the signal path. The differential input can also accept AC-coupled LVPECL and LVDS signals. Input voltages as small as 200 mV (400 mV_{PP}) are applied before the 9", 18", or 27" FR4 transmission line. For AC-coupled input interface applications, an internal voltage reference is provided to bias the VT pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 80 ps.

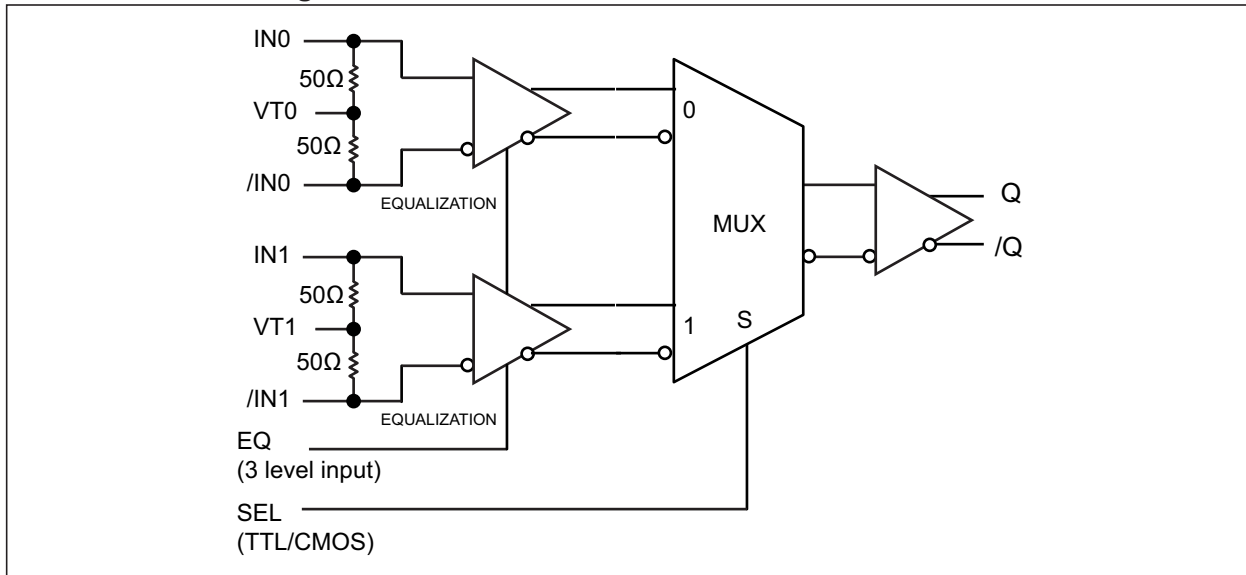
The SY56017R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V, or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY56017R is part of Microchip's high-speed, Precision Edge® product line.

Package Type



SY56017R

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC})	-0.5V to +3.0V
Supply Voltage (V_{CCO})	-0.5V to +3.0V
$V_{CC} - V_{CCO}$	<1.8V
$V_{CCO} - V_{CC}$	<0.5V
Input Voltage (V_{IN})	-0.5V to V_{CC}
CML Output Voltage (V_{OUT})	+0.6V to +3.0V
Current (I_T)		
Source or Sink on VT Pin	±100 mA
Input Current		
Source or Sink Current on, IN, /IN	±50 mA

Operating Ratings ††

Supply Voltage (V_{CC})	+2.375V to +2.625V
Supply Voltage (V_{CCO})	+1.14V to +2.625V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

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DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise stated. [Note 1](#)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	V_{CC}	2.375	2.5	2.625	V	V_{CC}
		1.14	1.2	1.26		V_{CCO}
		1.7	1.8	1.9		V_{CCO}
		2.375	2.5	2.625		V_{CCO}
Power Supply Current	I_{CC}	—	55	80	mA	Max. V_{CC}
Power Supply Current	I_{CCO}	—	16	21	mA	No load, V_{CCO}
Input Resistance (IN-to-VT, /IN-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	1.42	—	V_{CC}	V	IN, /IN
Input LOW Voltage (IN, /IN)	V_{IL}	1.22	—	$V_{IH} - 0.2$	V	IN, /IN, $1.22\text{V} = 1.7 - 0.475$
Input Voltage Swing (IN, /IN)	V_{IN}	0.2	—	1.0	V	See Figure 3-4 , (Note 2) applied to input of transmission line.
Differential Input Voltage Swing (IN - /IN)	V_{DIFF_IN}	0.4	—	2.0	V	See Figure 3-5 , (Note 2) applied to input of transmission line.
Voltage from Input to VT	V_{T-IN}	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: $V_{IN(MAX)}$ is specified when VT is floating.

CML OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CCO} = 1.14\text{V}$ to 1.26V $R_L = 50\Omega$ to V_{CCO} , $V_{CCO} = 1.7\text{V}$ to 1.9V , 2.375V to 2.625V , $R_L = 50\Omega$ to V_{CCO} or 100Ω across the outputs, $V_{CC} = 2.375\text{V}$ to 2.625V ; $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise stated. ([Note 1](#))

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	$V_{CC} - 0.02$	$V_{CC} - 0.01$	V_{CC}	V	$R_L = 50\Omega$ to V_{CCO}
Output Voltage Swing	V_{OUT}	300	390	475	mV	See Figure 3-4
Differential Output Voltage Swing	V_{DIFF_OUT}	600	780	950	mV	See Figure 3-5
Output Source Impedance	R_{OUT}	45	50	55	Ω	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.375V$ to $2.625V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input HIGH Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	—	—	0.8	V	—
Input HIGH Current	I_{IH}	-125	—	30	μA	—
Input LOW Current	I_{IL}	-300	—	—	μA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

THREE LEVEL EQ INPUT DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.375V$ to $2.625V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input HIGH Voltage	V_{IH}	$V_{CC} - 0.3$	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	0	—	$V_{EE} + 0.3$	V	—
Input HIGH Current	I_{IH}	—	—	400	μA	$V_{IH} = V_{CC}$
Input LOW Current	I_{IL}	-480	—	—	μA	$V_{IL} = GND$

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC0} = 1.14V$ to $1.26V$ $R_L = 50\Omega$ to V_{CC0} , $V_{CC0} = 1.7V$ to $1.9V$, $2.375V$ to $2.625V$, $R_L = 50\Omega$ to V_{CC0} or 100Ω across the outputs, $V_{CC} = 2.375V$ to $2.625V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Frequency	f_{MAX}	6.4	—	—	Gbps	NRZ (Data)
		4.5	—	—	GHz	$V_{OUT} \geq 200$ mV (Clock)
Propagation Delay IN-to-Q	t_{PD}	100	180	280	ps	Note 1, Figure 3-1
Propagation Delay SEL-to-Q		90	210	350	ps	Figure 3-1
Input-to-Input Skew	t_{SKEW}	—	—	20	ps	Note 2
Part-to-Part Skew		—	—	100	ps	Note 3
Random Jitter	t_{JITTER}	—	—	1	ps _{RMS}	Note 4
Crosstalk Induced Jitter		—	—	0.7	ps _{PP}	Note 5
Output Rise/Fall Time (20% to 80%)	t_r, t_f	20	50	80	ps	At full output swing

Note 1: Propagation delay is measured with no attenuating transmission line connected to the input.

2: Input-to-Input skew is the difference in time between both inputs and the output for the same temperature, voltage and transition.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Random jitter is measured with a K28.7 pattern, measured at $\leq f_{MAX}$.

5: Crosstalk induced jitter is defined as the added jitter that results from signals applied to the adjacent channel. It is measured at the output while applying a similar, differential clock frequencies that are asynchronous with respect to each other at the adjacent input.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	-40	—	+85	°C	—
Maximum Operating Junction Temperature	T_J	—	—	+125	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	-65	—	+150	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, 3x3 QFN-16Ld	θ_{JA}	—	75	—	°C/W	Still-air
	ψ_{JB}	—	33	—	°C/W	Junction-to-board

Note 1: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

$V_{CC} = 2.5V$, $V_{CCO} = 1.2V$, $GND = 0V$, $V_{IN} = 400\text{ mV}$, $R_L = 50\Omega$ to $1.2V$, Data Pattern: $2^{23}-1$, $T_A = +25^\circ C$, unless otherwise stated.

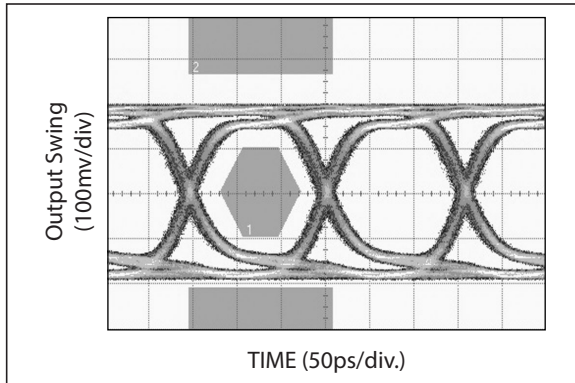


FIGURE 2-1: 6.4 Gbps, 24 inch FR4.

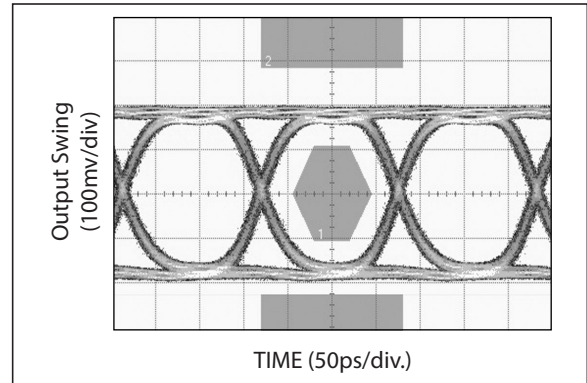


FIGURE 2-3: 6.4 Gbps, 9 inch FR4.

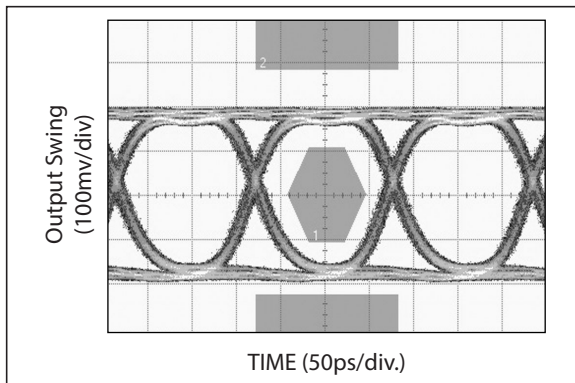


FIGURE 2-2: 6.4 Gbps, 18 inch FR4.

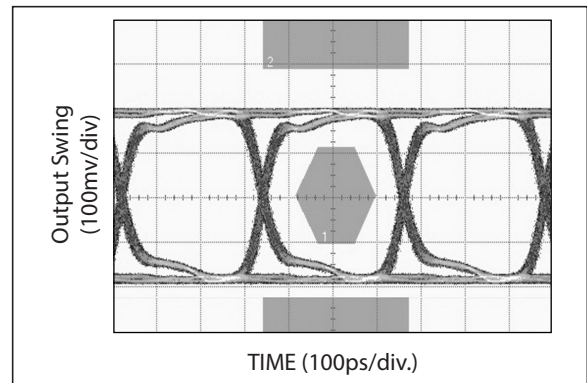


FIGURE 2-4: 3.2 Gbps, 24 inch FR4.

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
16, 1 4, 5	IN0, /IN0 IN1, /IN1	Differential Inputs: Signals as small as 200 mV V_{PK} (400 mV _{PP}) applied to the input of 9, 18, or 27 inches 6 mm FR4 stripline transmission line are then terminated with the differential input. Each input pin internally terminates with 50Ω to the VT pin.
2, 3	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC-coupling. For AC-coupling, bypass VT with 0.1 μF low ESR capacitor to VCC. See the Interface Applications section.
6	EQ	Three level input for equalization control. High, float, low. EQ pin applies the same EQ setting to both inputs.
15	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to a logic HIGH state if left open.
7	VCC	Positive Power Supply: Bypass with a 0.1 μF//0.01 μF low-ESR capacitor as close to the VCC pin as possible. Supplies input and core circuitry.
8, 13	VCCO	Output Supply: Bypass with 0.1 μF//0.01 μF low-ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers.
14	GND, Exposed Pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
11, 10	Q, /Q	CML Differential Output Pair: Differential buffered copy of the input signal. The output swing is typically 390 mV. See the Interface Applications section for termination information.

TABLE 3-2: TRUTH TABLE

SEL	Output
0	IN0 Input Selected
1	IN1 Input Selected

TABLE 3-3: TRUTH TABLE

EQ	Equalization
LOW	27"
FLOAT	18"
HIGH	9"

Timing Diagrams

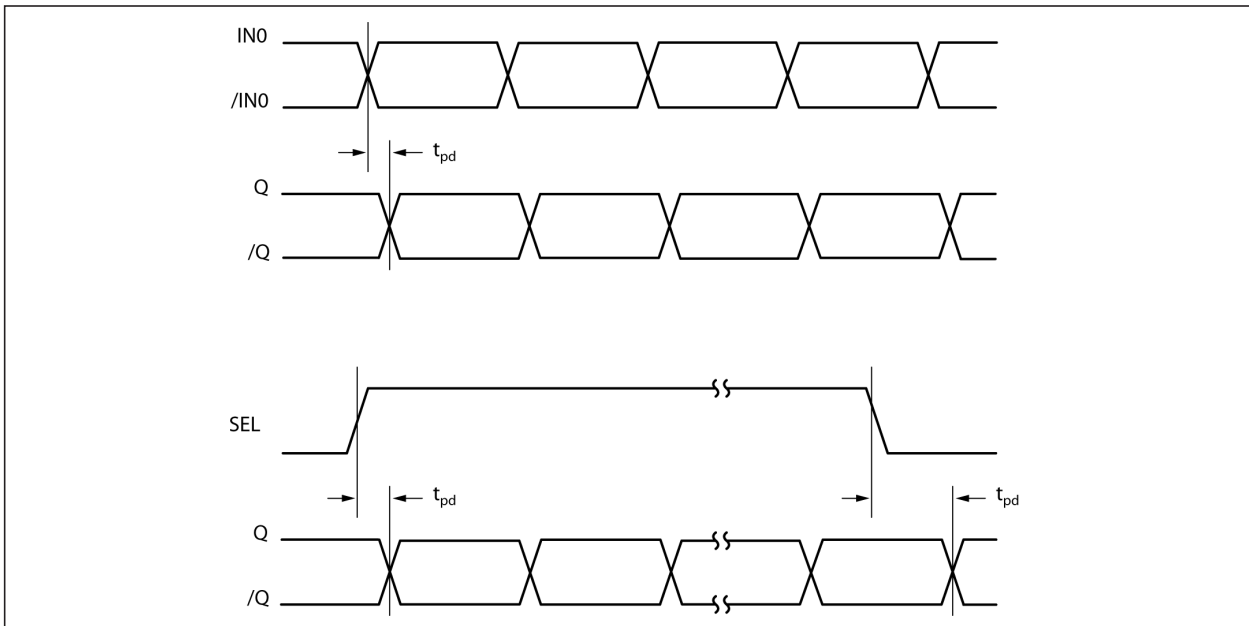


FIGURE 3-1: Propagation Delay.

Input and Output Stage

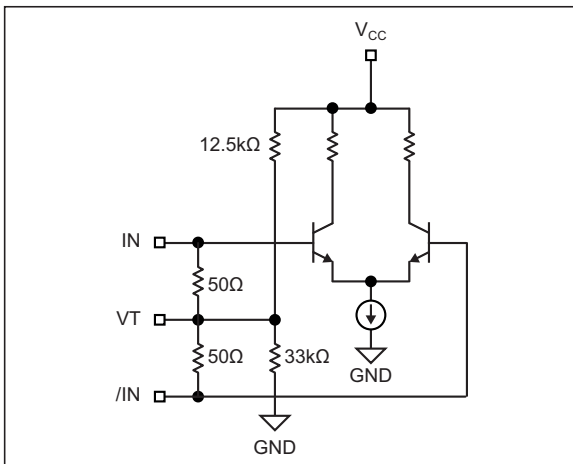


FIGURE 3-2: Simplified Differential Input Buffer.

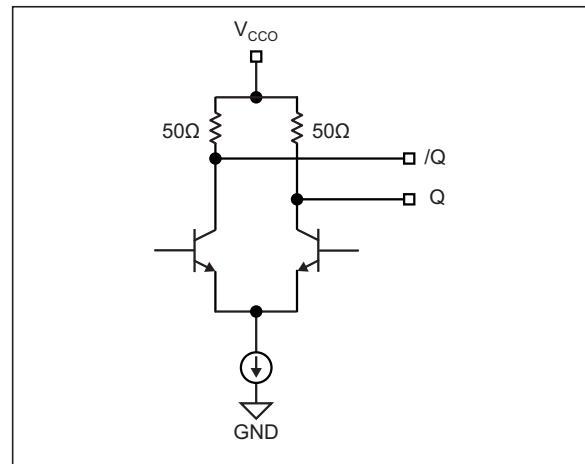


FIGURE 3-3: Simplified CML Output Buffer.

Single-Ended and Differential Swings

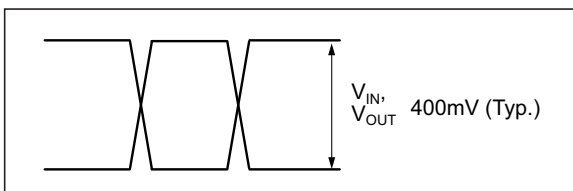


FIGURE 3-4: Single-Ended Swing.

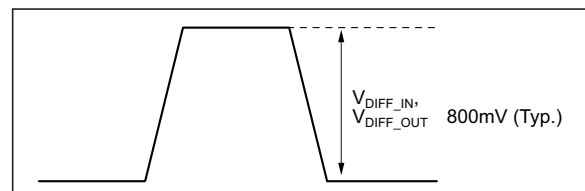


FIGURE 3-5: Differential Swing.

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4.0 INTERFACE APPLICATIONS

For Input Interface Applications see [Figure 4-1](#) through [Figure 4-5](#) and for CML Output Termination see [Figure 4-6](#) through [Figure 4-9](#).

4.1 Input Termination

1.8V CML driver: Terminate input with VT tied to 1.8V. Don't terminate 100Ω differentially.

2.5V CML driver: Terminate input with either VT tied to 2.5V or 100Ω differentially.

The input cannot be DC coupled from a 1.2V CML driver.

4.2 CML Output Termination with V_{CCO} 1.2V

For V_{CCO} of 1.2V, [Figure 4-6](#), terminate the output with 50Ω to 1.2V, not 100Ω differentially across the outputs. If AC-coupling is used, [Figure 4-9](#), terminate into 50Ω to 1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage. Any unused output pair needs to be terminated, do not leave floating.

4.3 CML Output Termination with V_{CCO} 1.8V

For V_{CCO} of 1.8V or 2.5V, [Figure 4-6](#) and [Figure 4-7](#), terminate with either 50Ω to 1.8V or 2.5V or 100Ω differentially across the outputs. AC- or DC-coupling is fine.

Input Interface Applications

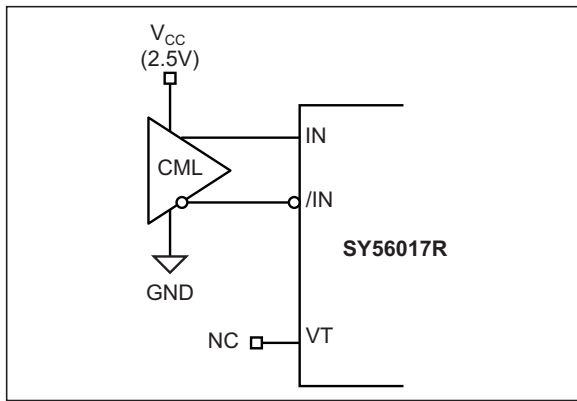


FIGURE 4-1: CML Interface (DC-Coupled, 2.5V, 100Ω Differential).

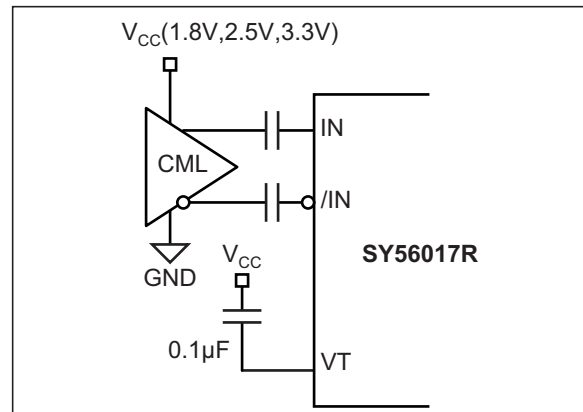


FIGURE 4-3: CML Interface (AC-Coupled).

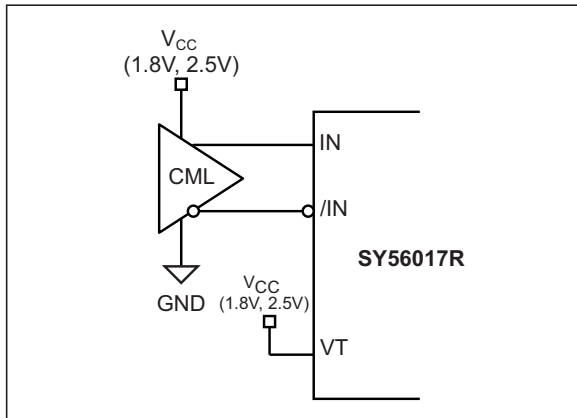


FIGURE 4-2: CML Interface (DC-Coupled, 1.8V, 2.5V, 50Ω to V_{CC}).

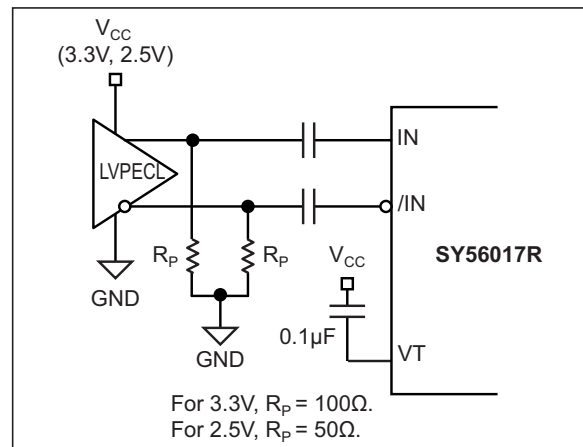


FIGURE 4-4: LVPECL Interface (AC-Coupled).

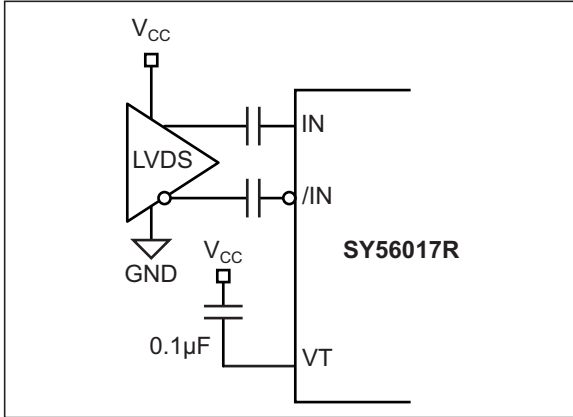


FIGURE 4-5: LVDS Interface (AC-Coupled).

CML Output Termination

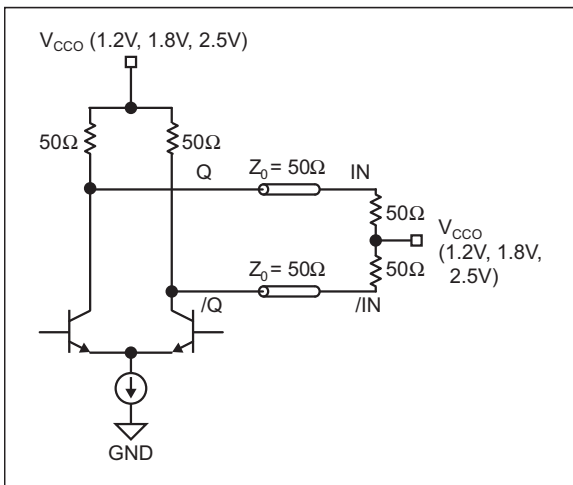


FIGURE 4-6: 1.2V, 1.8V, or 2.5V CML DC-Coupled Termination.

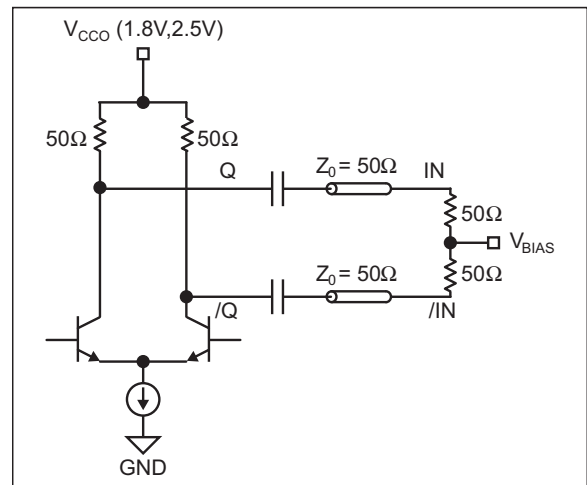


FIGURE 4-8: CML AC-Coupled Termination V_{CCO} 1.8V or 2.5V Only.

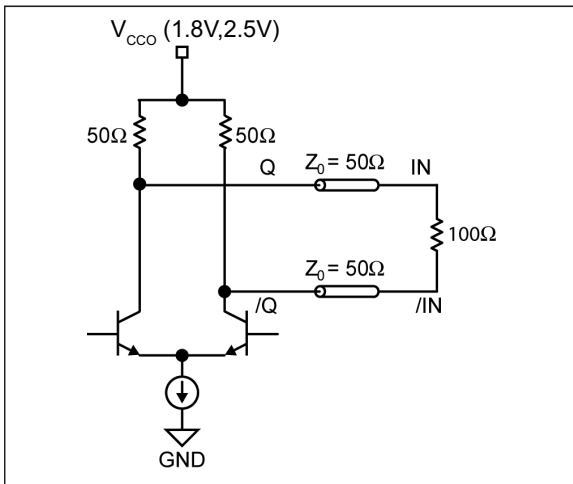


FIGURE 4-7: 1.8V or 2.5V CML DC-Coupled Termination.

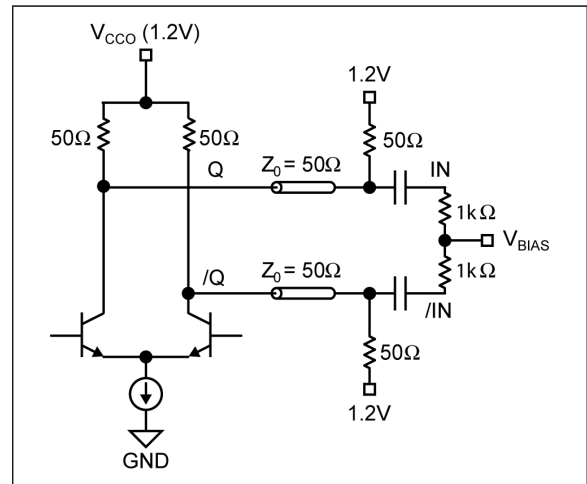


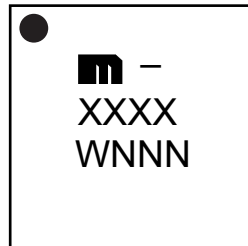
FIGURE 4-9: CML AC-Coupled Termination V_{CCO} 1.2V Only.

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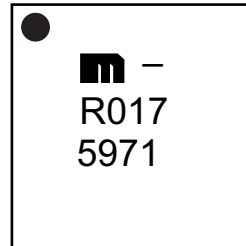
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

16-Lead QFN*

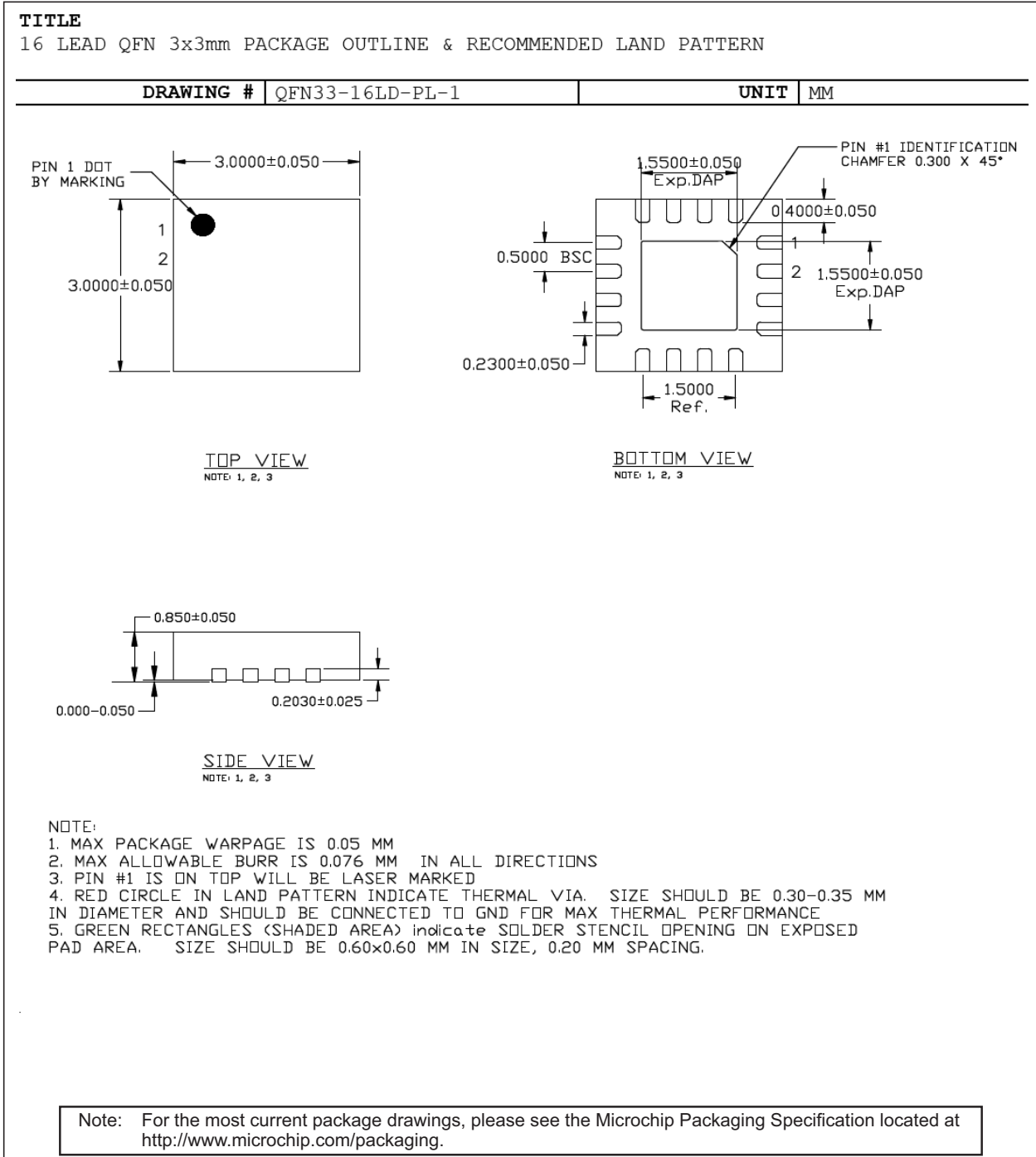


Example



<p>Legend: XX...X Product code or customer-specific information Y Year code (last digit of calendar year) YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code Ⓔ3 Pb-free JEDEC[®] designator for Matte Tin (Sn) * This package is Pb-free. The Pb-free JEDEC designator (Ⓔ3) can be found on the outer packaging for this package.</p> <p>●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).</p>
<p>Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.</p> <p>Underbar (¯) and/or Overbar (˘) symbol may not be to scale.</p>

16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

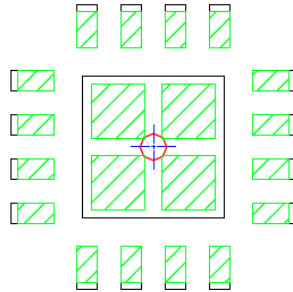


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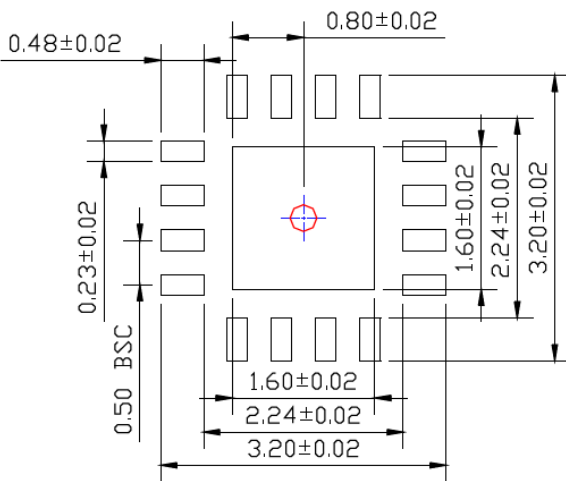
POD-Land Pattern drawing # QFN33-16LD-PL-1

RECOMMENDED LAND PATTERN

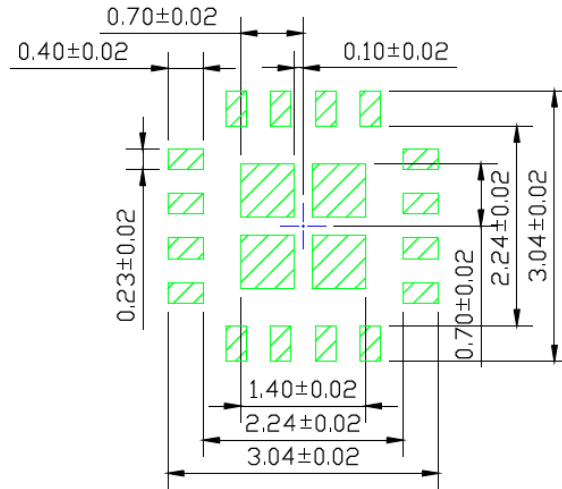
NOTE: 4, 5



STACKED-UP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (March 2020)

- Converted Micrel document SY56017R to Microchip data sheet template DS20006320A.
- Minor text changes throughout.

SY56017R

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>XX</u>
Device	Supply Voltage	Package	Temperature Range	Tape and Reel
Device:	SY56017:	Low Voltage 1.2V/1.8V/2.5V	CML 2:1 MUX	
			6.4 Gbps with Equalization	
Supply Voltage:	R	=	2.5V	
Package:	M	=	3 mm x 3 mm QFN-16	
Temperature Range:	G	=	-40°C to 85°C (NiPdAu Lead-Free)	
Special Processing:	<blank>	=	100/Tube	
	TR	=	1,000/Reel	

Examples:

- a) SY56017RMG: SY56017, 2.5V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 100/Tube
- b) SY56017RMG-TR: SY56017, 2.5V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, -40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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