LGA80D

Up to 80A
Digital DC-DC Convertor

Total Power: 200W
Input Voltage: 7.5-14Vdc
# of Outputs: Dual or Single

Special features

- 2 phase design
- DUAL or single output configuration possible.
- High Efficiency up to 95.5%
- Small size 1” x 0.5” x 0.48” (LxWxH)
- PMBus supporting
- No minimum load requirement
- Wide operating temperature range
- Exceptional power density
- Automatic loop compensation
- Excellent transient response
- Analogue or Digital control
- Tape and reel packaging
- Reflow compatible
- Possible to stack up to 8 phases for 320A
- 2 Years warranty

Safety

EN60950-1

Product Descriptions

The LGA80D power supply features a 7.5 to 14Vdc input voltage range and a 200W output power.

The LGA80D is a new design of high performance DC-DC converter. LGA80D has 2 phase design. It offers a total 200W output with just dimensions of 1.0”x0.5”x 0.48”. State-of the-art circuit topology provides a very high efficiency up to 95.5% which allows an operating temperature range of -40 ^{o}C to +85 ^{o}C .

Further features include remote On/Off, variable output voltage as well as overcurrent protection, over-voltage protection, and over-temperature protection.

Pin Function Description

PIN #	NAME	TYPE*	FUNCTION
1	Vin	PWR	Input positive power pin.
2	GND	PWR	Power ground pin.
3	PG1	O	Vo1 power-good output. Default is push-pull.
4	PG2	O	Vo2 power-good output. Default is push-pull.
5	EN1	I	Enable Vo1. Active signal enables LGA80D.
6	EN2	I	Enable Vo2. Active signal enables LGA80D.
7	SYNC	M/I/O	Clock synchronization input. Used to set the switching frequency. Refer to Switching Frequency Setting.
8	SHARE	I/O	Single-wire DDC bus (current sharing, LGA80Ds communication).
9	ADDR	M	Serial address select pin. Used to assign unique address for each individual device. Connect resistor to SGND. Refer to Address Setting.
10	SCL	I/O	Serial clock. Connect to external host and/or to other LGA80D.Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
11	SDA	I/O	Serial data. Connect to external host and/or to other LGA80D.Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
12	ALERT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5V to 5.5V source, the source must be always on.
13	SGND	PWR	Signal ground. All the external setting resistor, such as RSYNC, RADDR, RASCR, RCFG, RVtrimX, shall connect to SGND.
14	ASCRCFG	M	Control loop configuration settings. Refer to control Loop(ASCR) Setting.
15	CFG	M	Setting current sense, current limit and operating mode. Refer to Configuration Setting.
16	Vtrim1	M	Setting output voltage Vo1. Connect resistor to SGND. Refer to Output Voltage Setting.
17	VS1+	I	Differential output Vo1 voltage sense feedback. Connect to positive output regulation point.
18	VS1-	I	Differential output Vo1 voltage sense feedback. Connect to negative output regulation point.
19	Vtrim2	M	Setting output voltage Vo2. Connect resistor to SGND. Refer to Output Voltage Setting.
20	VS2-	I	Differential output Vo2 voltage sense feedback. Connect to negative output regulation point.
21	VS2+	I	Differential output Vo2 voltage sense feedback. Connect to positive output regulation point.
22	Vo1	PWR	Output Vo1 positive power pin.
23	Vo1	PWR	Output Vo1 positive power pin.
24	GND	PWR	Power ground pin.
25	Vo2	PWR	Output Vo2 positive power pin.
26	Vo2	PWR	Output Vo2 positive power pin.
27	GND	PWR	Power ground pin.
28	Vin	PWR	Input positive power pin.

***I = Input, O = Output, PWR = Power or Ground, M = Multimode pins.**

Electrical Specifications

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Absolute Maximum Ratings	Condition	Symbol	Min	Nom	Max	Unit
Input Voltage (DC continuous operation)		V_{IN}	-	-	15	V
Operating Ambient Temperature (*)		T_A	-40	-	+85	^oC
Storage Temperature		T_{STG}	-40	-	+125	^oC
Output Voltage		V_{out}	0.6	-	5.2	V
Logic I/O voltage: SHARE, EN1, EN2, PG1,PG2, SALRT, SCL, SDA, SYNC, VTRIM1, VTRIM2,CFG, ADDR			-0.3	-	6.0	V
Analog input voltages: VS1+, VS1-, VS2+, VS2-			-0.3	-	6.5	V

Note

(*) – At low temperatures, (at <-20degC), the accuracy of PMBus monitored parameters will be adversely affected.

Electrical Specifications

Typical values given at Vin=12V, switching frequency= 457KHz, 25^{o}C , unless otherwise specified under conditions.

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
Input						
Operating Input Voltage, DC (**)		V_{IN}	7.5	-	14	V
Maximum Input Current	Vin=7.5V, Vo=3.3V, Io = 60A, switching at 457kHz, with 200LFM at 55C	$I_{IN,\ MAX}$	-	-	33	A
Input current	Enable Off	I_{IN}	-	40	45	mA
Input Voltage UVLO Threshold(falling)	Default	UVLO	-	6.1	-	V
Input Voltage UVLO Threshold(rising)	Default	UVLO	-	6.8	-	V
Input Capacitance (internal)			-	120	-	uF
Input Capacitance (recommended external)	2x120uF/16V polymer cap (APXS160ARA121MH70G or equivalent) plus 4 x 10uF/16V ceramic cap		-	280	-	uF

Note

(**) - To maintain compliance to IPC9592B, input voltage must be kept at <13.2V

Electrical Specifications

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
LOGIC INPUT/OUTPUT						
Logic Input Leakage Current	Logic I/O - multimode pins		-100	-	100	nA
Logic Input Low, VIL			-	-	0.8	V
Logic Input High, VIH			2	-	-	V
Logic Output Low, VOL	2mA sinking		-	-	0.5	V
Logic Output High, VOH	2mA sourcing		2.25	-	-	V
Output						
Output voltage		V_{o1} V_{o2}	0.6	-	5.0	V
Output current	V_{o1} / V_{o2}=0.6V V_{o1} / V_{o2}=1.0V V_{o1} / V_{o2}=1.8V V_{o1} / V_{o2}=2.5V V_{o1} / V_{o2}=3.3V V_{o1} / V_{o2}=5.0V	I_{o1} I_{o2}	0	-	40 40 35 32.5 30 20	A
Output Power			-	-	200	W
Efficiency at 11V Vin & 25 ° C ambient	1.0V at 80A 1.8V at 70A 2.5V at 65A 3.3V at 60A 5.0V at 40A		- - - - -	89.9 93.0 94.5 95.0 95.5	- - - - -	%
Output Voltage Accuracy(Note 1)	With 1% Rvtrim resistor		-1	-	+1	%
Output Voltage Set-point Resolution (Note 2)	Set by PMBus™ command		-	±0.025	-	% Vo
Output Voltage Positive Sensing Bias Current	VS [1,2] + = 4V (negative = sinking)		-100	20	100	µA
Output Voltage Negative Sensing Bias Current	VS [1,2] - = 0V		-	20	-	µA
Line Regulation - 0.6 ~1.0V - 1.0 ~ 5.0V	Measured at Remote Sense point		-	2 0.2	-	mV %
Load Regulation - 0.6~1.0V - 1.0~5.0V	Measured at Remote Sense point		-	5 0.5	-	mV %

Electrical Specifications

Parameter	Conditions	Symbol	Min	Nom	Max	Unit
Output capacitor per output (external minimum)	2 x 220uF/6.3V Polymer Tan caps(6TPF220M5L or equivalent) 3 x 100uF/6.3V ceramic caps		-	740	-	uF
Output capacitor per output (external recommended)	4 x 330uF/6.3V Polymer Tan caps(T520D337M006ATE009 or equivalent) plus 10 x 100uF/6.3V ceramic caps		-	2320	-	uF
Ripple & Noise (with minimum caps) 5Hz to 20MHz - 0.6 to 1.8V - 2.5V to 3.3 - 5.0V	One module one output		- - -	15 25 40	- - -	mV
Ripple & Noise (with minimum caps) 5Hz to 20MHz - 0.6 to 1.8V - 2.5V to 3.3 - 5.0V	One module two outputs		- - -	18 35 50	- - -	mV
Ripple & Noise (with recommended caps) 5Hz to 20MHz - 0.6~1.8V - 2.5V to 3.3V - 5.0V	One module one output		- - -	10 16 27	- - -	mV
Ripple & Noise (with recommended caps) 5Hz to 20MHz - 0.6~1.8V - 2.5V to 3.3V - 5.0V	One module two outputs		- - -	12 20 32	- - -	mV
Transient response deviation (with recommended caps on 1 module two outputs configuration)	Vo=1V, 25% to 75% of step load, slew rate 1A/us		-	30	-	mV

Electrical Specifications

Parameter	Condition	Symbol	Min	Nom	Max	Unit
General						
Switching Frequency(Note 3)			400	457	800	kHz
PMBus™ Clock Frequency (Note 4)			100	-	400	kHz
Input Voltage Monitor Accuracy	Full Scale (FS) = 14V		-	+/-2	-	%FS
Input Voltage UV/OV Fault Response delay			-	100	-	µs
Power Good Vo Threshold	Default		-	90	-	%Vo
Power Good Vo Hysteresis	Default		-	5	-	%
Power-good Delay Applies to turn-on only (Low to High transition)	Default Set via PMBus™ command		- 0	1 -	- 5000	ms ms
Power good low voltage			-	-	0.5	V
CMTBF	Telcordia SR-332, issue 3, Method I Case I		50	-	-	MHours
Service Life	Calculated at 40 deg C		2			Years
Protection						
Over voltage	Default	OVP	-	110	-	% Vo
Over current(Note 5)	Refer to Configuration Setting on page 13	OCP	-	-	-	A
Over temperature	Default, refer to controller IC temperature	OTP	-	120	-	ºC

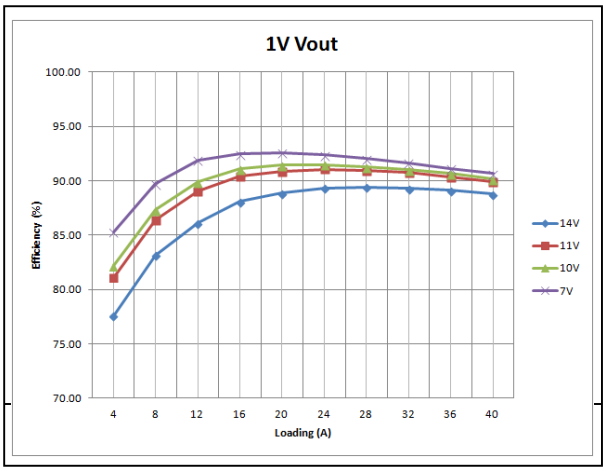
Note:

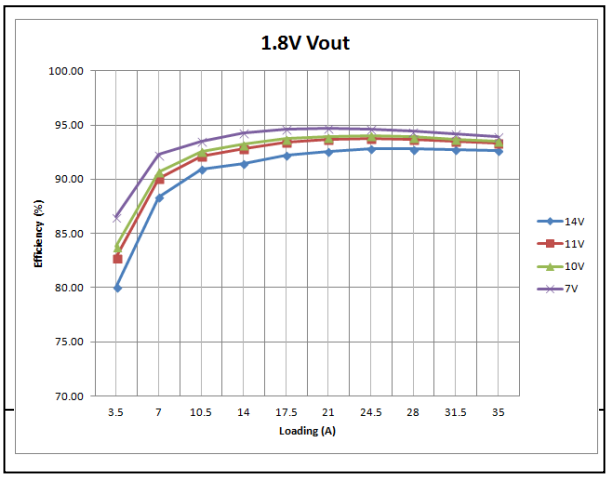
1. *VOUT measured at the termination of the VSx+ and VSx- sense points across line, load, temperature variation.*
2. *Percentage of Full Scale (FS) with temperature compensation applied.*
3. *Switching frequency will affect the thermal performance, the thermal derating will be no the same at different switching frequency.*
4. *For operation at 400kHz, see PMBus™ Power System Management Protocol Specification for timing parameter limits.*
5. *The OCP set point applies per phase. The total OCP current value will be twice the set value.*

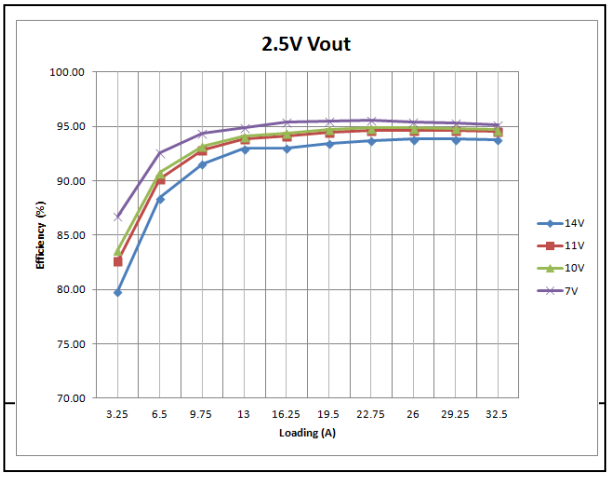
LGA80D Performance Curves

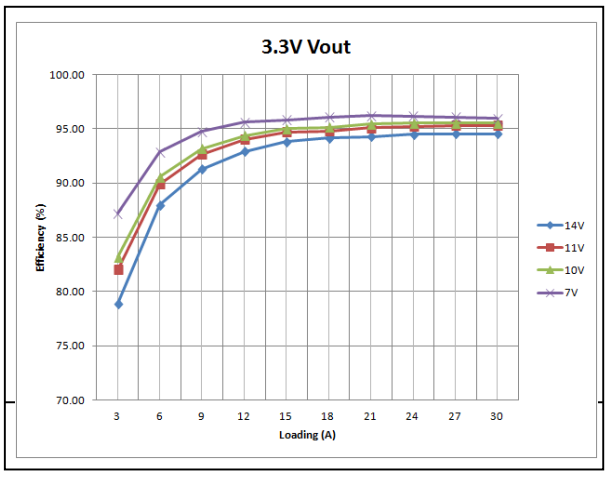
Efficiency

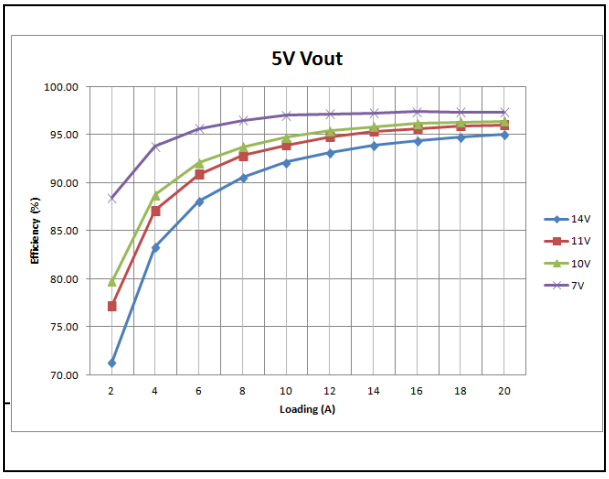
Tested at 200LFM room temp





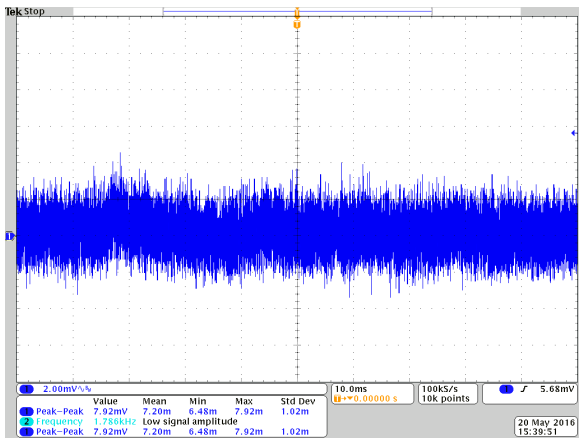




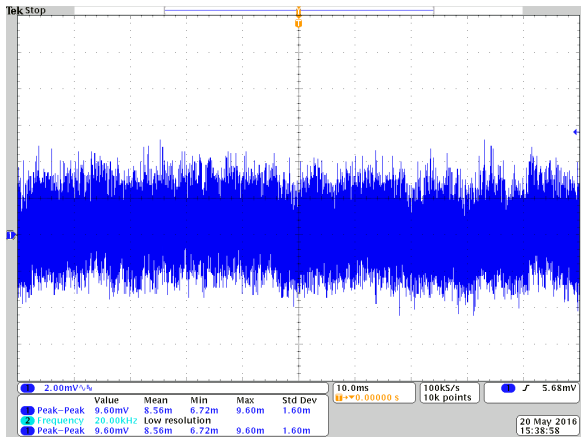


LGA80D Performance Curves

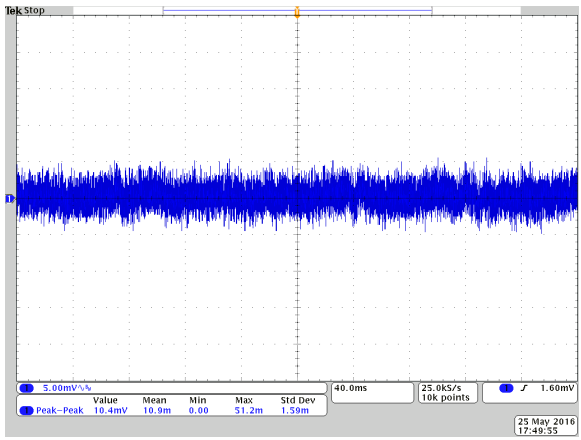
Ripple @ 12V Vin/ full load with recommended capacitance on 1 module 1 output (2 phases) configuration



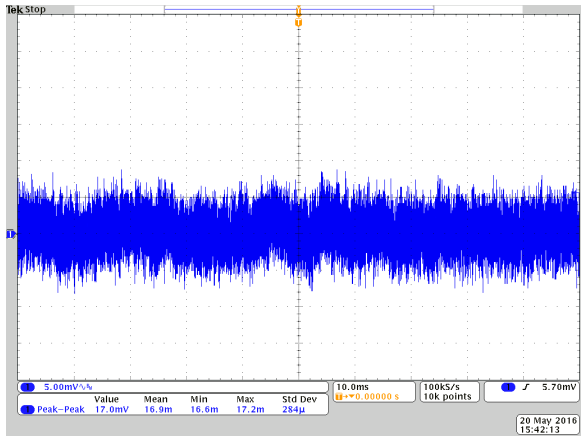
0.6V Vo



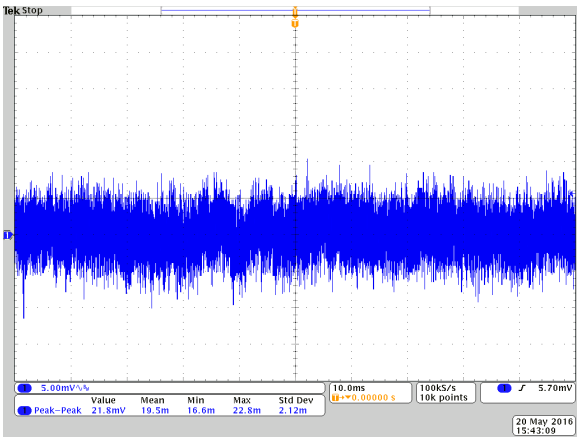
1.0V Vo



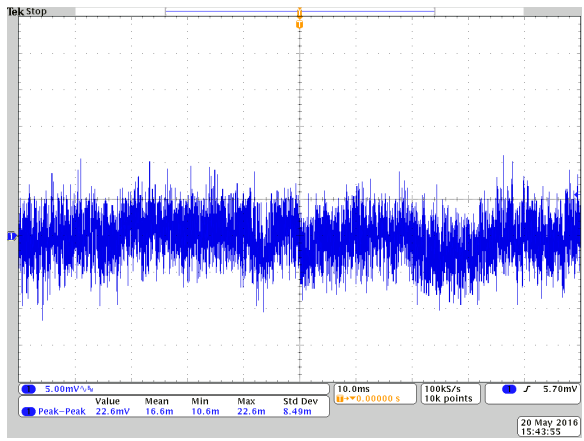
1.8V Vo



2.5V Vo

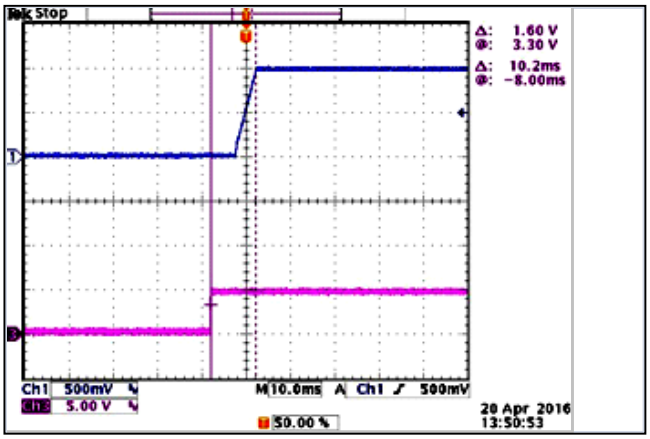


3.3V Vo

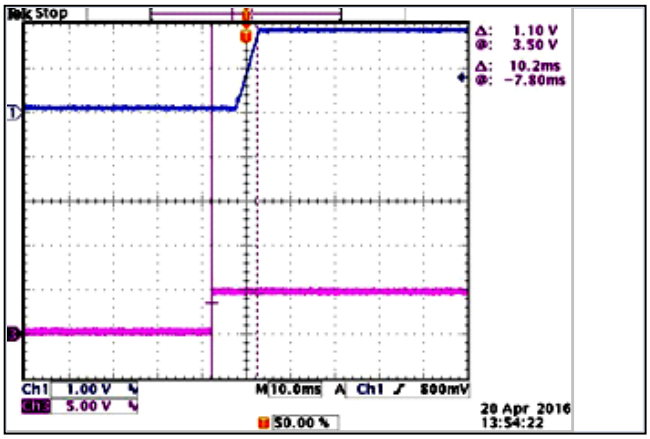


5.0V Vo

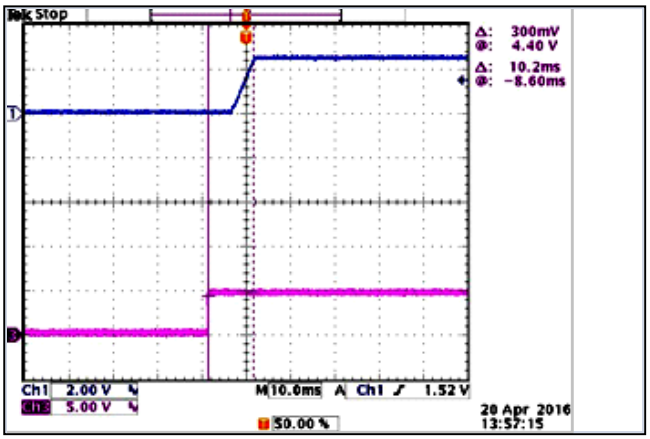
Startup _@ 12V Vin/ full load with recommended capacitance on 1 module 1 output (2 phases) configuration
CH1: Vout CH2: Enable



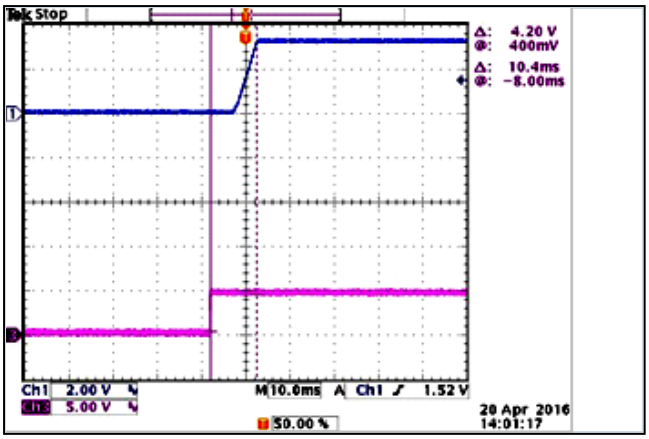
1.0V Vo



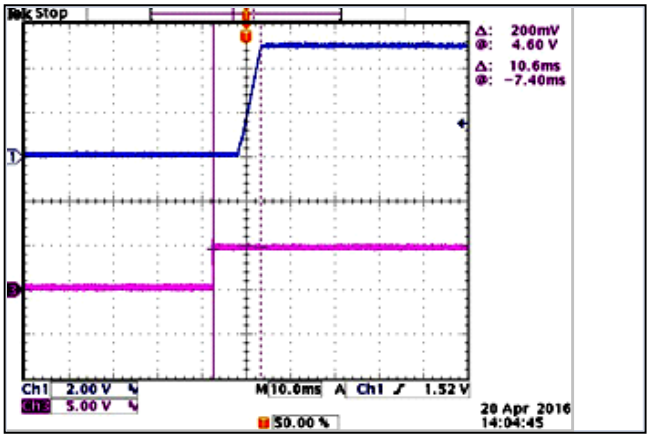
1.8V Vo



2.5V Vo

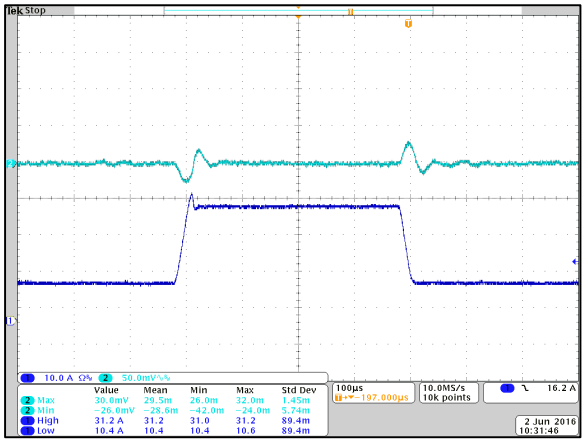


3.3V Vo

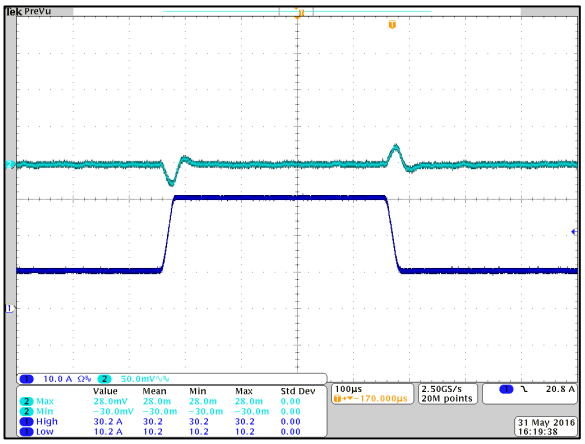


5.0V Vo

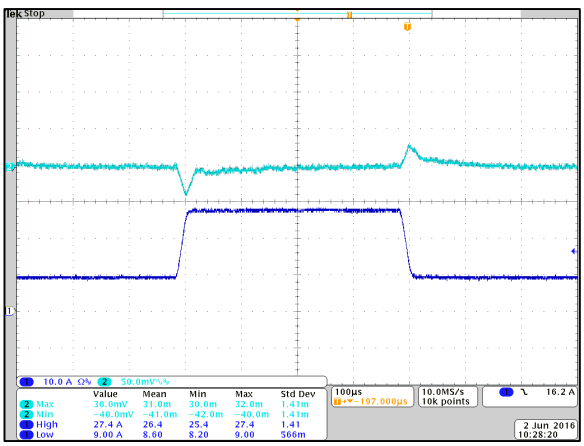
Dynamic @ 12V Vin/ full load with recommended capacitance on 1 module 2 output s configuration
CH1: Iout, CH2: Vout
12V Vin, 25%~75%~25% step load, 1A/us
4 x 330uF/6.3V/6mohm+10 x 100uF/6.3V ceramic caps



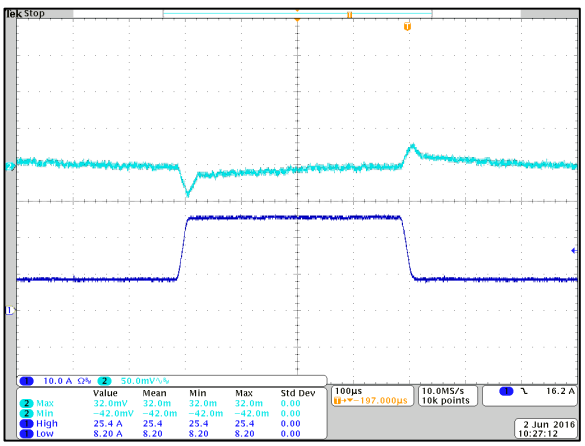
0.6 V



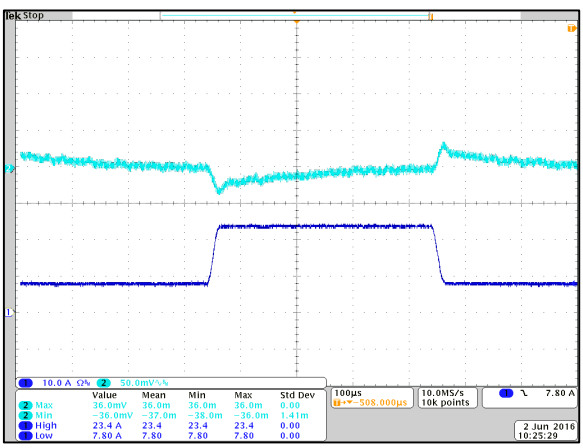
1.0 V



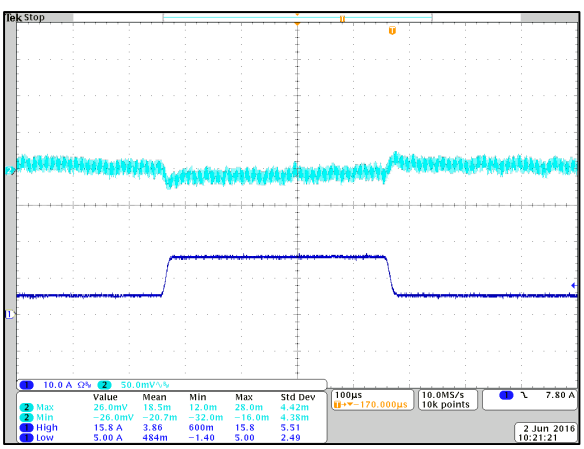
1.8 V



2.5 V



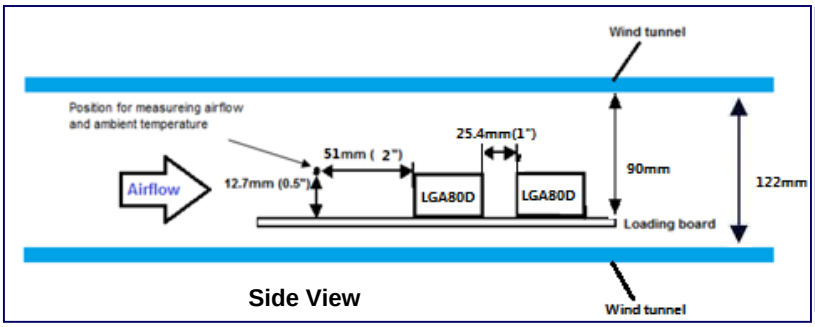
3.3 V

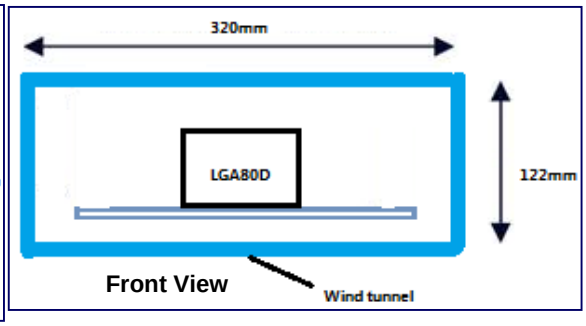


5.0 V

Thermal Test Setup

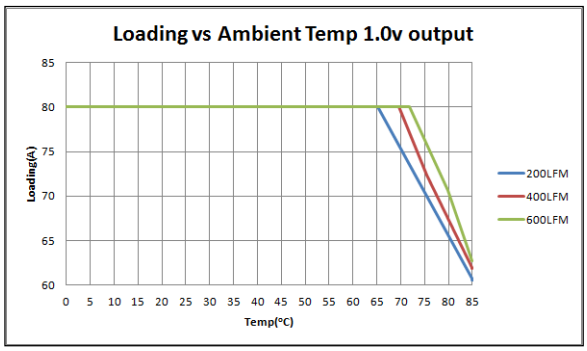
The following figure shows the wind tunnel setup. The LGA80D modules are mounted on a test board and is vertically positioned within the wind tunnel.

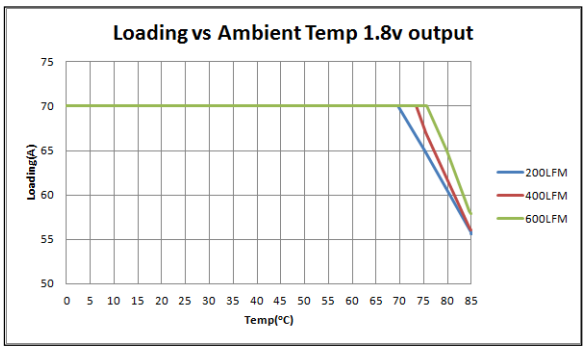


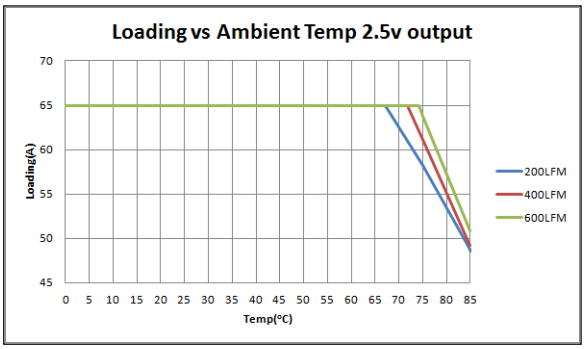


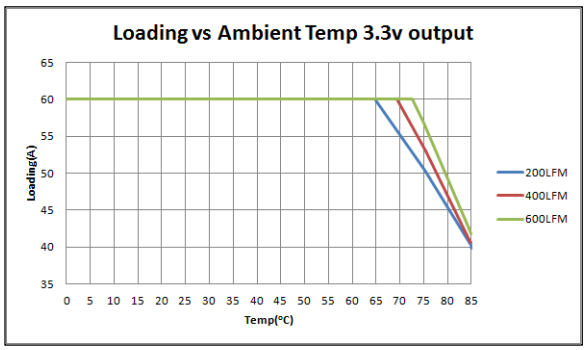
Thermal Derating Curve (Two LGA80Ds with longitudinal airflow)@ 12V Vin

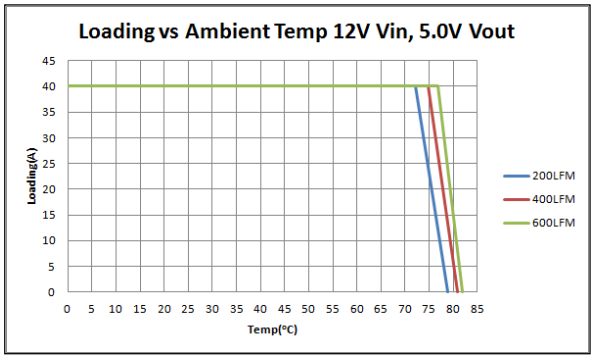
Note: One LGA80D temperature is better than two LGA80Ds











Technical Reference Note

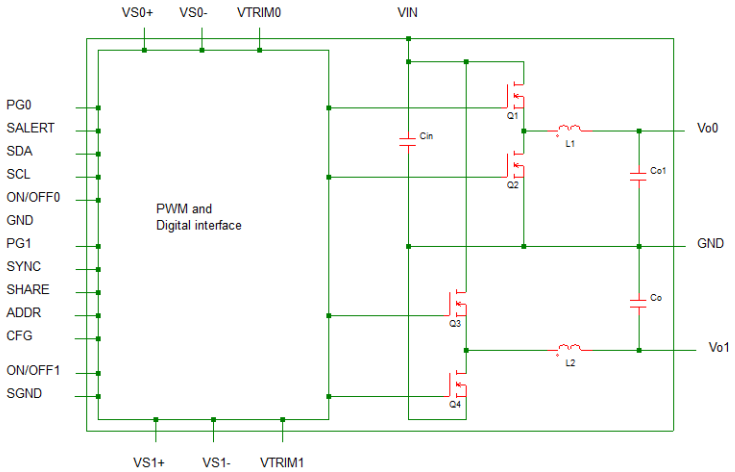
Electrical Description

The LGA80D is designed with a voltage mode dual-phase synchronous buck topology and the block diagram is shown in Figure 1.

The output voltage is adjustable over a range of 0.6 – 5.0 V by using an external resistor or voltage as described on Page 8.

The POL module can be shut down via the ENABLE input pin. The module is enabled when the ENABLE pin is in logic high, and disabled when it is in logic low.

The output is monitored for over current and short-circuit conditions. When the PWM controller detects an over current condition, it forces the module into the defaulted latch mode.



Note: LGA80D shall be protected with a fuse in the positive input path.

Wide Operating Temperature Range

The LGA80D's ability to accommodate a wide range of ambient temperatures is the result of its extremely high power conversion efficiency and resultant low power dissipation, combined with the excellent thermal performance of the thermally enhanced cover. The maximum output power that the module delivers will depend on a number of parameters, primarily:

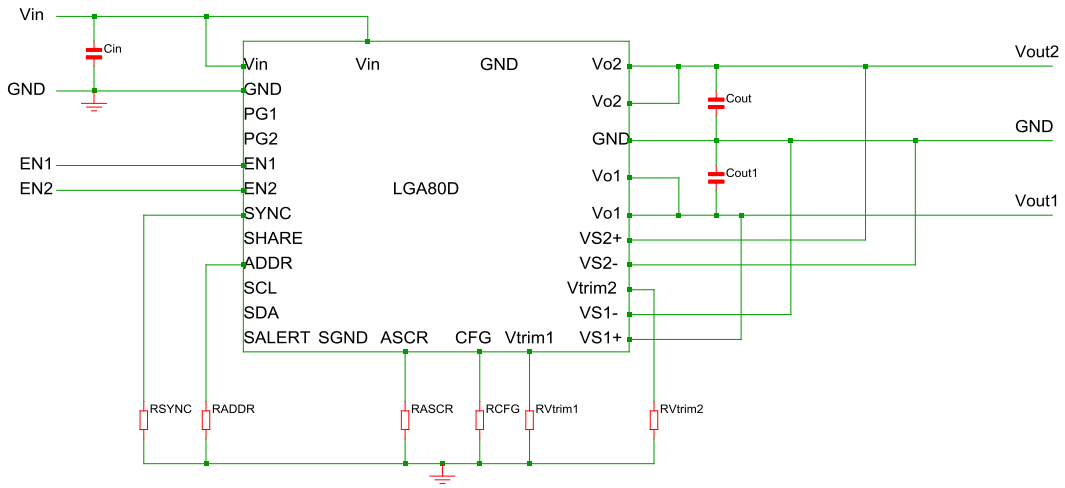
Input voltage range

Output load current

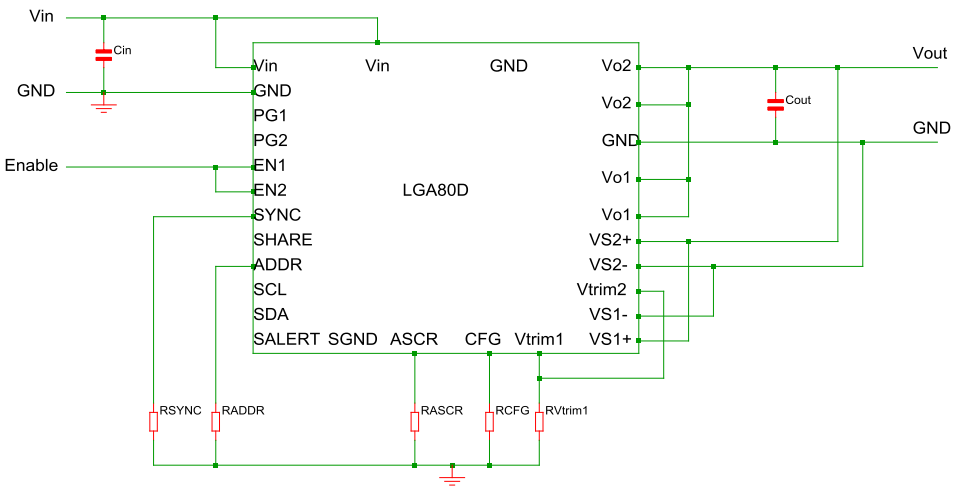
Air velocity (forced or natural convection)

The LGA80D module has an operating temperature range of -40 ° C to 85 ° C with suitable derating.

Typical applications

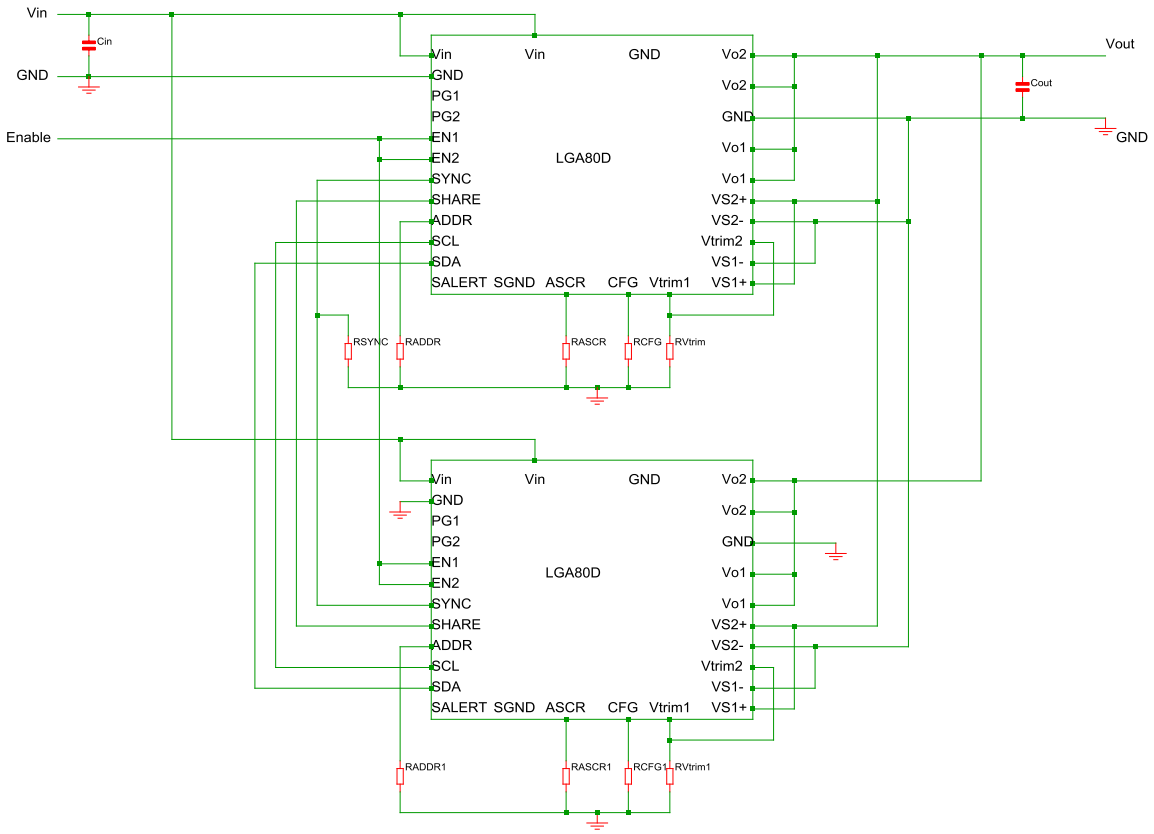


One Module Two Outputs



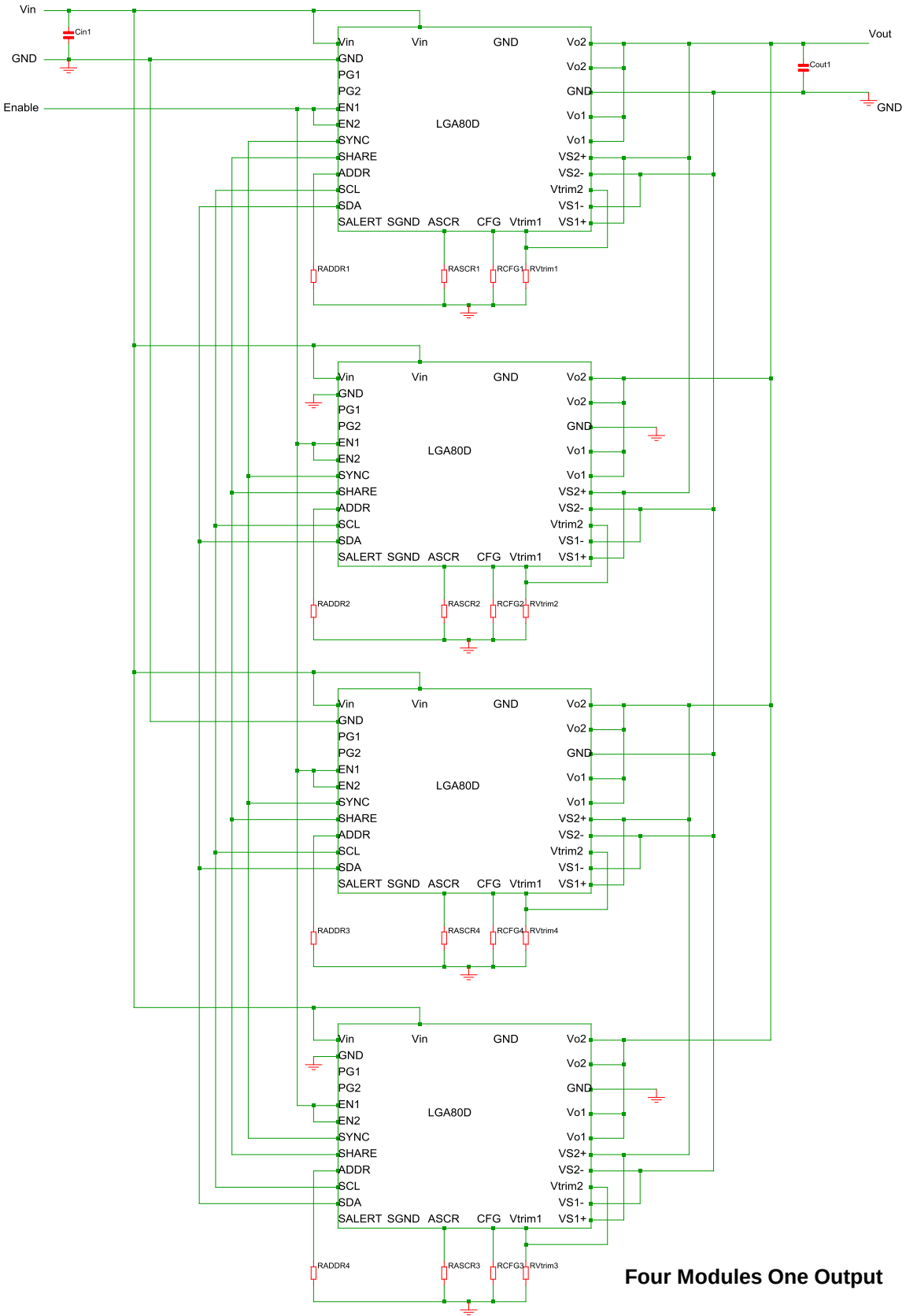
One Module One Output

Typical applications



Two Modules One Output

Typical applications



Four Modules One Output

Features and Functions

Output Voltage Setting

The output voltage is adjustable from 0.6 – 5.0 V. The outputs V_{out1} and V_{out2} can be adjusted with an external resistor RVtrim placed between the “Vtrim1 or Vtrim2” and “GND” pin shown in Table 3. V_{out1} and V_{out2} can also be set by GUI/PMBus up to 5.2V.

RVtrim(kΩ)	VOUT(V)	RVtrim(kΩ)	VOUT(V)
LOW	1	38.3	1.3
OPEN	1.2	42.2	1.4
HIGH	0.9	46.4	1.5
10	0.6	51.1	1.6
11	0.65	56.2	1.7
12.1	0.7	61.9	1.8
13.3	0.75	68.1	1.9
14.7	0.8	75	2
16.2	0.85	82.5	2.1
17.8	0.9	90.9	2.2
19.6	0.95	100	2.3
21.5	1	110	2.5
23.7	1.05	121	2.8
26.1	1.1	133	3
28.7	1.15	147	3.3
31.6	1.2	162	4
34.8	1.25	178	5

Table 3 Vout setting

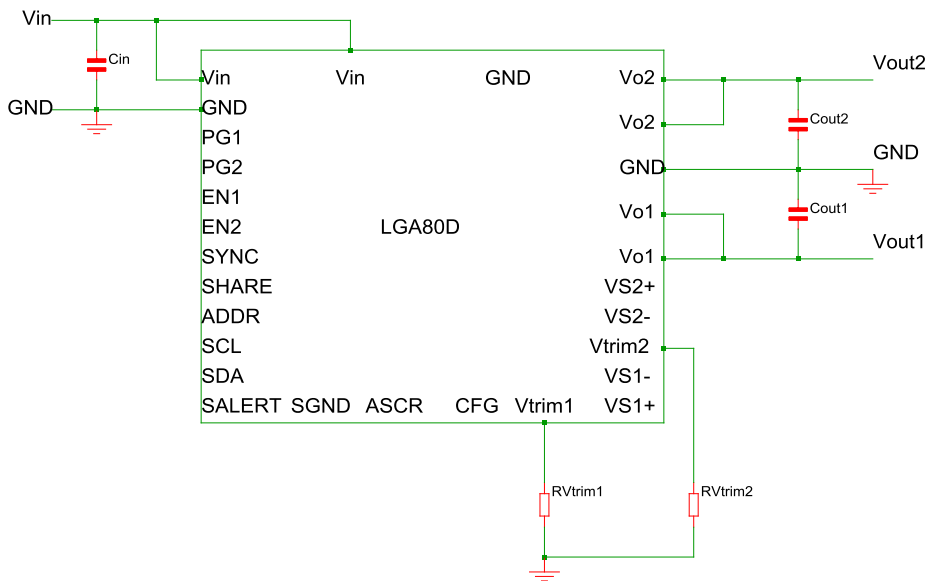


Figure 3 Vout Setting

Features and Functions

Address Setting

When communicating with multiple PMBus modules using the PMBus interface, each module must have its own unique address so the host can distinguish between the modules. The module address can be set according to the external resistor RADDR between pin ADDR and GND that options listed in Table 4. When operating in 2 output mode, care must be taken when using sequential PMBus addresses. Since share addresses are automatically set using the PMBus address, it is possible for a module with a PMBus address immediately after a 2 output LGA80D module to be automatically configured with the same share address as one of the LGA80D channels, which could cause unintended operating modes. When using the LGA80D in a 4-phase application, the master device address must be 1 higher than the slave address. For this reason, do not use the next higher PMBus address when using the LGA80D as a 2 output module.

RADDR (kΩ)	PMBus ADDRESS	RADDR (kΩ)	PMBus ADDRESS
LOW	40h	42.2	51h
OPEN	42h	46.4	52h
10	41h	51.1	53h
11	43h	56.2	54h
12.1	44h	61.9	55h
13.3	45h	68.1	56h
14.7	46h	75	57h
16.2	47h	82.5	58h
17.8	48h	90.9	59h
19.6	49h	100	5Ah
21.5	4Ah	110	5Bh
23.7	4Bh	121	5Ch
26.1	4Ch	133	5Dh
28.7	4Dh	147	5Eh
31.6	4Eh	162	5Fh
34.8	4Fh	178	60h

Table 4 Address Setting

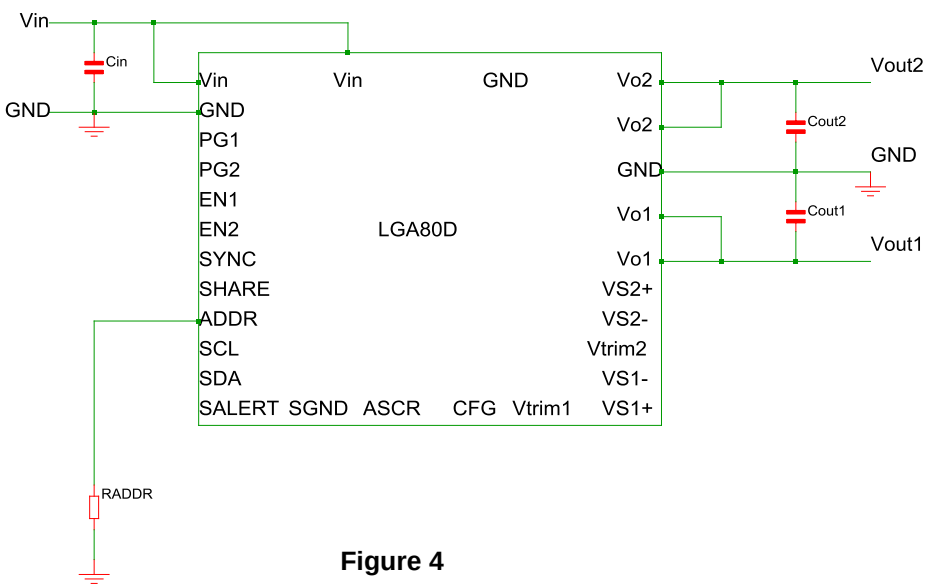


Figure 4

Features and Functions

Switching Frequency Setting (SYNC)

The LGA80D switching frequency can be set from 400kHz to 800kHz by using the external resistor RSYNC between SYNC pin and GND as shown in Table 3. The recommended switching frequency is set at 457kHz with a 23.7KOhm resistor.

RSYNC(kΩ)	FREQ(kHz)	RSYNC(kΩ)	FREQ(kHz)
OPEN	400	28.7	571
HIGH	485	31.6	615
21.5	432	34.8	727
23.7	457	38.3	800
26.1	533		

Table 5 Frequency Setting

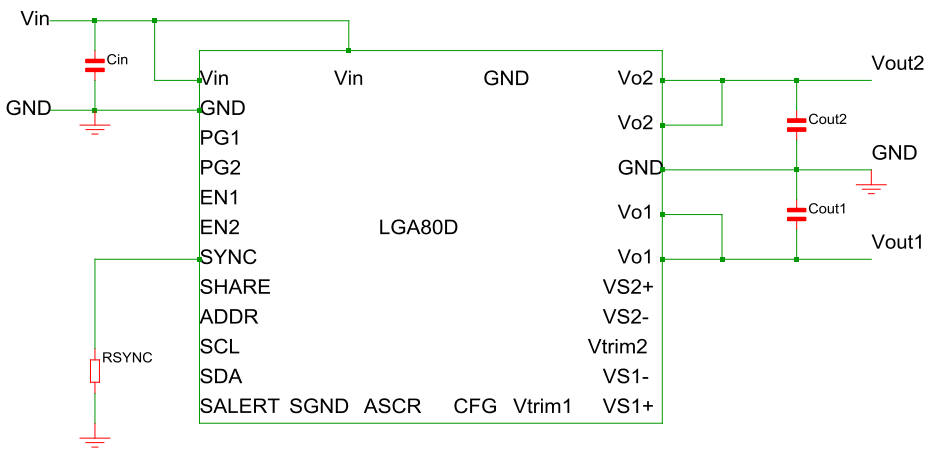


Figure 5

Input Voltage Undervoltage Lock-Out Setting (UVLO)

The input undervoltage lockout (UVLO) prevents the LGA80D from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage undervoltage lock-out threshold can be set between 2.85V and16V using the GUI. The default UVLO value is 6.13V.

Once an input undervoltage fault condition occurs, LGA80D is to shutdown and stay off until the fault has cleared and the module has been disabled and re-enabled.

Configuration Setting (CFG)

The Configuration pin (CFG) sets several module configuration settings by external resistor RCFG between CFG pin and GND that allowing the LGA80D to be used in applications without the need for loading configuration files. The settings are shown in Table 6. When using the LGA80D in a 4 phase application, the master module address must be 1 higher than the slave address. This must be done in order for the 2 modules to be recognized as part of a current sharing group.

RCFG (kΩ)	Vout1 OC LIMIT (A)	Vout2 OC LIMIT (A)	CIRCUIT	RCFG (kΩ)	Vout1 OC LIMIT (A)	Vout2 OC LIMIT (A)	CIRCUIT
10	25	25	2 Output	51.1	45	55	2 Output
11	35	35	2 Output	56.2	25	25	1 output
12.1	45	45	2 Output	61.9	35	35	1 output
13.3	55	55	2 Output	68.1	45	45	1 output
14.7	60	60	2 Output	75	55	55	1 output
16.2	65	65	2 Output	82.5	65	65	1 output
17.8	35	25	2 Output	90.9	35	35	4 phases master
19.6	45	25	2 Output	100	35	35	4 phases slave
21.5	55	25	2 Output	110	45	45	4 phases master
23.7	45	35	2 Output	121	45	45	4 phases slave
26.1	55	35	2 Output	133	55	55	4 phases master
28.7	55	45	2 Output	147	55	55	4 phases slave
31.6	25	35	2 Output	162	65	65	4 phases master
34.8	25	45	2 Output	178	65	65	4 phases slave
38.3	25	55	2 Output	LOW	20	20	1 output
42.2	35	45	2 Output	OPEN	20	20	2 Output
46.4	35	55	2 Output	HIGH	35	35	2 Output

Table 6 Configuration Setting

Each LGA80D module has two phases, the OC limit value in table is for each phase. The OC fault will be triggered if any phase current meet OC limit.

For example: RCFG=56.2kΩ, total OC limit of this LGA80D module is double table's value 2x25=50A, but if one phase meet 25A, OC fault will be triggered.

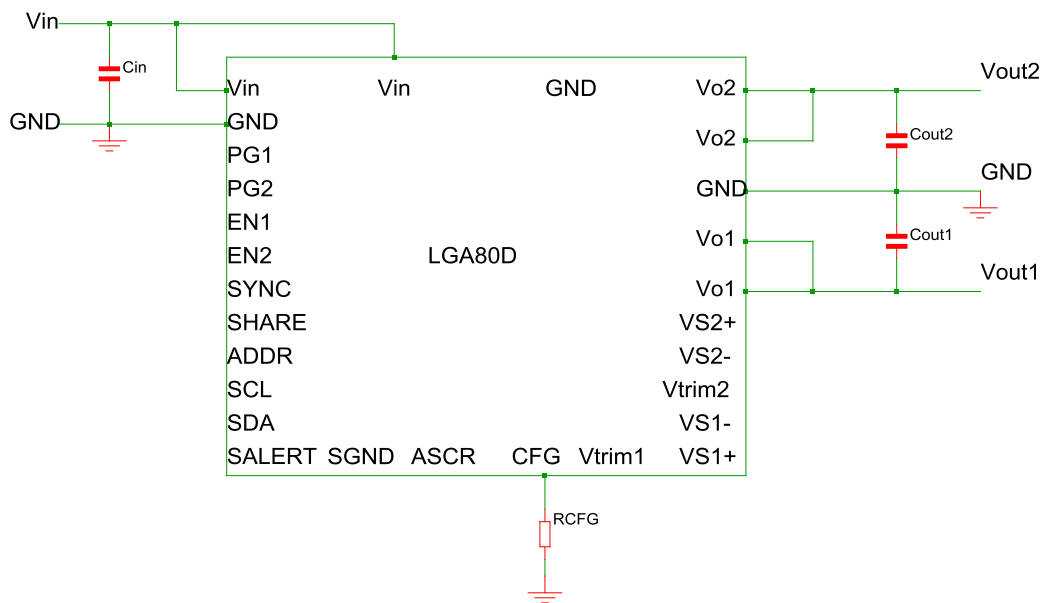


Figure 6

Control Loop(ASCR) Setting

The LGA80D's response can be optimized by adjusting the ASCR Gain and Residual settings by using external resister RASCR between pin ASCR and GND. The resister setting is followed Table 7. The gain value affects dynamic response and gain/phase, the higher gain value, the faster dynamic response and lower gain/phase margin, whereas the opposite. User can select balanced value in the system design, recommended GAIN value is 200~400. The ASCR can also be set via PMBus command ASCR_CONFIG.

RASCR(kΩ)	GAIN Vo1	GAIN Vo2	RASCR(kΩ)	GAIN Vo1	GAIN Vo2
10	200	200	51.1	600	800
11	400	200	56.2	800	800
12.1	600	200	61.9	1000	800
13.3	800	200	68.1	200	1000
14.7	1000	200	75	400	1000
16.2	200	400	82.5	600	1000
17.8	400	400	90.9	800	1000
19.6	600	400	100	1000	1000
21.5	800	400	110	100	100
23.7	1000	400	121	300	300
26.1	200	600	133	500	500
28.7	400	600	147	700	700
31.6	600	600	162	900	900
34.8	800	600	178	1100	1100
38.3	1000	600	LOW	300	300
42.2	200	800	OPEN	500	500
46.4	400	800	HIGH	700	700

Table 7 Response Setting

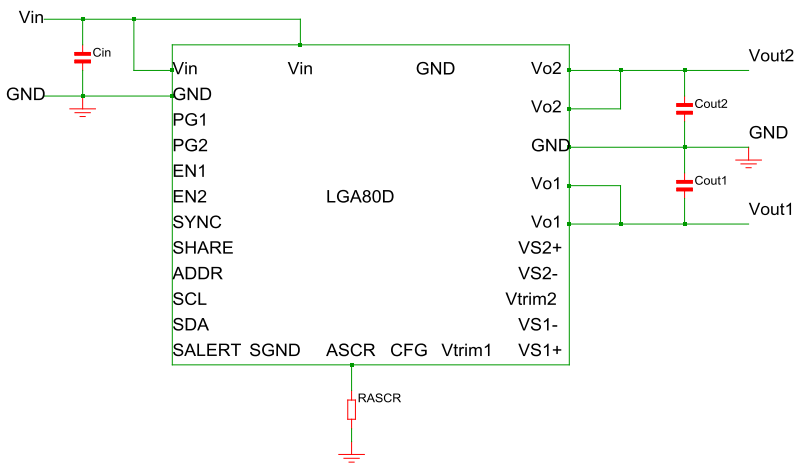


Figure 7

Note: All the High/Low/OPEN in setting table is defined as below.

PIN Connected TO	VALUE
LOW (Logic LOW)	<0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	>2.0 VDC
Resistor to SGND	Set by resistor value

Enable

EN1 and EN2 are used to enable and disable each channel of the LGA80D. When operated as a 2-phase converter, it can either use EN2 with EN1 grounded, or just tie EN1 and EN2 together. However, when operated as 4/6/8 phases configuration, EN1 and EN2 shall be tied together (refer to the block diagram of 4 modules 1 output configuration on page 15). The enable pins shall be held low whenever a configuration file or script is used to configure the LGA80D. LGA80D can be enable/disable by PMBus and GUI also.

Power Good

The LGA80D provides a power good signal(PG0, PG1) for each channel that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the target voltage.

Output Overvoltage Protection

The LGA80D offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VS pin) to a programmable threshold set to 10% higher than the target output voltage (the default setting).

If the VS voltage exceeds this threshold, the PG pin will de-assert and the LGA80D will latch, unit can be restarted if OV fault is removed and reset via toggle the EN(enable).

Output Pre-Bias Start-up

The LGA80D provides pre-biased start-up function in one module one output and one module two outputs operation. Pre-Bias start-up function is not provided when operating in current sharing 2, 3, or 4 LGA80D modules in parallel (4, 6 or 8 phase configurations). An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output.

The LGA80D provides pre-bias start-up function by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the desired output voltage is present after the Ton-delay time the LGA80D starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-up from the pre-bias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command.

The resulting output voltage rise time will vary depending on the pre-bias voltage, but the total time elapsed from the end of the Ton-delay time to when the Ton-rise time is complete and the output is at the desired value will match the pre-configured ramp time. See Figure 4

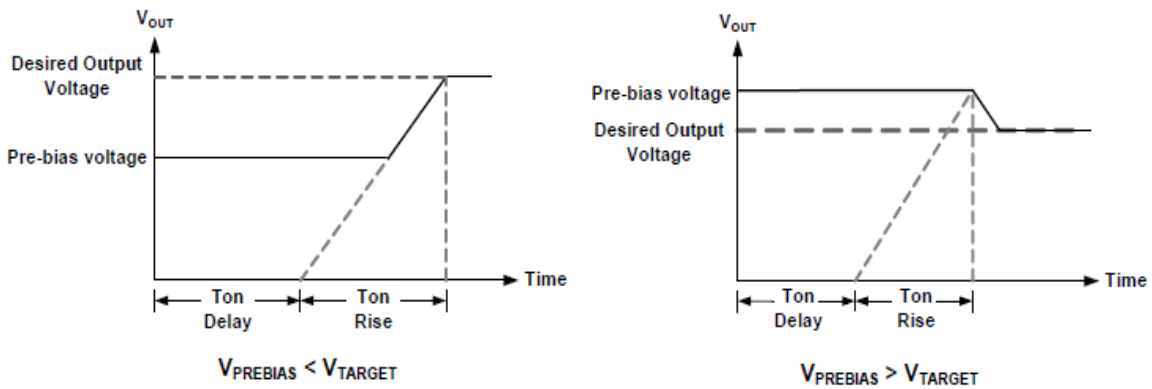


Figure 4

If a pre-bias voltage higher than the target voltage exists after the pre-configured Ton-delay time and Ton-rise time have completed, the LGA80D starts switching with a duty cycle that matches the pre-bias voltage. This ensures that the ramp-down from the pre-bias voltage is monotonic. The output voltage is then ramped down to the desired output voltage

If a pre-bias voltage higher than the overvoltage limit exists, the LGA80D will not initiate a turn-on sequence and will stay off with an output OV fault recorded.

Output Over current Protection
The LGA80D can protect the power supply from damage from an overloaded or shorted output. Once the current trigger OCP set point, the unit will latch, unit can be restarted if OC fault is removed and reset via toggle the EN(enable).

Over Temperature Protection
The LGA80D provide over temperature protection where the hotspot of the LGA80D.
Once the LGA80D has been disabled due to over temperature fault(default value is 120 ºC), the unit will shut down, and will auto-restart when the temperature drop below the OT_WARN_LIMIT value(default is 110 ºC)

Digital Bus(Share Pin of LGA80D)
The Digital-DC Communications via the Share pin bus is used to communicate the LGA80Ds mainly for single output multi-phases configuration.
This dedicated bus provides the communication channel between LGA80Ds for features such as sequencing, fault spreading, and current sharing.
The share pin on all LGA80D modules in a single output configuration shall be connected together.

Fault Spreading
LGA80D can be configured to broadcast a fault event over the share bus to the other LGA80Ds in the group. When a fault occurs and the LGA80D is configured to shut down on a fault, the LGA80D will shut down and broadcast the fault event over the share bus. The other LGA80Ds on the share bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Active Current Sharing
The PWM outputs of the LGA80D are used in parallel to create a dual phase power rail. The LGA80D output will share the current equally within +/-5% at Vo=1.2V.

Stackable

When multiple LGA80D modules shares a common DC input supply, it is desirable to adjust the clock phase offset of each LGA80D such that not all LGA80Ds have coincident rising edges. Setting each LGA80D to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses are reduced.

In order to enable stackable feature, all LGA80D modules must be synchronized to the same switching clock. Configuring the SYNC pin is described in the Configurable Pins Section of this document.

For 2 x LGA80Ds in parallel, set configuration via external resistor refer to configuration setting table.

For 3 or 4 LGA80Ds in parallel, only can be set via GUI or PMBUS on each LGA80D. Each LGA80D will have a different configuration file. It doesn't matter which LGA80D is the "master" and which LGA80D are "slaves". Total four PMBus commands, FREQUENCY_SWITCH, USER_GLOBAL_CONFIG, DDC_CONFIG and DDC_GROUP, shall be used . Please note that DDC_CONFIG and DDC_GROUP must be set on both PAGE 0 and PAGE 1 of each LGA80D's configuration. Below are the example of 4 LGA80Ds(8 phases) single output configuration in parallel via GUI/PMBus.

1. LGA80D Master Setting:

USER_GLOBAL_CONFIG	0x1102	
PAGE	0x00	
DDC_CONFIG	0x0007	# Phase 0
DDC_GROUP	0x00202020	
PAGE	0x01	
DDC_CONFIG	0x8007	# Phase 4
DDC_GROUP	0x00202020	

2. LGA80D Slave1 Setting:

FREQUENCY_SWITCH	0xFB20	# 400 kHz
USER_GLOBAL_CONFIG	0x1104	
PAGE	0x00	
DDC_CONFIG	0x2007	# Phase 1
DDC_GROUP	0x00202020	
PAGE	0x01	
DDC_CONFIG	0xA007	# Phase 5
DDC_GROUP	0x00202020	

3. LGA80D Slave2 Setting:

FREQUENCY_SWITCH	0xFB20	# 400 kHz
USER_GLOBAL_CONFIG	0x1104	
PAGE	0x00	
DDC_CONFIG	0x4007	# Phase 2
DDC_GROUP	0x00202020	
PAGE	0x01	
DDC_CONFIG	0xC007	# Phase 6
DDC_GROUP	0x00202020	

4. LGA80D Slave3 Setting:

FREQUENCY_SWITCH	0xFB20	# 400 kHz
USER_GLOBAL_CONFIG	0x1104	
PAGE	0x00	
DDC_CONFIG	0x6007	# Phase 3
DDC_GROUP	0x00202020	
PAGE	0x01	
DDC_CONFIG	0xE007	# Phase 7
DDC_GROUP	0x00202020	

The addresses are arbitrary, any addresses can be used but all the LGA80D must have a different PMBus address.

For 3 or 4 LGA80Ds in parallel, the following pins shall be connected together:

1. SYNC pins. There must not be a resistor connected from SYNC to ground in the 6 or 8 Phase configuration
2. Share pins.
3. EN (enable) pins.

All the LGA80Ds shall have the same resistor value connected to ASCR, VTRIM0.

3 LGA80D(6 phases) in parallel setting is similar as 4 LGA80Ds'.

Monitoring via PMBus

A system controller can monitor a wide variety of different LGA80D parameters through the PMBus interface. The LGA80D can monitor fault conditions by monitoring the SALRT pin, which will be asserted when any number of pre-configured fault conditions occur.

The LGA80D can also be monitored continuously including the following:

- Input voltage
- Output voltage
- Output current
- Internal controller IC junction temperature
- Internal hottest Mosfet junction temperature
- Fault status information

The PMBus™ Host should respond to SALRT as follows:

1. LGA80D module pulls SALRT Low.
2. PMBus™ Host detects that SALRT is now low, performs transmission with Alert Response Address to find which LGA80D module is pulling SALRT low
3. PMBus™ Host talks to the LGA80D module that has pulled SALRT low.

The actions that the host performs are up to the System Designer.

If multiple LGA80Ds are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to the PMBus™ Commands section of this document for details on how to monitor specific parameters via the PMBus interface.

PMBus Communications

The LGA80D provides a PMBus digital interface. LGA80D can be used with any standard 2-wire PMBus host LGA80D. In addition, LGA80D is compatible with PMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. External Pull-up resistors are required on the PMBus. The pull-up resistor may be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during LGA80D power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any LGA80D to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the LGA80D monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the LGA80D (nominally 4mA). A pull-up resistor of 10kΩ is a good value for most applications.

PMBus Data and Clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V respectively will cause command transmissions to be interrupted and result in slow bus operation or missed commands.

LGA80D accepts most standard PMBus™ commands. When enabling the LGA80D with ON_OFF_CONFIG command, it is recommended that the enable pin is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the PMBus are compliant to the PMBus™ command standards. Any LGA80D module that can be malfunction in a way that permanently shorts PMBus lines will disable PMBus™ communications. Incomplete PMBus™ commands can also cause the LGA80D to halt PMBus™ communications. This can be corrected by disabling, then re-enabling the LGA80D.

PMBUS SUMMARY

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
00h	PAGEf	SelectsController0,1,orboth	R/W	BIT	0h	Page0Controlleraddressed
01h	OPERATION	Enable/disable,marginsettings	R/W	BIT	00h	Immediateoff,nominalmargin
02h	ON_OFF_CONFIG	On/offconfigurationsettings	R/W	BIT	17h	ENABLEpincontrol,activehigh
03h	CLEAR_FAULTS	Clearsfaults	Write	N/A	N/A	N/A
11h	STORE_DEFAULT_ALL	Storesvaluestodefaultstore	Write	N/A	N/A	N/A
12h	RESTORE_DEFAULT_ALL	Restoresvaluesfromdefaultstore	Write	N/A	N/A	N/A
15h	STORE_USER_ALL	Storesvaluestouserstore	Write	N/A	N/A	N/A
16h	RESTORE_USER_ALL	Restoresvaluesfromuserstore	Write	N/A	N/A	N/A
20h	VOUT_MODE	ReportsVOUTmodeandexponent	Read	BIT	13h	LinearMode,Exponent=-13
21h	VOUT_COMMAND	SetsnominalVOUTset-point	R/W	L16u	N/A	PinStrapSetting
23h	VOUT_CAL_OFFSET	AppliesoffsetvoltagetoVOUTset-point	R/W	L16s	0000h	0V
24h	VOUT_MAX	SetsmaximumVOUTset-point	R/W	L16u	N/A	1.15XVOUTpinstrapsetting
25h	VOUT_MARGIN_HIGH	SetsVOUTset-pointduringmarginhigh	R/W	L16u	N/A	1.05xVOUTpinstrapsetting
26h	VOUT_MARGIN_LOW	SetsVOUTset-pointduringmarginlow	R/W	L16u	N/A	0.95xVOUTpinstrapsetting
27h	VOUT_TRANSITION_RATE	Sets VOUT transition rate during margin commands	R/W	L11	BA00h	1V/ms
28h	VOUT_DROOP	Sets V/I slope for total rail output current (all phases combined)	R/W	L11	0000h	0mV/A
33h	FREQUENCY_SWITCH	Setsswitchingfrequency	R/W	L11	N/A	SYNCPinstrapsetting
37h	INTERLEAVE	Configures phase offset during group operation	R/W	BIT	N/A	Set by pin-strapped PMBus™ address
38h	IOUT_CAL_GAIN	Setsimpedanceofcurrentsensecircuit	R/W	L11	B9BCh	0.867mΩ
39h	IOUT_CAL_OFFSET	SetsanoffsettoIOUTsensecircuit	R/W	L11	0000h	0A
40h	VOUT_OV_FAULT_LIMIT	SetstheVOUTovervoltagefaultthreshold	R/W	L16u	N/A	1.1xVOUTpinstrapsetting
41h	VOUT_OV_FAULT_RESPONSE	SetstheVOUTovervoltagefaultresponse	R/W	BIT	80h	Disable,noretry
44h	VOUT_UV_FAULT_LIMIT	Sets the VOUT undervoltage fault threshold	R/W	L16u	N/A	0.85xVOUTpinstrapsetting
45h	VOUT_UV_FAULT_RESPONSE	Sets the VOUT undervoltage fault response	R/W	BIT	80h	Disable, noretry
46h	IOUT_OC_FAULT_LIMIT	Sets the IOUT peak overcurrent fault threshold for each phase	R/W	L11	N/A	CFG pin strap setting
4Bh	IOUT_UC_FAULT_LIMIT	Sets the IOUT valley undercurrent fault threshold for each phase	R/W	L11	N/A	-1*IOUT_OC_FAULT_LIMIT from CFG pin strap setting
4Fh	OT_FAULT_LIMIT	Setstheover-temperaturefaultlimit	R/W	L11	EBC0h	+120°C
50h	OT_FAULT_RESPONSE	Setstheover-temperaturefaultresponse	R/W	BIT	FFh	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature falls below the OT_WARN_LIMIT.
51h	OT_WARN_LIMIT	Setstheover-temperaturewarninglimit	R/W	L11	EB70h	+110°C
52h	UT_WARN_LIMIT	Setstheunder-temperaturewarninglimit	R/W	L11	DC40h	-30°C
53h	UT_FAULT_LIMIT	Setstheunder-temperaturefaultlimit	R/W	L11	E530h	-45°C
54h	UT_FAULT_RESPONSE	Sets the under-temperature fault response	R/W	BIT	BFh	Continuousretry,280msretrydelay
55h	VIN_OV_FAULT_LIMIT	SetstheVINovervoltagefaultthreshold	R/W	L11	D3A0h	14.5V
56h	VIN_OV_FAULT_RESPONSE	SetstheVINovervoltagefaultresponse	R/W	BIT	80h	Disable, noretry
57h	VIN_OV_WARN_LIMIT	Sets the VIN overvoltage warning threshold	R/W	L11	D360h	13.5V
58h	VIN_UV_WARN_LIMIT	Sets the VIN undervoltage warning threshold	R/W	L11	N/A	1.1 x UVLO pin-strap setting
59h	VIN_UV_FAULT_LIMIT	Sets the VIN undervoltage fault threshold	R/W	L11	N/A	UVLO pin-strap setting
5Ah	VIN_UV_FAULT_RESPONSE	Sets the VIN undervoltage fault response	R/W	BIT	BFh	Continuous retries, 280ms retry delay
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication	R/W	L16U	N/A	0.9 x VSET pin-strap setting
60h	TON_DELAY	Sets the delay time from enable to VOUT rise	R/W	L11	CA80h	5ms
61h	TON_RISE	Sets the rise time of VOUT after ENABLE and TON_DELAY	R/W	L11	CA80h	5ms
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of VOUT fall	R/W	L11	CA80h	5ms
65h	TOFF_FALL	Sets the fall time for VOUT after DISABLE and TOFF_DELAY	R/W	L11	CA80h	5ms
78h	STATUS_BYTE	First byte of STATUS_WORD	read	BIT	00h	No faults
79h	STATUS_WORD	Summary of critical faults	read	BIT	00h	No faults
7Ah	STATUS_VOUT	Reports VOUT warnings/faults	read	BIT	00h	No faults

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
7Bh	STATUS_IOUT	Reports IOUT warnings/faults	read	BIT	00h	No faults
7Ch	STATUS_INPUT	Reports input warnings/faults	read	BIT	00h	No faults
7Dh	STATUS_TEMP	Reports input warnings/faults	read	BIT	00h	No faults
7Eh	STATUS_CML	Reports communication, memory, logic errors	read	BIT	00h	No faults
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock synchronization faults	read	BIT	00h	No faults
88h	READ_VIN	Reports input voltage measurement	read	L11	N/A	N/A
89h	READ_IIN	Reports input current measurement	read	L11	N/A	N/A
8Bh	READ_VOUT	Reports output voltage measurement	read	L16U	N/A	N/A
8Ch	READ_IOUT	Reports output current measurement	read	L11	N/A	N/A
8Dh	READ_TEMPERATURE_1	Reports internal temperature measurement	read	L11	N/A	N/A
8Eh	READ_TEMPERATURE_2	Reports external temperature measurement from XTEMP pins	read	L11	N/A	N/A
8Fh	READ_TEMPERATURE_3	Reports external temperature measurement from VMON/TMON pin	read	L11	N/A	N/A
94h	READ_DUTY_CYCLE	Reports actual duty cycle	read	L11	N/A	N/A
95h	READ_FREQUENCY	Reports actual switching frequency	read	L11	N/A	N/A
98h	PMBUS_REVISION	Reports the PMBUS revision used	read	BIT	22h	P1 R1.2, P2 R1.2
99h	MFR_ID	Sets a user defined identification	R/W	ASC	N/A	LGA80D-00DADJJ
9Ah	MFR_MODEL	Sets a user defined model	R/W	ASC	N/A	<null>
9Bh	MFR_REVISION	Sets a user defined revision	R/W	ASC	N/A	001
9Ch	MFR_LOCATION	Sets a user defined location identifier	R/W	ASC	N/A	<null>
9Dh	MFR_DATE	Sets a user defined date	R/W	ASC	N/A	<null>
9Eh	MFR_SERIAL	Sets a user defined serialized identifier	R/W	ASC	N/A	<null>
Adh	IC_DEVICE_ID	Reports device identification information	read	CUS	49A02D00h	
AEh	IC_DEVICE_REV	Reports device revision information	read	CUS	01000000h	
B0h	USER_DATA_00	Sets user defined data	R/W	ASC	N/A	<null>
CEh	MIN_VOUT_REG	Sets a minimum start-up voltage	R/W	L11	0000h	0mV
D0h	ISENSE_CONFIG	Sets the resistance of the input current sensing resistor	R/W	BIT	420Eh	Downslope, 5 fault count, 384ns blanking, high range
D1h	USER_CONFIG	Configures several user-level features	R/W	BIT	N/A	Set by CFG pin-strap setting
D2h	IIN_CAL_GAIN	Sets the resistance of the input current sensing resistor	R/W	L11	C200h	2mΩ
D3h	DDC_CONFIG	Configures the DDC addressing and current sharing	R/W	BIT	N/A	Set by pin-strapped PMBus™ address and CFG pin-strap setting
D4h	POWER_GOOD_DELAY	Sets the delay between PG threshold and PG assertion	R/W	L11	BA00h	
D5h	MULTI_PHASE_RAMP_GAIN	Adjusts the ramp-up and ramp-down rate by setting the feedback gain	R/W	CUS	03h	3
D6h	INDUCTOR	Sets the inductor value	R/W	L11	A23h	0.14µH
D7h	SNAPSHOT_FAULT_MASK	Masks faults that cause a snapshot to be taken	R/W	BIT	00h	No faults masked
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection	R/W	BIT	00h	Low side FET off on fault, 1 violation triggers fault.
D9h	XTEMP_SCALE	Calibrates external temperature sensor	R/W	L11	BA00h	1/degree C
DAh	XTEMP_OFFSET	Offset calibration for external temperature sensor	R/W	L11	00h	No offset
DBh	MFR_SMBALERT_MASK	Identifies which fault limits will not assert SALRT	R/W	Custom	00h	N/A
DCh	TEMPCO_CONFIG	Sets tempco settings	R/W	BIT	00h	0ppm/°C
DDh	PINSTRAP_READ_STATUS	Reads pin-strap settings	Read	BIT	N/A	Set by pin-straps
DFh	ASCR_CONFIG	Configures the ASCR settings	R/W	BIT	N/A	ASCRCFG pin-strap setting
E0h	SEQUENCE	DDC rail sequencing configuration	R/W	BIT	00h	Prequel and sequel disabled
E1h	TRACK_CONFIG	Configures voltage tracking.	R/W	BIT	00h	Tracking disabled
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION and VOUT	R/W	BIT	N/A	Set by CFG pin-strap
E4h	DEVICE_ID	Returns the device identifier string	Read	ASC	TBD	ZL8802, current revisions
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the IOUT overcurrent fault response	R/W	BIT	80h	Disable, no retry
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the IOUT undercurrent fault response	R/W	BIT	80h	Disable, no retry
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the IOUT average overcurrent fault threshold	R/W	L11	N/A	Set by CFG pin-strap

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the IOUT average undercurrent fault threshold	R/W	L11	N/A	-1* IOUT_AVG_OC_FAULT_LIMIT from CFG pin-strap setting
E9h	USER_GLOBAL_CONFIG	Sets options pertaining to advanced features	R/W	BIT	N/A	Set by CFG pin-strap setting
EAh	SNAPSHOT	32-byte read-back of parametric and status values	Read	BIT	N/A	<null>
F0h	LEGACY_FAULT_GROUP	Configures fault group compatibility with older Intersil digital power devices	R/W	BIT	00h	<null>
F3h	SNAPSHOT_CONTROL	Snapshot feature control command	R/W	BIT	00h	N/A
F4h	RESTORE_FACTORY	Restores device to the hard-coded default values	Write	N/A	N/A	N/A
F5h	MFR_VMON_OV_FAULT_LIMIT	Sets the VMON overvoltage fault threshold	R/W	L11	C266h	2.4V, SPS OT trip voltage
F6h	MFR_VMON_UV_FAULT_LIMIT	Sets the VMON undervoltage fault threshold	R/W	L11	B0CCh	0.2V, corresponds to -50°C
F7h	MFR_READ_VMON	Reads the VMON voltage	Read	L11	N/A	N/A
F8h	VMON_OV_FAULT_RESPONSE	Configures the VMON overvoltage fault response	R/W	BIT	BFh	Continuous retry
F9h	VMON_UV_FAULT_RESPONSE	Configures the VMON undervoltage fault response	R/W	BIT	BFh	Continuous retry
FAh	SECURITY_LEVEL	Reports the security level	Read	Hex	01h	Public security level
FBh	PRIVATE_PASSWORD	Sets the private password string	R/W	ASC	00…00h	<null>
FCh	PUBLIC_PASSWORD	Sets the public password string	R/W	ASC	00…00h	<null>
FDh	UNPROTECT	Identifies which commands are protected	R/W	Custom	FF…FFh	No commands are protected

Note: For the PMBUS setting details, please contact Artesyn.

PMBus™ Use Guidelines

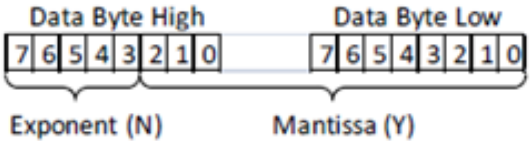
The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring the LGA80D for their application. When configuring the LGA80D, the LGA80D should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW and ASCCR_CONFIG. While the LGA80D is enabled any command can be read. Many commands do not take effect until after the LGA80D has been re-enabled, hence the recommendation that commands that change device settings are written while the LGA80D is disabled.
When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.
In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

SUMMARY:
All commands can be read at any time.
Always disable the LGA80D when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the LGA80D is enabled, for example, VOUT_MARGIN_HIGH.
To be sure a change to LGA80D setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable the LGA80D.

PMBus™ Data Formats

Linear-11 (L11)

L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X).



Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)

L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)

L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X).
Relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)

Breakdown of Bit Field is provided in "PMBus™ Command Detail"

Custom (CUS)

Breakdown of Custom data format is provided in "PMBus™ Command Detail". A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)

A variable length string of text characters uses ASCII data format.

PMBus™ Command Detail

PAGE (00h)

Definition: Selects Controller 0, Controller 1 or both Controllers 0 and 1 to receive commands. All commands following this command will be received and acted on by the selected controller or controllers.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: No

Default Value: 00h (Page 0)

Units: N/A

COMMAND	PAGE (00h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:4	BITS 3:0	PAGE
0000	0000	0
0000	0001	1
1111	1111	Both

OPERATION (01h)

Definition: Sets Enable, Disable and V_{OUT} Margin settings. This command can also be monitored to read the operating state of the device on bits 7:6. Writing Immediate off will turn off the output and ignore TOFF_DELAY and TOFF_FALL settings. This command is not stored like other PMBus commands. The value read reflects the current state of the device. When this command is written the command takes effect, but if a STORE _USER_ALL written and the device is reenabled, the OPERATION settings may not be the same settings that were written before the device was reenabled.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (immediate off)

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:6	BITS 5:4	BITS 3:0 (NOT USED)	UNIT ON OR OFF	MARGIN STATE
00	00	0000	Immediate off (No sequencing)	N/A
01	00	0000	Soft off (With sequencing)	N/A
10	00	0000	On	Nominal
10	01	0000	On	Margin Low
10	10	0000	On	Margin High

NOTE: Bit combinations not listed above may cause command errors.

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN). When bit 0 is set to 1 (turn off the output immediately), the TOFF_FALL setting is ignored.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 17h (ENABLE pin control, active high, turn off output immediately – no ramp down)

Units: N/A

COMMAND	ON_OFF_CONFIG (02h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
7:5	Not Used	000	Not used
4:2	Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin or OPERATION command	000	Not used
		101	Device starts from ENABLE pin only.
		110	Device starts from OPERATION command only.
1	(Polarity of ENABLE pin - not used)	1	Active high only.
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured ramp-down settings ("soft-off")
		1	Turn off the output immediately.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Paged or Global: Global

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Protectable: Yes

Default Value: N/A

Units: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores all current PMBus™ values from the operating memory into the nonvolatile DEFAULT Store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation, the device will be unresponsive for 100ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus™ settings from the nonvolatile DEFAULT store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in USER store. Security level is changed to level 1 following this command. This command should not be used during device operation, the device will be unresponsive for 100ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus™ settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation, the device will be unresponsive for 100ms while storing values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus™ settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command should not be used during device operation, the device will be unresponsive for 100ms while restoring values.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

VOUT_MODE (20H)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 13h (Linear Mode, Exponent = -13)

Units: N/A

COMMAND	VOUT_MODE (20h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1

MODE	BITS 7:5	BITS 4:0 (PARAMETER)
Linear	000	5-bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

VOUT_COMMAND (21h)

Definition: This command sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set to be higher than 115% of the pin-strap VSET setting, or VOUT_MAX if VOUT_MAX is set higher than 115% of the pin-strap VSET setting.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: VSET pin-strap setting

Units: Volts

Equation: V_{OUT} = VOUT_COMMAND × 2^{-13}

Range: 0 to VOUT_MAX

Example: VOUT_COMMAND = 699Ah = 27,034

Target voltage equals 27034 × 2^{-13} = 3.3V

COMMAND	VOUT_COMMAND (21h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	VSET Pin-strap Setting															

VOUT_TRIM (22h)

Definition: The VOUT_TRIM command is used to apply a fixed trim voltage to the output voltage command value. This command is typically used by the manufacturer of a power supply subassembly to calibrate a device in the subassembly circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: Volts

Equation: VOUT trim = VOUT_TRIM × 2^{-13}

Range: ±150mV

COMMAND	VOUT_TRIM (22h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_CAL_OFFSET (23h)

Definition: The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Signed

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: Volts

Equation: V_{OUT} calibration offset = VOUT_CAL_OFFSET$\times 2^{-13}$

Range: ±150mVV

COMMAND	VOUT_CAL_OFFSET (23h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: The VOUT_ MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. If a VOUT_COMMAND is sent with a value higher than VOUT_MAX, the device will set the output voltage to VOUT_MAX. **Note that this command setting does not automatically scale with a stored VOUT_COMMAND setting.**

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear -16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 1.15 x VSET pin-strap setting

Units: Volts

Equation: V_{OUT} max = VOUT_MAX $\times 2^{-13}$

Range: 0V to 5.5V

COMMAND	VOUT_MAX (24h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.15 x VSET Pin-strap Setting															

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin High".

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W word

Protectable: Yes

Default Value: 1.05 x VSET pin-strap setting.

Units: V

Equation: V_{OUT} margin high = VOUT_MARGIN_HIGH x 2^{-13}

Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.05 x VSET Pin-strap Setting															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to "Margin Low".

Paged or Gl

Data Length

Data Format

Type: R/W

Protectable:

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	Not Used	0	Not used
7:4	Number in Group	0 to 15d	Sets the number of devices in the interleave group. A value of 0 is interpreted as 16.
3:0	Position in Group (Interleave Order)	0 to 15d	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 will have a 22.5 degree offset.

Default Value: 0.95 x VSET pin-strap setting.

Units: V

Equation: V_{OUT} margin low = VOUT_MARGIN_LOW

Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_LOW (26h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.95 x VSET Pin-strap Setting															

VOUT_TRANSITION_RATE (27h)

Definition: This command sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible. This commanded rate does not apply when the device is commanded to turn on or to turn off.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0V/ms)

Units: V/ms

Equation: VOUT_TRANSITION_RATE = $Y \times 2^N$

Range: 0.1 to 4V/ms

COMMAND	VOUT_TRANSITION_RATE (27h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

VOUT_DROOP (28h)

Definition: The VOUT_DROOP sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A at which the output voltage decreases with increasing output current for use with passive current sharing schemes. For devices that are set to sink output current (negative output current), the output voltage continues to increase as the output current is negative. VOUT_DROOP is not needed with a single (2-phase) LGA80D. VOUT_DROOP is needed when multiple LGA80Ds are operated in current sharing mode, i.e., 4-, 6- and 8-phase configurations. In this case, VOUT_DROOP is calculated based on the combined output current of all phases as applicable.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: mV/A

Equation: VOUT_DROOP = $Y \times 2^N$

Range: 0 to 40mV/A

COMMAND	VOUT_DROOP (28h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Set by CFG Pin-strap Setting															

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by the equation f_{SW} = 16MHz/n where 12 ≤ n ≤ 80.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC pin-strap setting

Units: kHz

Equation: FREQUENCY_SWITCH = $Y \times 2^N$

Range: 200kHz-1.33MHz

COMMAND	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	SYNC Pin-strapped Value															

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. Interleave is used for setting the phase offset between individual devices, current sharing groups, and/or combinations of devices and current sharing groups. For devices within single current sharing group the phase offset is set automatically. **In a multiphase current share group the same interleave settings must be stored in all devices in the current sharing group in order to phase spread properly.** Interleave Offset refers to the phase offset of Phase 0 of the device; Phase 1 is always Phase 0 + 180 degrees. INTERLEAVE Phase offset is calculated with Equation 6:

Phase Offset (in degrees) = {Rounded(Position • 16/Number)} • 22.5 (EQ. 6)

Phase offsets greater than 360 degrees are "wrapped around" by subtracting 360 degrees.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting.

Units: N/A

COMMAND	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	Set by CFG Pin-strap Setting															

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	Not Used	0	Not used
7:4	Number in Group	0 to 15d	Sets the number of devices in the interleave group. A value of 0 is interpreted as 16.
3:0	Position in Group (Interleave Order)	0 to 15d	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 will have a 22.5 degree offset.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: B2AEh (0.67mΩ)

Units: mΩ

Equation: IOUT_CAL_GAIN = $Y \times 2^N$

COMMAND	IOUT_CAL_GAIN (38h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	1	0	1	0	1	0	1	1	1	0

IOUT_CAL_OFFSET (39h)

Definition: Used to null out any offsets in the output current sensing circuit, and to compensate for delayed measurements of current ramp due to the current sense blanking time (see "ISENSE_CONFIG (D0h)" on page 62).

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BD00h (-1.5A)

Units: A

Equation: IOUT_CAL_OFFSET = $Y \times 2^N$

COMMAND	IOUT_CAL_OFFSET (39h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 1.10 x VSET pin-strap setting.
Units: V
Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT×2^{-13}
Range: 0V to 7.99V

COMMAND	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	1.10 x VSET Pin-strap Setting															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. The retry time is the time between restart attempts.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (shut down immediately, no retries)
Units: Retry time = 35ms increments

COMMAND	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10-11	Disable and retry according to the setting in bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled. VOUT_UV_FAULT_LIMIT should be set to a value below POWER_GOOD

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned.

Type: R/W

Protectable: Yes

Default Value: 0.85 x VSET pin-strap setting.

Units: V

Equation: V_{OUT} UV fault limit = VOUT_UV_FAULT_LIMIT×2^{-13}

Range: 0V to 7.99V

COMMAND	VOUT_UV_FAULT_LIMIT (44h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.85 x VSET Pin-strap Setting															

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response. Note that V_{OUT} UV faults can only occur after Power-good (PG) has been asserted. Under some circumstances this will cause the output to stay fixed below the power-good threshold indefinitely. If this behavior is undesired, use setting 80h. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (shut down immediately, no retries)

Units: Retry time unit = 35ms

COMMAND	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10-11	Disable and Retry according to the setting in bits [5:3].
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired (see "ISENSE_CONFIG (D0h)" on page 62). A fault occurs after this limit is exceeded for the number of consecutive samples as defined in ISENSE_CONFIG. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_AVG_OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_OC_FAULT_LIMIT (46h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	CFG Pin-strap Setting															

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded for the number of consecutive sample as defined in ISENSE_CONFIG. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_AVG_UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -1 * IOUT_OC_FAULT_LIMIT from CFG pin-strap setting

Units: A

Equation: IOUT_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_UC_FAULT_LIMIT (4Bh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-1 * IOUT_OC_FAULT_LIMIT from CFG Pin-strap Setting															

OT_FAULT_LIMIT (4Fh)

Definition: The OT_FAULT_LIMIT command sets the temperature at which the device should indicate an over-temperature fault.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: EBE8h (+125°C)
Units: Celsius
Equation: OT_FAULT_LIMIT = $Y \times 2^N$
Range: 0 to 175°C

COMMAND	OT_FAULT_LIMIT (4Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over-temperature fault. The retry time is the time between restart attempts.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: BFh (Continuous retries, retry delay 280ms)
Units: Retry time unit = 35ms

COMMAND	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature falls below the OT_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature falls below the OT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

OT_WARN_LIMIT (51h)

Definition: The OT_WARN_LIMIT command sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE and notifies the host.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110 °C)

Units: Celsius

Equation: OT_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 175 °C

COMMAND	OT_WARN_LIMIT (51h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

UT_WARN_LIMIT (52h)

Definition: The UT_WARN_LIMIT command set the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE and notifies the host.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30 °C)

Units: Celsius

Equation: UT_WARN_LIMIT = $Y \times 2^N$

Range: -55 °C to +25 °C

COMMAND	UT_WARN_LIMIT (52h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0

UT_FAULT_LIMIT (53h)

Definition: The UT_FAULT_LIMIT command sets the temperature, in degrees Celsius, of the unit at which it should indicate an under-temperature fault.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: E530h (-45°C)

Units: Celsius

Equation: UT_FAULT_LIMIT = $Y \times 2^N$

Range: -55°C to +25°C

COMMAND	UT_FAULT_LIMIT (53h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the table below. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: BFh (Continuous retries, 280ms retry delay)

Units: Retry time unit = 35ms

COMMAND	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the temperature rises above the UT_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the temperature rises above UT_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)* 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D380h (14V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the table below.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Disable, no retry)

Units: N/A

COMMAND	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and Retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when VIN falls below the VIN_OV_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the output falls below the VIN_OV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold as defined by the table below. In response to the OV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D360h (13.5V)

Units: V

Equation: VIN_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_OV_WARN_LIMIT (57h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, Sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 1.10 x UVLO pin-strap setting

Units: V

Equation: VIN_UV_WARN_LIMIT = $Y \times 2^N$

Range: 0 to 19V

COMMAND	VIN_UV_WARN_LIMIT (58h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1.10 x UVLO Pin-strap Setting															

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: UVLO pin-strap setting
Units: V
Equation: VIN_UV_FAULT_LIMIT = $Y \times 2^N$
Range: 0 to 18V

COMMAND	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	UVLO pin-strapped value															

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the VIN undervoltage fault response as defined by the table below. The retry time is the time between restart attempts.
Paged or Global: Global
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: BFh (continuous retries, 280ms retry delay)
Units: Retry time unit = 35ms

COMMAND	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not used
		10	Disable and retry according to the setting in bits [5:3].
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when V_{IN} rises above the VIN_UV_WARN_LIMIT.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after the input voltage rises above the VIN_UV_WARN_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)*35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. POWER_GOOD_ON should be set to a value above VOUT_UV_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-16 Unsigned

Type: R/W

Protectable: Yes

Default Value: 0.9 x VSET pin-strap setting.

Units: V

COMMAND	POWER_GOOD_ON (5Eh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0.9 x VSET Pin-strap Setting															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TON_DELAY = $Y \times 2^N$

Range: 0 to 5 seconds

COMMAND	TON_DELAY (60h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TON_RISE (61h)

Definition: Sets the rise time of VOUT after ENABLE and TON_DELAY for single and dual channel operation. To adjust the rise time in 4-, 6- or 8-phase operation, use MULTI_PHASE_RAMP_GAIN (D5h).

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TON_RISE = $Y \times 2^N$

Range: 0 to 100ms. Although values can be set below 0.50ms, rise time accuracy cannot be guaranteed. In addition, short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

COMMAND	TON_RISE (61h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of VOUT fall.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TON_DELAY = $Y \times 2^N$

Range: 0 to 5 seconds

COMMAND	TOFF_DELAY (64h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY. This setting is only valid in single or 2-phase operation. Setting the TOFF_FALL to values less than 0.5ms will cause the LGA80D to turn-off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time. In 4-, 6- or 8-phase operation, the LGA80D will always turn-off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CA80h (5ms)

Units: ms

Equation: TOFF_FALL = $Y \times 2^N$

Range: 0 to 100ms. Values less than 0.5ms will cause the LGA80D to tri-state the PWM signal (turn-off both the high and low-side FETs) immediately after the expiration of the TOFF_DELAY time.

COMMAND	TOFF_FALL (65h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

STATUS_BYTE (78h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	None of the above	A fault other than the faults listed in bits 7:1 above has occurred. The source of the fault will be in bits 15:8 of the STATUS_WORD

STATUS_WORD (79h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 0000h

Units: N/A

COMMAND	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current fault has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal, if present, is negated. (Note 15)
10	NOT USED	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not used
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	None of the above	A fault other than the faults listed in bits 7:1 above has occurred. The source of the fault will be in bits 15:8 of the STATUS_WORD

NOTE:

15. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

STATUS_VOUT (7Ah)

Definition: The STATUS_VOUT command returns one data byte with the status of the output voltage.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Not used
5	VOUT_UV_WARNING	Not used
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	Not Used	Not used

STATUS_IOUT (7Bh)

Definition: The STATUS_IOUT command returns one data byte with the status of the output current.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	Not Used	Not used
5	Not Used	Not used
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	Not Used	Not used

STATUS_INPUT (7Ch)

Definition: The STATUS_INPUT command returns input voltage and input current status information.
Paged or Global: Global
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read-only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	Not Used	Not used

STATUS_TEMPERATURE (7Dh)

Definition: The STATUS_TEMPERATURE command returns one byte of information with a summary of any temperature related faults or warnings.
Paged or Global: Paged
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read-only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_TEMP (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	Not Used	Not used

STATUS_CML (7Eh)

Definition: The STATUS_WORD command returns one byte of information with a summary of any communications, logic and/or memory errors.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 00h

Units: N/A

COMMAND	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus™ command was received.
6	The PMBus™ command was sent with invalid or unsupported data.
5	A packet error was detected in the PMBus™ command.
4:2	Not used
1	A PMBus™ command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: The STATUS_MFR_SPECIFIC command returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.
Paged or Global: Global
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	MEANING
7	Not Used	Not used
6	DDC Warning	An error was detected on the DDC bus.
5	VMON UV Warning	The voltage on the VMON pin has dropped 10% below the level set by MFR_VMON_UV_FAULT.
4	VMON OV Warning	The voltage on the VMON pin has risen 10% above the level set by MFR_VMON_OV_FAULT.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Not Used	Not used
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by MFR_VMON_UV_FAULT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by MFR_VMON_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: V
Equation: READ_VIN = $Y \times 2^{N}$
Range: N/A

COMMAND	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IIN (89h)

Definition: Returns the input current reading.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IIN = $Y \times 2^{N}$
Range: N/A

COMMAND	READ_IIN (89h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: Read Only
Protectable: No
Default Value: N/A
Equation: READ_VOUT = READ_VOUT × 2^{-13}
Units: V

COMMAND	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IOUT (8Ch)

Definition: Returns the output current reading.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IOUT = $Y \times 2^N$
Range: N/A

COMMAND	READ_IOUT (8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading internal to the device.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: °C
Equation: READ_TEMPERATURE_1 = $Y \times 2^N$
Range: N/A

COMMAND	READ_TEMPERATURE_1 (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_2 (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_2 = $Y \times 2^N$

Range: N/A

COMMAND	READ_TEMPERATURE_2 (8Eh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the VMON/TMON pin when the device is configured to read temperature on the VMON/TMON pin by setting bit 12 in the USER_GLOBAL_CONFIG command to 1. The voltage on the VMON/TMON pin is converted to °C by the equation TEMPERTATURE 3 = (VMON voltage - 0.6V)/0.008. See MFR_VMON commands starting on page 85 (F5h, F6h, F8h, F9H) for fault limits when reading temperature on the VMON/TMON pin.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_3 = $Y \times 2^N$

Range: N/A

COMMAND	READ_TEMPERATURE_3 (8Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.
Paged or Global: Paged
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: %
Equation: READ_DUTY_CYCLE = $Y \times 2^N$
Range: 0 to 100%

COMMAND	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.
Paged or Global: Global
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Default Value: N/A
Units: kHz
Equation: READ_FREQUENCY = $Y \times 2^N$
Range: N/A

COMMAND	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

PMBUS_REVISION (98h)

Definition: The PMBUS_REVISION command returns the revision of the PBus Specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: N/A

Default Value: 22h (Part 1 Revision 1.2, Part 2 Revision 1.2)

Units: N/A

COMMAND	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	See Following Table							
Default Value	0	0	1	0	0	0	1	0

BITS 7:4	PART 1 REVISION	BITS 3:0	PART 2 REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

MFR_ID (99h)

Definition: MFR_ID sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_MODEL (9Ah)

Definition: MFR_MODEL sets a user defined model string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII, ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_REVISION (9Bh)

Definition: MFR_REVISION sets a user defined revision string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_LOCATION (9Ch)

Definition: MFR_LOCATION sets a user defined location identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_DATE (9Dh)

Definition: MFR_DATE sets a user defined date string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MFR_SERIAL (9Eh)

Definition: MFR_SERIAL sets a user defined serialized identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Data Length in Bytes: 4

Data Format: CUS

Type: Block Read

Protectable: No

Default Value:

Units: N/A

COMMAND	IC_DEVICE_ID (ADh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	MFR code	ID High Byte	ID Low Byte	Reserved
Default Value	49h	A0h	2Ah	00h

IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Data Length in Bytes: 4

Data Format: CUS

Type: Block Read

Protectable: No

Default Value: 01000000h (initial release)

Units: N/A

COMMAND	IC_DEVICE_REV (AEh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	Firmware Major	Firmware Minor	Factory Configuration	Reserved
Default Value	01h	00h	00h	00h

USER_DATA_00 (B0h)

Definition: USER_DATA_00 sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Paged or Global: Global

Data Length in Bytes: User defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: Null

Units: N/A

MIN_VOUT_REG (CEh)

Definition: Sets the minimum output voltage in millivolts (mV) that the device will attempt to regulate to during start-up and shutdown ramps.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0mV)

Units: A

Equation: MIN_VOUT_REG = $Y \times 2^N$

COMMAND	MIN_VOUT_REG (CEh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	1	0	0	1	0	0	1	0	1	1	0	0	0

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W word

Protectable: Yes

Default Value: 620Eh (384ns blanking, SPS sensing, high range)

Units: N/A

Range: N/A

COMMAND	ISENSE_CONFIG (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Current Sense Blanking Time	00000	0	Sets the blanking time current sense blanking time in increments of 32ns
		00001	32	
		00010	64	
		00011	96	
		00100	128	
		00101	160	
		00110	192	
		00111	224	
		01000	256	
		01001	288	
		01010	320	
		01011	352	
		01100	384	
		01101	416	
		01110	448	
		01111	480	
		10000	512	
		10001	544	
		10010	576	
		10011	608	
		10100	640	
		10101	672	
		10110	704	
		10111	736	
		11000	768	
		11001	800	
		11010	832	
10:8	Current Sense Fault Count	000	1	Sets the number of consecutive overcurrent (OC) or undercurrent (UC) events required for a fault. An event can occur once during each switching cycle. For example, if 5 is selected, an OC or UC event must occur for 5 consecutive switching cycles, resulting in a delay of at least 5 switching periods.
		001	3	
		010	5	
		011	7	
		100	9	
		101	11	
		110	13	
		111	15	
7:4	Not Used	0000	Not Used	Not used
3:2	Current Sense Control	00	Not Used	Selection of current sensing method (SPS IMON)
		01	DCR (Down Slope)	
		10	DCR (Up Slope)	
		11	SPS	
1:0	Current Sense Range	00	Low Range	Low range ±25mV, medium range ±35mV, high range ±50mV
		01	Medium Range	
		10	High Range	
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command should be saved immediately after being written to the desired user or default store. This is recommended when written as an individual command or as part of a series of commands in a configuration file or script.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	CFG Pin-strap Setting															

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Minimum Duty Cycle	00000	0-31d	Sets the minimum duty-cycle to 2X(VALUE+1)/512. Must be enabled with Bit 7
10	Not Used	1	Not Used	Not used
9:8	Not Used	00	Not Used	Not used
7	Minimum Duty Cycle Control	0	Disable	Control for minimum duty cycle
		1	Enable	
6	Not Used	0	Not Used	Not used
5	VSET Select	0	VSET0	0 = Uses only VSET0 to set the pin-strapped output voltage
		1	VSET1	1 = Uses only VSET1 to set the pin-strapped output voltage
4	Not Used	0	Not Used	Not used
3	PWML disabled state	0	Low when disabled	PWML is low (off) when device is disabled (bit 3 set to 0), or high (on) when device is disabled (bit 3 set to 1)
		1	High when disabled	
2	Power-good Configuration	0	Open Drain	0 = PG is open-drain output
		1	Push-Pull	1 = PG is push-pull output
1	XTEMP Enable	0	Disable	Enable external temperature sensor
		1	Enable	
0	XTEMP Fault Select	0	Disable	Selects external temperature sensor to determine temperature faults
		1	Enable	

IIN_CAL_GAIN (D2h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating input current at +25°C.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: C200h (2mΩ)

Units: mΩ

Equation: IIN_CAL_GAIN = $Y \times 2^N$

COMMAND	IIN_CAL_GAIN (D2h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing for up to 8 phases. To operate as a 2-phase controller, set both phases to the same rail ID, set phases in rail to 2, then set each phase ID **sequentially** as 0 and 1. To operate as a 4-phase controller, set all phases to the same rail ID, set phases in rail to 4, then set each phase ID alternately, for example, the first LGA80D will be set to 0 and 2, the second LGA80D will be set to 1 and 3. The LGA80D will automatically equally offset the phases in the rail. Phase spreading is done automatically as part of the DDC_CONFIG command. **When using CFG pin-strap settings, the DDC_CONFIG command is set automatically.**

NOTE: The output MUST be connected to VSEN0P and VSEN0N when operating as a 2-phase controller.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: PMBus™ address pin-strap dependent.

Units: N/A

COMMAND	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:13	Phase ID	0 to 7	0	Sets the output's phase position within the rail
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (Shared output)
7:3	Not Used	00	00	Not used
2:0	Phases In Rail	0 to 7	0	Identifies the number of phases on the same rail (+1)

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500ms, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h, 1ms

Units: ms

Equation: POWER_GOOD_DELAY = $Y \times 2^N$

Range: 0 to 500ms

COMMAND	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

MULTI_PHASE_RAMP_GAIN (D5h)

Definition: MULTI_PHASE_RAMP_GAIN command value indirectly determines the output voltage rise time during the turn-on ramp. Typical gain values range from 1 to 10. Lower gain values produce longer ramp times.

MULTI_PHASE_RAMP_GAIN mode is automatically selected when the ZLS8802 is configured to operate in a 4-phase current sharing group. When in MULTI_PHASE_RAMP_GAIN mode, the turn-on ramp up is done with the high bandwidth ASCR control circuitry disabled, resulting in a lower loop bandwidth during start-up ramps. Once POWER_GOOD has been asserted, ASCR circuitry is enabled and the LGA80D operates normally. When MULTI_PHASE_RAMP_GAIN mode is enabled, soft-off ramps are not allowed (TOFF_FALL is ignored). When the LGA80D is commanded to shutdown, the PWMHO/1 output is tri-stated, turning both the high-side and low-side MOSFETs off, and the PWMLO/1 pin is pulled low (DrMOS disabled). Large load current transitions during multphase ramp-ups will cause output voltage discontinuities.

When the phase count is 2; i.e., when the LGA80D is operating standalone, ASCR is enabled at all times and all commands associated with turn-on and turn-off (TON_RISE, TOFF_FALL, Soft-Off) operate normally.

Rise time can be calculated using Equation 7:

$$RiseTime = VOUT\_COMMAND / \{14 \bullet Input\ Voltage \bullet FREQUENCY\_SWITCH\ (In\ MHz) \bullet MULTI\_PHASE\_RAMP\_GAIN\} \quad \text{(EQ. 7)}$$

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Custom

Type: R/W

Protectable: Yes

Default Value: 03h

Units: N/A

COMMAND	MULTI_PHASE_RAMP_GAIN (D5h)							
Format	1 Byte Binary							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value	0	0	0	0	0	0	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:0	Gain	00-FF	Start-up ramp gain

INDUCTOR (D6h)

Definition: Informs the device of the circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: B133h (0.3µH)

Units: µH

Equation: INDUCTOR = $Y \times 2^N$

Range: 0 to 100µH

COMMAND	INDUCTOR (D6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1

SNAPSHOT_FAULT_MASK (D7h)

Definition: Prevents faults from causing a SNAPSHOT event (and store) from occurring.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: NA

Range: NA

COMMAND	SNAPSHOT_FAULT_MASK (D7h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
15:14	Not Used	Not used
13	Group	Ignore Fault Spreading faults
12	Phase	Ignore Other Phase faults
11	CPU	Ignore CPU faults
10	CRC	Ignore CRC Memory faults
9	Not Used	Not used
8	Not Used	Not used
7	IOUT_UC_FAULT	Ignore output undercurrent faults
6	IOUT_OC_FAULT	Ignore output overcurrent faults
5	VIN_UV_FAULT	Ignore input undervoltage faults
4	VIN_OV_FAULT	Ignore input undervoltage faults
3	UT_FAULT	Ignore under-temperature faults
2	OT_FAULT	Ignore over-temperature faults
1	VOUT_UV_FAULT	Ignore output undervoltage faults
0	VOUT_OV_FAULT	Ignore output overvoltage faults

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection feature

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	OVUV_CONFIG (D8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
7	Controls how an OV fault response shutdown sets the output driver state	0	An OV fault does not enable low-side power device
		1	An OV fault enables the low-side power device
6:4	Not Used	0	Not used
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response

XTEMP_SCALE (D9h)

Definition: Sets a scalar value that is used for calibrating the external temperature. The constant is applied in the equation below to produce the read value of XTEMP via the PMBus™ command READ_TEMPERATURE_2.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0)

Units: $1/^{\circ}C$

Equation: $\text{READ\_TEMPERATURE\_2} = \left(\text{ExternalTemperature} \cdot \frac{1}{\text{XTEMP\_SCALE}}\right) + \text{XTEMP\_OFFSET}$

Range: 0.1 to 10

COMMAND	XTEMP_SCALE (D9h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

XTEMP_OFFSET (DAh)

Definition: Sets an offset value that is used for calibrating the external temperature. The constant is applied in the equation below to produce the read value of XTEMP via the PMBus™ command READ_TEMPERATURE_2.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0)

Units: °C

Equation: $\text{READ\_TEMPERATURE\_2} = \left(\text{ExternalTemperature} \cdot \frac{1}{\text{XTEMP\_SCALE}}\right) + \text{XTEMP\_OFFSET}$

Range: -100°C to +100°C

COMMAND	XTEMP_OFFSET (DAh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MFR_SMBALERT_MASK (DBh)

Definition: The MFR_SMBALERT_MASK command is used to prevent faults from activating the SALRT pin. The bits in each byte correspond to a specific fault type as defined in the STATUS command.

Data Length in Bytes: 7

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00 00 00 00 00 00 00h (No faults masked)

Units: N/A

COMMAND	MFR_SMBALT_MASK (DBh)							
Format	Bit Field							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See following table							
Bit Position	55	54	53	52	51	50	49	48
Default Value Byte 6	0	0	0	0	0	0	0	0
Bit Position	47	46	45	44	43	42	41	40
Default Value Byte 5	0	0	0	0	0	0	0	0
Bit Position	39	38	37	36	35	34	33	32
Default Value Byte 4	0	0	0	0	0	0	0	0
Bit Position	31	30	29	28	27	26	25	24
Default Value Byte 3	0	0	0	0	0	0	0	0
Bit Position	23	22	21	20	19	18	17	16
Default Value Byte 2	0	0	0	0	0	0	0	0
Bit Position	15	14	13	12	11	10	9	8
Default Value Byte 1	0	0	0	0	0	0	0	0
Bit Position	7	6	5	4	3	2	1	0
Default Value Byte 0	0	0	0	0	0	0	0	0

BYTE	STATUS BYTE NAME	MEANING
6	STATUS_MFR_SPECIFIC	Mask manufacturer specific faults as identified in the STATUS_MFR_SPECIFIC byte.
5	STATUS_OTHER	Not used
4	STATUS_CML	Mask communications, memory or logic specific faults as identified in the STATUS_CML byte.
3	STATUS_TEMPERATURE	Mask temperature specific faults as identified in the STATUS_TEMPERATURE byte
2	STATUS_INPUT	Mask input specific faults as identified in the STATUS_INPUT byte
1	STATUS_IOUT	Mask output current specific faults as identified in the STATUS_IOUT byte
0	STATUS_VOUT	Mask output voltage specific faults as identified in the STATUS_VOUT byte

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values are applied as negative correction to a positive temperature coefficient. TEMPCO_CONFIG should be set to 3900ppm (27h) when using inductor DCR current sensing in order to compensate for the variation in inductor resistance due to the temperature coefficient of copper. When using the ISL9922X Smart Power Stage, TEMPCO_CONFIG should be set to 0ppm (00h) since the IMON signal from the ISL9922X is internally compensated for temperature.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (0ppm/°C, copper)

Equation: To determine the hex value of the Tempco Correction factor (TC) for current scale of a power stage current sensing, first determine the temperature coefficient of resistance for the sensing element, α. This is found with Equation 8:

$$\alpha = \frac{R_{REF} - R}{R_{REF}(T_{REF} - T)} \qquad \text{(EQ. 8)}$$

Where:

R = Sensing element resistance at temperature "T"

R_{REF} = Sensing element resistance at reference temperature T_{REF}

α = Temperature coefficient of resistance for the sensing element material

T = Temperature measured by temperature sensor, in degrees Celsius

T_{REF} = Reference temperature that α is specified at for the sensing element material

After α is determined, convert the value in units of 100ppm/°C. This value is then converted to a hex value with Equation 9:

$$TC = \frac{\alpha \times 10^6}{100} \qquad \text{(EQ. 9)}$$

Range: 0 to 12700ppm/°C

COMMAND	TEMPCO_CONFIG (DCh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
7	Selects the temp sensor source for tempco correction	0	Selects the internal temperature sensor
		1	Selects the XTEMP pin for temperature measurements (2N3904 Junction) Note that XTEMP must be enabled in USER_CONFIG, bit 1.
6:0	Sets the tempco correction in units of 100ppm/°C for IOUT_CAL_GAIN	TC	RSEN (DCR) = IOUT_CAL_GAIN x (1+TC x (T-25)) Where RSEN = resistance of sense element

PINSTRAP_READ_STATUS (DDh)

Definition: Reads back 7 bytes of 8 bit values that represent the pin-strap settings of each of the device's pin-strap pins. This value corresponds to a resistor value, a high, a low or an open condition. The pin decode values correspond to pin-strap settings according to Table 9:

TABLE 9.

R (kΩ)	DECODE	R (kΩ)	DECODE
10	00	51.1	11
11	01	56.2	12
12.1	02	61.9	13
13.3	03	68.1	14
14.7	04	75	15
16.2	05	82.5	16
17.8	06	90.9	17
19.6	07	100	18
21.5	08	110	19
23.7	09	121	1A
26.1	0A	133	1B
28.7	0B	147	1C
31.6	0C	162	1D
34.8	0D	178	1E
38.3	0E	LOW	F1
42.2	0F	OPEN	F2
46.4	10	HIGH	F3
Unmeasured			F4

Paged or Global: Global
Data Length in Bytes: 7
Data Format: Bit Field
Type: Read Only
Protectable: Yes
Default Value: Pin-strap settings
Units: N/A

COMMAND	READ_PINSTRAP (DDh)															
Format	Bit Field															
Bit Position									55	54	53	52	51	50	49	48
Access									R	R	R	R	R	R	R	R
Function									ASCRCFG Pin Decode							
Default Value									ASCRCFG Pin-strap Setting							
Format	Bit Field															
Bit Position	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	CFG Pin Decode								SYNC Pin Decode							
Default Value	CFG Pin-strap Setting								SYNC Pin-strap Setting							
Format	Bit Field															

COMMAND	READ_PINSTRAP (DDh) (Continued)															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	UVLO Pin Decode								VSET0 Pin Decode							
Default Value	UVLO Pin-strap Setting								VSET0 Pin-strap Setting							
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	VSET1 Pin Decode								Reserved							
Default Value	VSET1 Pin-strap Setting								N/A							

BITS	PURPOSE	VALUE	DESCRIPTION
55:48	ASCRCFG Pin Decode	00-F4h	Decode value of ASCRCFG pin-strap setting
47:40	CFG Pin Decode	00-F4h	Decode value of CFG pin-strap setting
39:32	SYNC Pin Decode	00-F4h	Decode value of SYNC pin-strap setting
31:24	UVLO Pin Decode	00-F4h	Decode value of UVLO pin-strap setting
23:16	VSET0 Pin Decode	00-F4h	Decode value of VSET0 pin-strap setting
15:8	VSET1 Pin Decode	00-F4h	Decode value of VSET1 pin-strap setting
7:0	Not Used	FF	Not used

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain and residual value are automatically set by the LGA80D based on input voltage and output voltage. ASCR gain is analogous to bandwidth, ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but will not affect the peak output voltage deviation. Typical ASCR gain settings range from 100 to 1000, and ASCR residual settings range from 10 to 90.

Paged or Global: Paged

Data Length in Bytes: 4

Data Format: Bit Field and nonsigned binary

Type: R/W

Protectable: Yes

Default Value: ASCRCFG pin-strap setting

Units: N/A

COMMAND	ASCR_CONFIG (DFh)															
Format	Bit Field/Linear-8 Unsigned															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	1	ASCRCFG Pin-strap Setting (residual)							
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	ASCRCFG Pin-strap Setting (gain)															

BITS	PURPOSE	VALUE	DESCRIPTION
31:25	Not Used	0000000h	Not used
24	ASCR Enable	1	Enable
		0	Disable
23:16	ASCR Residual Setting	0 - 7Fh	ASCR residual
15:0	ASCR Gain Setting	0-FFh	ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multirail sequencing. The device will enable its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus as a result of the prequel's Power-good (PG) signal going high. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus at the completion of its ramp-down (its output voltage is 0V).

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h (prequel and sequel disabled)

Units: N/A

COMMAND	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail
		1	Enable	Enable, prequel to this rail is defined by bits 12:8
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail
7	Sequel Enable	0	Disable	Disable, no sequel following this rail
		1	Enable	Enable, sequel to this rail is defined by bits 4:0
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device. Single device (Channel 0, Channel 1 or 2-phase) tracking is supported. Tracking as part of a 4-, 6- or 8-phase current sharing group is not supported. When tracking, the TOFF_DELAY in the tracking device must be greater than TOFF_DELAY + TOFF_FALL in the device being tracked. When configured to track, VOUT_COMMAND must be set to the desired steady state output voltage.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	TRACK_CONFIG (E1h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	Voltage Tracking Control	0	Disable	Tracking is Disabled.
		1	Enable	Tracking is Enabled.
6:3	Not Used	0000	Not Used	Not used
2	Tracking Ratio Control	0	100%	Output Tracks at 100% ratio of VTRK input.
		1	50%	Output Tracks at 50% ratio of VTRK input.
1	Tracking Upper Limit	0	Target Voltage	Output Voltage is Limited by Target Voltage.
		1	VTRK Voltage	Output Voltage is Limited by VTRK Voltage.
0	Not Used	0	Not Used	Not used

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned Group numbers in order to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Rail IDs (see "DDC_CONFIG (D3h)" on page 65). Current sharing rails need to be in the same DDC Group in order to respond to broadcast VOUT_COMMAND and OPERATION commands. Power fail event responses (and phases) are automatically spread in Phase 0 and 1 when the LGA80D is operating in 2-phase current sharing mode when it is configured using DDC_CONFIG, regardless of its setting in DDC_GROUP.

Paged or Global: Paged

Data Length in Bytes: 34

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	DDC_GROUP (E2h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used										EN>	VOUT_COMMAND Group ID				
Default Value	Set by CFG Pin-strap Setting															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Not Used		EN>	OPERATION Group ID					Not Used		EN>	Power Fail Group ID				
Default Value	Set by CFG Pin-strap Setting															

BITS	PURPOSE	VALUE	DESCRIPTION
31:22	Not Used	00	Not used
21	BROADCAST_VOUT_COMMAND response	1	Responds to broadcast VOUT_COMMAND with same Group ID
		0	Ignores broadcast VOUT_COMMAND
20:16	BROADCAST_VOUT_COMMAND group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events
15:14	Not Used	00	Not used
13	BROADCAST_OPERATION response	1	Responds to broadcast OPERATION with same Group ID
		0	Ignores broadcast OPERATION
12:8	BROADCAST_OPERATION group ID	0-31d	Group ID sent as data for broadcast OPERATION events
7:6	Not Used	00	Not used
5	POWER_FAIL response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string. The format is: Part number, Major Revision, (period), Minor Revision, Engineering version letter

Paged or Global: Global

Data Length in Bytes: 16

Data Format: ASCII. ISO/IEC 8859-1

Type: Block Read

Protectable: Read Only

Default Value:

Units: N/A

COMMAND	DEVICE_ID (E4h)															
Format	Characters (Bytes)															
Characters	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Part Number										Maj. Rev.		.	Min. Rev		Engr.
Default Value	Z	L	8	8	0	0					*	*	*	*	*	*
* Current revision at time of manufacture																

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (immediate shutdown, no retries)

Units: Retry time unit = 35ms

COMMAND	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1)* 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT. The retry time is the time between restart attempts.

Data Length in Bytes: 1

Paged or Global: Paged

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: 80h (Immediate shutdown, no retries)

Units: Retry time unit = 35ms

COMMAND	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, for all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when the fault is no longer present.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1) *35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: CFG pin-strap setting

Units: Amperes

Equation: IOUT_AVG_OC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	CFG Pin-strap Setting															

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: -1 X IOUT_AVG_OC_FAULT_LIMIT as set by CFG pin-strap setting

Units: Amperes

Equation: IOUT_AVG_UC_FAULT_LIMIT = $Y \times 2^N$

Range: -100A to 100A

COMMAND	IOUT_AVG_UC_FAULT_LIMIT (E8h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	-1 X IOUT_AVG_OC_FAULT_LIMIT as set by CFG Pin-strap Setting															

USER_GLOBAL_CONFIG (E9h)

Definition: This command is used to set options for output voltage sensing, VMON/TMON pin configuration, SMBus time-out and DDC and SYNC output configurations.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: Set by CFG pin-strap setting

Units: N/A

COMMAND	USER_GLOBAL_CONFIG (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	Set by CFG Pin-strap Setting															

BITS	PURPOSE	VALUE	DESCRIPTION
15:13	Not Used	000000	Not used
12	VMON/TMON Config	0	MFR_READ_VMON returns voltage on VMON pin in Volts. External 16:1 voltage divider needed on VMON/TMON pin (pin 6) to voltage being monitored.
		1	READ_TEMPERATURE_3 returns TMON in °C. External 2:1 voltage divider needed on VMON/TMON pin (pin 6) to SPS TMON pin.
11:10	Not Used	00	Not used
9:8	VSENSE Select for monitoring and fault detection	00	Output 0 uses VSEN0, Output 1 uses VSEN1
		01	Both outputs use VSEN0
		10-11	Not used
7	Not Used	0	Not used
6	DDC output Configuration	0	DDC output open drain
		1	DDC output push-pull
5	Not Used	0	Not used
4	Disable SMBus Time-Outs	0	SMBus time-outs enabled
		1	SMBus time-outs disabled
3	Not Used	0	Not used
2:1	Sync I/O Control	00	Use internal clock (frequency initially set with pin-strap)
		01	Use internal clock and output internal clock (not for use with pin-strap)
		10	Use external clock
		11	Not used
0	Not Used	0	Not used

SNAPSHOT (EAh)

Definition: The SNAPSHOT command is a 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or via a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command. When a fault occurs, the latest snapshot in RAM is stored to flash. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT.

Paged or Global: Paged

Data Length in Bytes: 32

Data Format: Bit Field

Type: Block Read

Protectable: No

Default Value: N/A

Units: N/A

BYTE NUMBER	VALUE	PMBus™ COMMAND	FORMAT
31:23	Not Used	Not Used	0000h
22	Flash Memory Status Byte	N/A	Bit Field
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
13:12	External Temperature	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
11:10	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
7:6	Highest Measured Output Current	N/A	2 Byte Linear-11
5:4	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
3:2	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
1:0	Input Voltage	READ_VIN (88h)	2 Byte Linear-11

LEGACY_FAULT_GROUP (F0h)

Definition: This command allows the LGA80D to sequence and fault spread with devices other than the ZL8800 family of ICs. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

NOTE: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail must shut down for the rail to report a shutdown.

If fault spread mode is enabled in USER_CONFIG, the device will immediately shut down if on of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults.

If fault spread mode is disabled in USER_CONFIG, the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Paged or Global: Paged
Data Length in Bytes: 4
Data Format: Bit field
Type: Block R/W
Protectable: Yes
Default Value: 00000000h
Units: N/A

COMMAND	LEGACY_FAULT_GROUP (F0h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
31:0	Fault Group	NA	00000000h	Identifies the devices in the fault spreading group.

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current SNAPSHOT values from NVRAM to the 32-byte SNAPSHOT command parameter. Writing a 02h will cause the device to write the current SNAPSHOT values to NVRAM, 03h will erase all SNAPSHOT values from NVRAM. Write (02h) and Erase (03h) may only be used when the device is disabled. All other values will be ignored. SNAPSHOT 03h must be written to the device when the device is DISABLED. Data will not be updated, or written to NVRAM after a fault occurs until the SNAPSHOT 03h command has been written.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W Byte

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	SNAPSHOT_CONTROL (F3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

VALUE	DESCRIPTION
01	Read SNAPSHOT values from NVRAM
02	Write SNAPSHOT values to NVRAM
03	Erase SNAPSHOT values from NVRAM

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write Only

Protectable: Yes

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Sets the VMON over-temperature fault threshold. The VMON overvoltage warn limit is automatically set to 90% of this fault value. If VMON is not used, set VMON_OV_FAULT_RESPONSE to 00h, which will disable VMON OV faults entirely.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: C266h (2.4V)

Units: Volts

Equation: MFR_VMON_OV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 20V

COMMAND	MFR_VMON_OV_FAULT_LIMIT (F5h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Sets the VMON undervoltage fault threshold. The VMON undervoltage warn limit is automatically set to 110% of this fault value. If VMON is not used, set VMON_UV_FAULT_RESPONSE to 00h, which will disable VMON UV faults entirely.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: B0CCh (0.2V)

Units: Volts

Equation: MFR_VMON_UV_FAULT_LIMIT = $Y \times 2^N$

Range: 0 to 20V

COMMAND	MFR_VMON_UV_FAULT_LIMIT (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0

MFR_READ_VMON (F7h)

Definition: Reads the voltage on the VMON pin.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Linear-11

Type: Read Only

Protectable: No

Default Value: N/A

Units: °C

Equation: MFR_READ_VMON = Y x 2^N

Range: -200 °C to +200 °C

COMMAND	MFR_READ_VMON (F7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Configures the VMON overvoltage fault response as defined by the table below. Note: The retry time is the time between restart attempts. If VMON is not used, set this response to 00h, which will disable VMON OV faults entirely

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Protectable: Yes

Default Value: BFh (continuous retries)

Units: N/A

COMMAND	VMON_OV_FAULT_RESPONSE (F8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Ignore faults
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when VMON falls below 95% of the VMON_OV_FAULT_LIMIT setting.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after VMON falls below 95% of the VMON_OV_FAULT_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1) * 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Configures the VMON undervoltage fault response as defined by the table below. Note: The retry time is the time between restart attempts. If VMON is not used, set this response to 00h, which will disable VMON UV faults entirely

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field.

Type: R/W

Protectable: Yes

Default Value: BFh (continuous retries)

Units: Retry time unit = 35ms

COMMAND	VMON_UV_FAULT_RESPONSE (F9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	See Following Table							
Default Value	1	0	1	1	1	1	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response behavior, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Fault ignored
		01	Not used
		10	Disable without delay and retry according to the setting in bits 5:3.
		11	Output is disabled while the fault is present. Operation resumes and the output is enabled when VMON rises above 105% of the VMON_UV_FAULT_LIMIT setting.
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without checking if the fault is still present, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. A retry is attempted after VMON has risen above 105% of VMON_UV_FAULT_LIMIT. The time between the start of each attempt to restart is set by the value in bits [2:0] multiplied by 35ms.
2:0	Retry Delay	000-111	Retry delay time = (Value +1) * 35ms. Sets the time between retries in 35ms increments. Range is 35ms to 280ms.

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writeable (commands are always readable). If a command is not writeable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as nonwriteable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as nonwriteable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT store must be sent in order to change that command. If a command is writeable according to the default UNPROTECT parameter, it may still be marked as nonwriteable in the user store UNPROTECT parameter. In this case, the user private password can be sent to make the command writeable.

The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed below. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1.

Figure 12 on page 88 shows the algorithm used by the device to determine if a particular command write is allowed.

Paged or Global: Global

Data Length in Bytes: 1

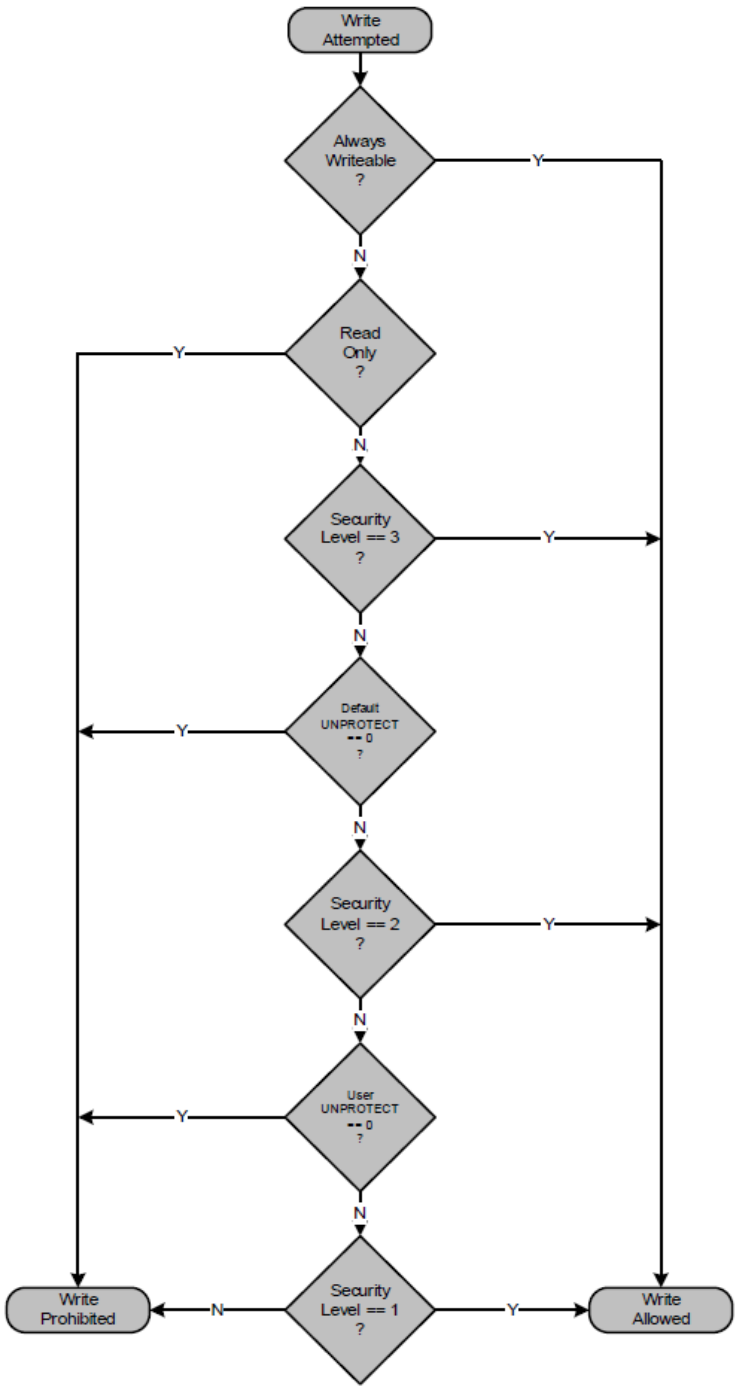
Data Format: Hex

Type: Read Byte

Protectable: No

Default Value: 01h

Units: N/A



ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITEABLE

Security Level 3 – Module Vendor

Level 3 is intended primarily for use by module vendors to protect device configurations in the default store. Clearing a UNPROTECT bit in the default store implies that a command is writeable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the default store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 – User

Level 2 is intended for use by the end user of the device. Clearing a UNPROTECT bit in the user store implies that a command is writeable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 – Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the default and User Store. Security is raised to Level 1 by writing the public password stored in the user store using the PUBLIC_PASSWORD command. The public password stored in the default store has no effect.

Security Level 0 - Unprotected

Level 0 implies that only commands which are always writeable (e.g., PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value which does not match the stored public password.

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.
Paged or Global: Global
Data Length in Bytes: 9
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: No
Default Value: 000000000000000000h
Units: N/A

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.
Paged or Global: Global
Data Length in Bytes: 4
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: No
Default Value: 00000000h
Units: N/A

UNPROTECT (FDh)

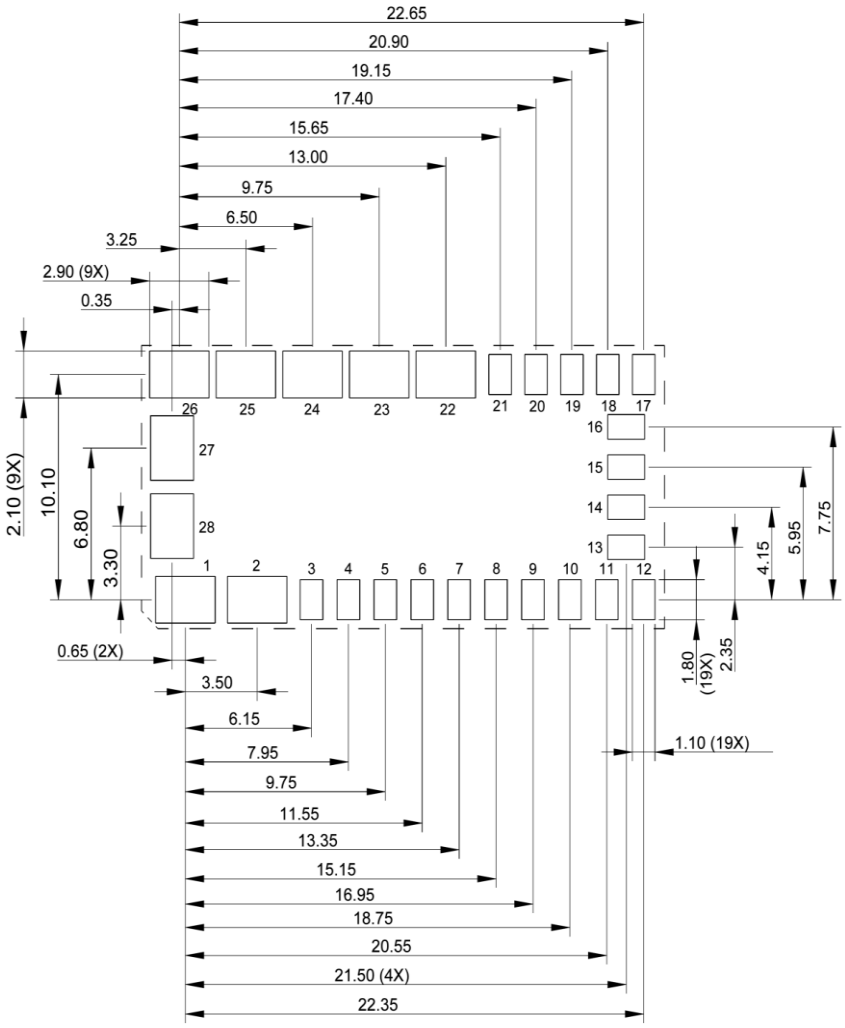
Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protectable or supported by the device. Clearing a command's UNPROTECT bit indicates that write-access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the default store require a security level 3 or greater to be writeable. The UNPROTECT bits in the user store require a security level of 2 or higher.
Data Length in Bytes: 32
Paged or Global: Global
Data Format: Custom
Type: Block R/W
Protectable: No
Default Value: FF...FFh
Units: N/A

LGA80D™ GUI

LGA80D GUI setting refer to separate document “LGA80D™ GUI User’s Manual”.

Mechanical Drawings

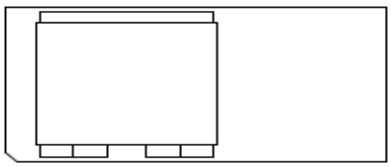
PIN#	Function
1	Vin
2	GND
3	PG1
4	PG2
5	EN1
6	EN2
7	SYNC
8	SHARE
9	ADDR
10	SCL
11	SDA
12	SALERT
13	SGND
14	ASCRCFG
15	CFG
16	Vtrim1
17	VS1+
18	VS1-
19	Vtrim2
20	VS2-
21	VS2+
22	Vo1
23	Vo1
24	GND
25	Vo2
26	Vo2
27	GND
28	Vin



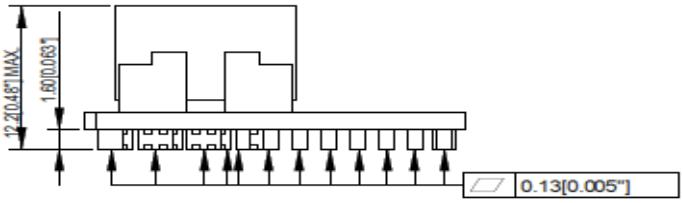
RECOMMENDED PAD LAYOUT

NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCE: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

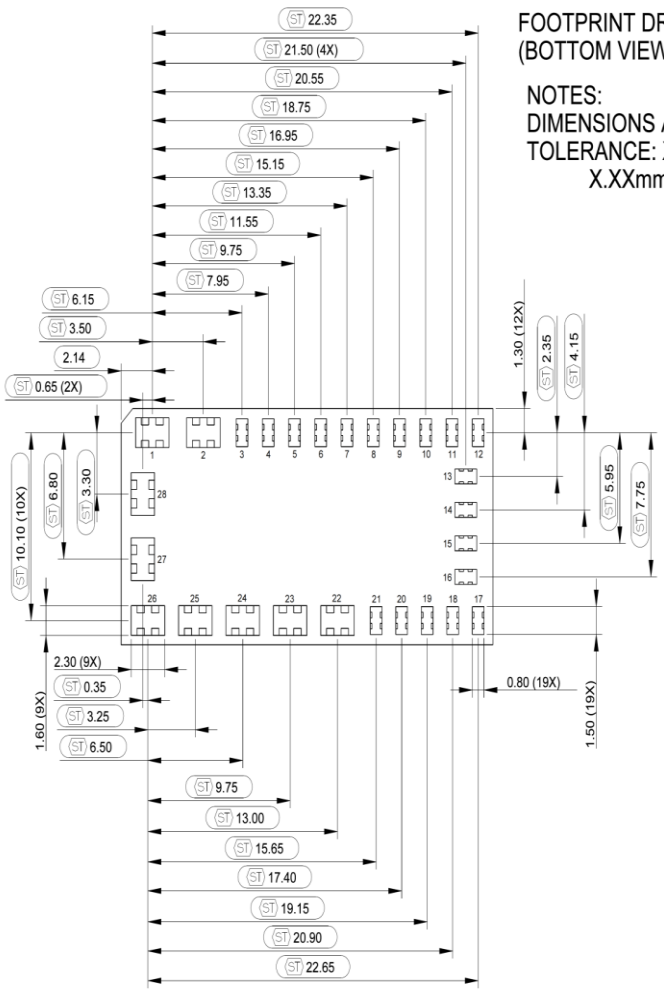
Mechanical Drawings



TOP VIEW



SIDE VIEW



FOOTPRINT DRAWING OF METAL PINS
(BOTTOM VIEW)

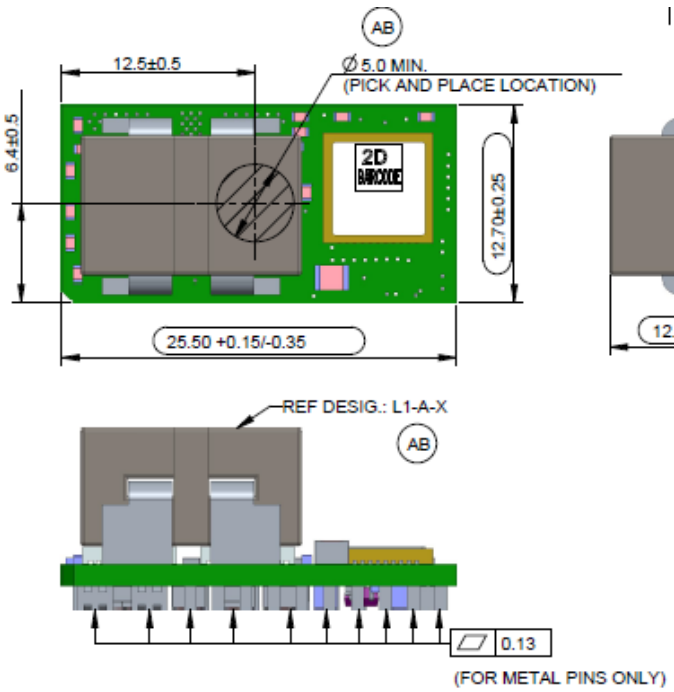
NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCE: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

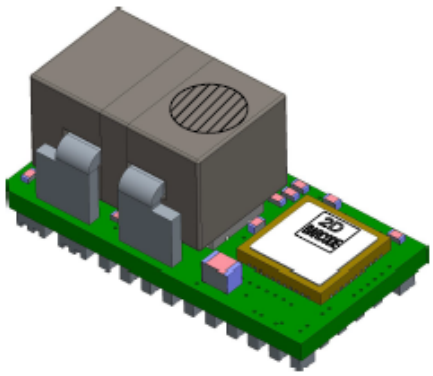
Surface Mount Information

Pick and Place

The LGA80D is designed with certain features to ensure it is compatible with standard pick and place equipment.

• The low mass of typically 9 grams is within the capability of standard pick and place equipment. The choice of nozzle size and style and placement speed may need to be optimized
• The inductor has a flat area of 133.2mm2 (0.206in2) that can be used as a pick-up area.





PC Board Assembly Side

LGA80D module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Reflow Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free reflow soldering process

Pb-free Reflow Profile

This module will comply with IPC/JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. The Standard provides reflow profile based on the volume and thickness of the module. The suggested Pb-free solder paste is Sn/Ag/Cu (SAC305). The recommended reflow temperature profile using SAC305 solder is shown below.

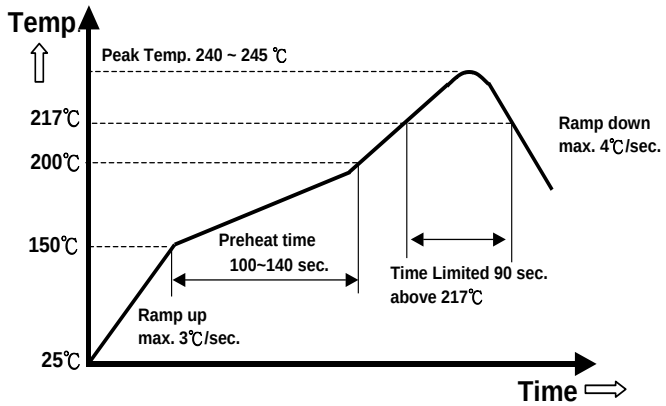


Figure Recommended reflow profile using SAC305 solder paste

Tin-Pb Reflow Profile

The power modules are lead free modules and can be soldered either in a lead-free solder process or in a conventional Tin/Lead (Sn/Pb) process. It is recommended that the customer review datasheets in order to customize the solder reflow profile for each load board assembly. The following instructions must be observed when soldering these units. Failure to observe there instructions may result in the failure of or cause damage to the modules, and can adversely affect long-term reliability.

In a conventional Tin/Lead (Sn/Pb) solder process, peak reflow temperatures are limited to less than 235ºC. Typically, the eutectic solder melts at 183ºC, wets the land, and subsequently wicks the device connection. Sufficient time must be allowed to fuse the plating on the connection ensure a reliable solder joint. There are several types of SMTreflow technologies currently used in the industry. These surface mount power modules can be reliably soldered using natural forced convection, IR (radiant infrared), or a combination of convection/IR. For reliable soldering the solder reflow profile should be established by accurately measuring the modules block pin temperatures.

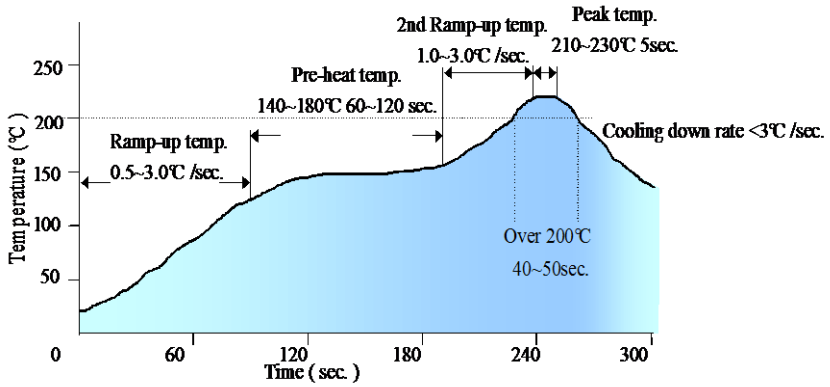


Figure Recommended reflow profile

Note: 1. The stencil thickness for soldering module to load board is recommended as 5mil.
2. Recommended soldering Nitrogen process.

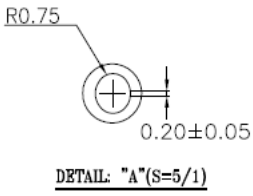
Surface Mount Information

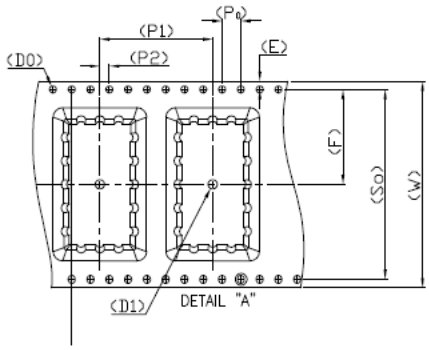
- **Moisture Sensitivity Level (MSL)**
- This module is classified as MSL level 3

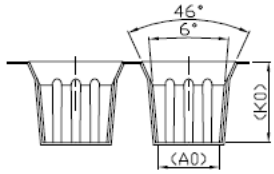
- **Storage and Handling**
- The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of <= 30ºC and 60% relative humidity varies according to the MSL rating (See J-STD-033). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: <40ºC, <90% relative humidity.

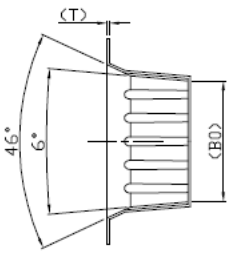
- **Post Soldering Cleaning**
- Post solder cleaning is not recommended because it may affect the reliability of module

Tape and Reel









EIA DIMENSIONS	
W	44.00±0.30
E	1.75±0.10
F	20.20±0.15
P_1	24.00±0.10
P_0	4.00±0.10
P_2	2.00±0.10
D_0	ø1.50 $^{+0.10}_{-0.00}$
D_1	ø2.00Min
T	0.50±0.05
S_0	40.40±0.10
A_0	13.10±0.10
B_0	25.80±0.10
K_0	12.40±0.10

Record of Revision and Changes

ISSUE	DATE	DESCRIPTION	ORIGINATORS
1	6/1/2016	First Release	Shuang Qiu / MH.Chiang
2	6/22/2016	Updated to reflect -40degC operation, Included Enable connection into block diagrams and modified enable connection instructions.	MH Chiang, Shuang Qiu, A Brown