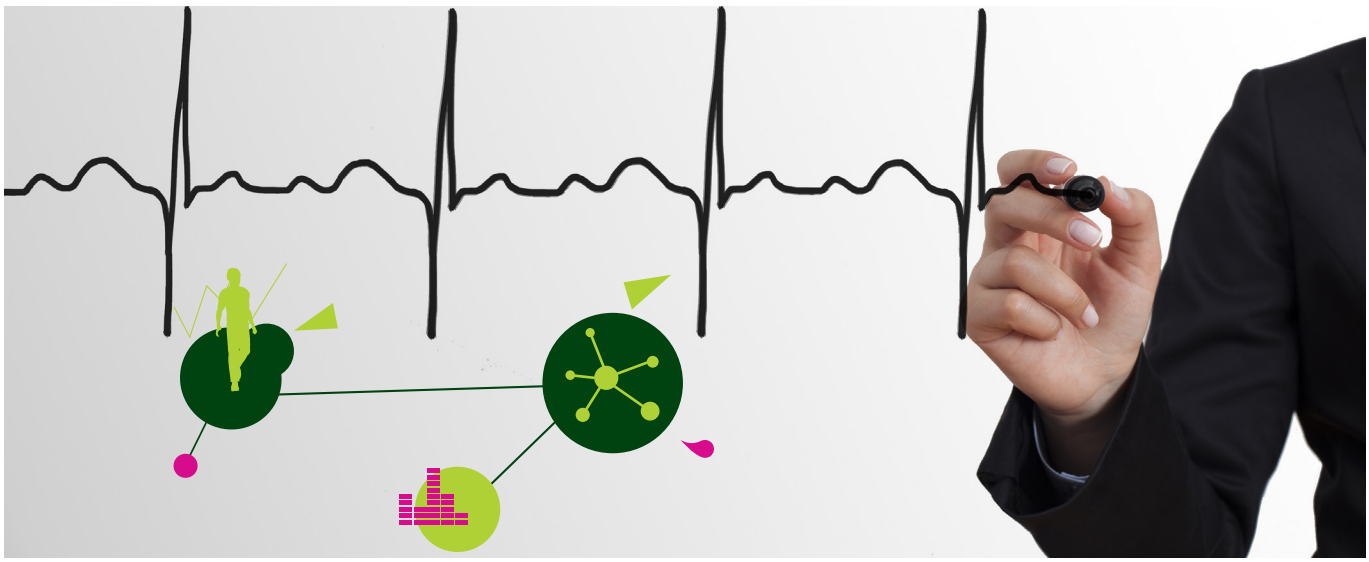
Repetitive voltage suppressors for overvoltage protection



The STRVS is the first TVS series to be specified against repetitive overvoltages in high temperature conditions

In applications, overvoltage constraints may not always come from lightning, electrical overstress or electrostatic discharge, but from the circuit itself. In such cases, standards do not apply.

Repetitive surges may raise protection device temperature. This is why protection devices must be selected according to their power capability at high junction temperatures and their clamping voltage specified at high temperature.

KEY FEATURES

Application driven

- 2 key parameters specified:
  - V_{CL} for multiple temperatures and peak current from 0 to 2 A
  - R_D for multiple temperatures and peak currents from 0 to 2 A
- Application note supporting product selection
- Improved power derating versus temperature

TARGETED APPLICATIONS

MOSFET and IGBT protection in:

- Solar inverters
- SMPS and auxiliary power supplies
- Smart metering
- LED drivers

KEY BENEFITS

- Better Transil™ selection for cost optimization (oversizing avoided)
- Fixed and reliable clamping voltage not sensitive to output load
- Better protection with smaller package versus competition
- Reduced power consumption versus discrete protection (RC snubber)
- Customer design effort reduced

DESIGN NOTES

Design information and calculations are developed in detail in the application note “Design methodology of TVS in repetitive mode: STRVS”. Below, you will find a short summary of the steps to be considered.

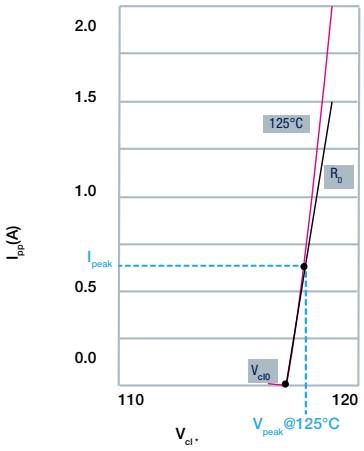
1. V_{RM} selection
   The V_{RM} selected should be higher than the highest voltage at STRVS nodes during normal operating conditions.
2. V_{CL} @ 125 °C verification
   The designer should check that V_{CL} @ 125 °C is low enough to protect the MOSFET during surges (assuming that 125 °C is the worst case application temperature).
3. STRVS temperature verification

- The power dissipated in the STRVS should be calculated.
  - $P_{step} = I_{peak} x (3xV_{CL0} + 2xI_{peak} xR_D)/6$
  - $P_D = t_p xF_{SW} xP_{step}$
- The calculated temperature has to be lower than 125 °C:
  - $T_{jpeak} = R_{th(j-a)} xP_D + T_{amb}$

STRVS PROTECTION FOR ST COMPANION CHIPS

- VIPers
- HVLEDs
- Power MOSFETs
- ALTAIR

APPLICATION KEY PARAMETERS



Glossary

- V_{peak}: Clamping voltage @ I_{peak} for a given temperature (25/85/125°C)
- V_{CL0}: Voltage value where the R_D line crosses the 0 A axis
- R_d: Dynamic resistance allowing designer to linearize the avalanche zone for $0 < I < I_{peak}$
- I_{peak}: Maximum current flowing through the STRVS during each pulse

DEVICE SUMMARY

Part number	I_{RM} max @ V_{RM} (25 °C)		V_{BR} (typ. with I_R = 1 mA)	Values @ 125 °C				Packages
	(µA)	(V)	(V)	I_{peak} (A)	V_{peak} (typ) (V)	V_{CL0} (V)	R_D(Ω)	
STRVS118X02C(*)	0.2	85	100	2	118	116	1.0	SMC
STRVS142X02F(*)	1	102	120	2	142	140	1.0	DO-201
STRVS182X02F(*)	1	128	150	2	182	177	2.5	DO-201
STRVS185X02B/E(*)	0.2	128	150	2	185	178	3.5	SMB/DO-15
STRVS222X02F(*)	1	154	180	2	222	213	4.5	DO-201
STRVS225X02E(*)	0.5	154	180	2	225	214	5.5	DO-15
STRVS241X02E(*)	0.5	171	200	2	241	234	3.5	DO-15
STRVS248X02C(*)	0.2	171	200	2	248	238	5.0	SMC
STRVS252X02F(*)	1	171	200	2	252	239	6.5	DO-201
STRVS280X02F(*)	1	188	220	2	280	263	8.5	DO-201

Note: (*): available in october 2012