

Reference Design:

HFRD-26.0

Rev. 8; 11/08

As of July, 2008 this reference design board is no longer available.
Gerber files and schematics are available upon request.

REFERENCE DESIGN
GEPON SFF Host Board



Maxim Integrated Products



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1 Overview

High-Frequency Reference Design (HFRD-26.0) is a Small Form Factor (SFF) host board designed for evaluating GEAPON and GPON SFF modules. The host board can be used to test a variety of different modules, but includes additional features for testing, monitoring, and programming HFRD-25.2 (Low-cost GEAPON SFF ONT with μ C).

HFRD-26.0



1.1 Features

- SFF MSA Compatible
- GUI Interface with USB Connection
- SMA Connectors for High-Speed Data
- Schematics and Bill of Materials Provided
- Gerber Files Available

2 Obtaining Additional Information

For more information about the reference design email to: <https://support.maxim-ic.com/>.

3 Reference Design Details

HFRD-26.0 provides micro-strip transmission lines and SMA connectors for transmitted data, received data, and burst enable. Supply current monitors, voltage monitors, and LEDs are provided for diagnostic information. All other I/O ports are controlled through the graphical user interface (GUI) (Figure 1). Connections to the module board are made through a 20-pin SFF connector (Note: some I/O pins have been redefined to facilitate GEAPON operation and enhanced evaluation options of HFRD-25.2).

HFRD-26.0 comes complete with a Windows® operating system based graphical user interface (GUI). The GUI communicates to the board through an easy-to-use USB connection. Through the software, the user can monitor and change all of the critical parameters of the HFRD-26.0 and HFRD-25.2 reference design boards.

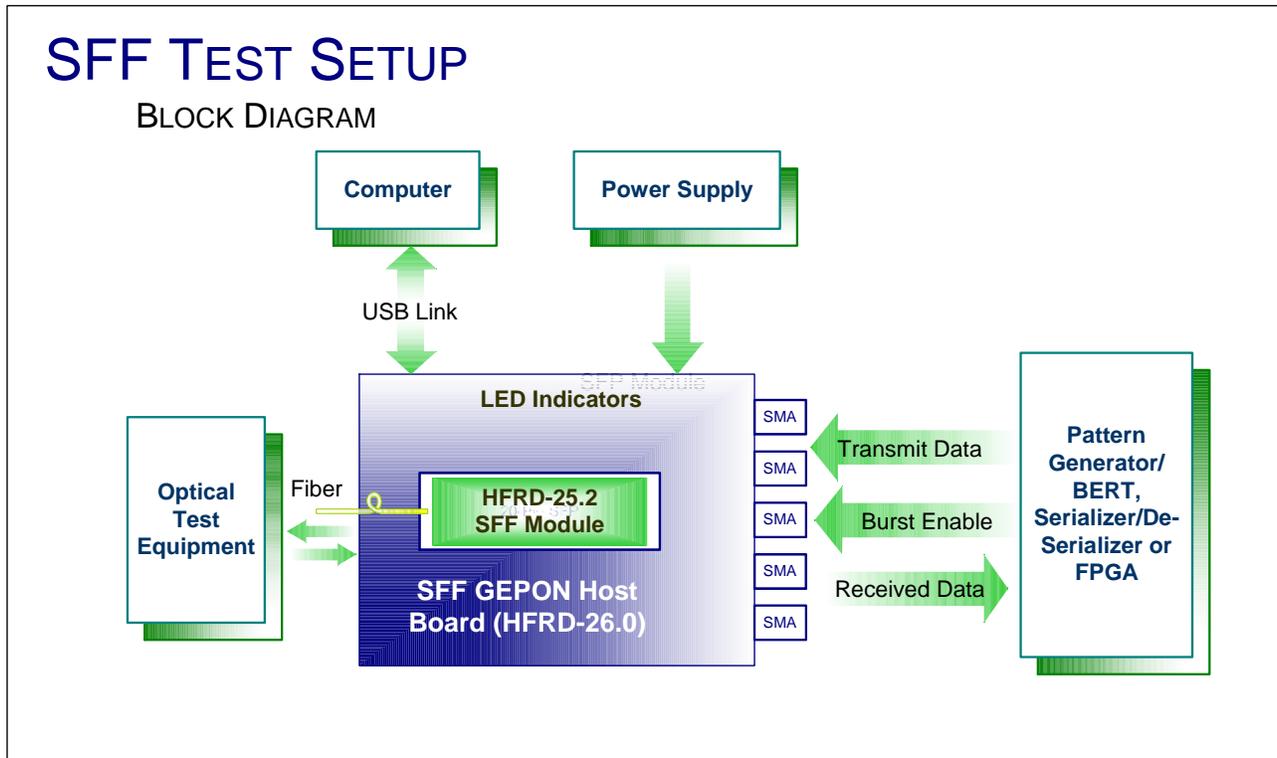


Figure 1. SFF test setup (block diagram).

4 Application Information

4.1 The GUI Evaluation Software

The GUI evaluation software is available at: <http://www.maxim-ic.com/tools/other/>. Please check the website regularly for updates and revision history.

4.1.1 Software Requirements

The evaluation software is designed to operate on Microsoft® Windows 2000 or Windows XP operating systems. The software can also be used on Windows 98; however, in that latter case, unstable software operation can occur if the USB cable is unplugged without first stopping the device from windows.

4.1.2 Software Installation

To install the software, simply download the file (<http://www.maxim-ic.com/tools/other/>) and run it on your computer or run the Setup.exe file from the provided CD ROM. The evaluation software was built on the Microsoft .NET platform. If the current version of this platform is not already installed on your computer, the evaluation software will need an internet connection to download the components and complete the installation.

4.1.3 Software Usage

Figures 2 through 5 are screen shots of the GUI that highlight various features. A brief explanation of the features is listed below each figure.

4.2 ISP Programming

The Atmel® microcontroller (ATTiny24) used on HFRD-25.2 can be in-system programmed using the J9 connector and an ISP programmer such as the AVRISP mkII (www.atmel.com). The evaluation board must be placed in programming mode (Figure 5) before the μ C can be in-system programmed. (Note: HFRD-25.2 is shipped preprogrammed.) Follow the AVRISP programmer guidelines when connecting to and programming the μ C on the HFRD-25.2 reference-design board.

4.3 Layout Considerations

Single-ended transmission lines are designed on the HFRD-26.0 host board. Changing the PCB layer profile (see Section 11) can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated.

5 Evaluation Quick Start

5.1 Evaluation Notice

The HFRD-25.2 reference design has DC-coupled I/Os and a large optical output signal (approximately -1.0dBm to +1.0dBm). Care should be taken to ensure that all signal levels are within the proper range (common-mode, differential swing, optical input/output power, etc.). Failure to do so may damage to the test equipment or reference design. The HFRD-25.2 reference design document (www.maxim-ic.com/products/fiber/reference_designs.cfm) can be used as a guide when verifying the proper levels and connections.

Precautions must also be taken in order to ensure safe operation when using a device with a laser diode. Laser light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm, injury, or test-equipment damage as a result of the use of this reference design.

5.2 Evaluation Setup

To evaluate the HFRD-25.2 reference design using the HFRD-26.0 host board:

1. Install the user software as indicated in section 4.1.2.
2. Clean and inspect the fiber pigtail connector (HFRD-25.2) and then recap the fiber connector. In all of the proceeding steps, assume that laser light could be emitted from the laser diode. Handle the fiber with care to avoid eye or equipment damage.
3. Connect the fiber pigtail to an optical attenuator and/or optical to electrical converter. Note that the output of the laser pigtail can be in excess of 2dBm. Use safe handling procedures and use an optical

attenuator, if needed, to ensure that the power level is within the safe operating limits of the test equipment.

4. Connect HFRD-26.0 to the computer using the provided USB cable. When the cable is inserted, D6 (USB_PWR) should be illuminated. Wait to start the software until step 7.
5. Connect the HFRD-25.2 into the HFRD-26.0 SFF Host Board.
6. Apply a +5V supply to J14 (5V_Input) and J16 (GND). Set the current limit to 250mA and turn the supply on. The host board will generate the +3.3V supply needed for HFRD-25.2.
7. Run the HFRD-26.0 software from the Windows operating system start menu:
 - start
 - All Programs
 - Maxim Integrated Products
 - HFRD-26: GEAPON...
8. Press Initialize/Test Communication. If everything is connected correctly, a screen similar to that shown in Figure 3 should appear. Wait to enable the driver until the proper mode of operation (see HFRD-25.2 document) is set and the remaining connections are made.
9. To complete the setup, review the HFRD-25.2 document carefully, noting the DC-coupled connections of TD. Make the appropriate optical and electrical connections by using the Recommended Operating Conditions (HFRD-25.2 document, Page 5) and SFF Module Pin Description (HFRD-25.2 document, page 38) sections as a reference. If assistance is required, please email questions to: <https://support.maxim-ic.com/>.

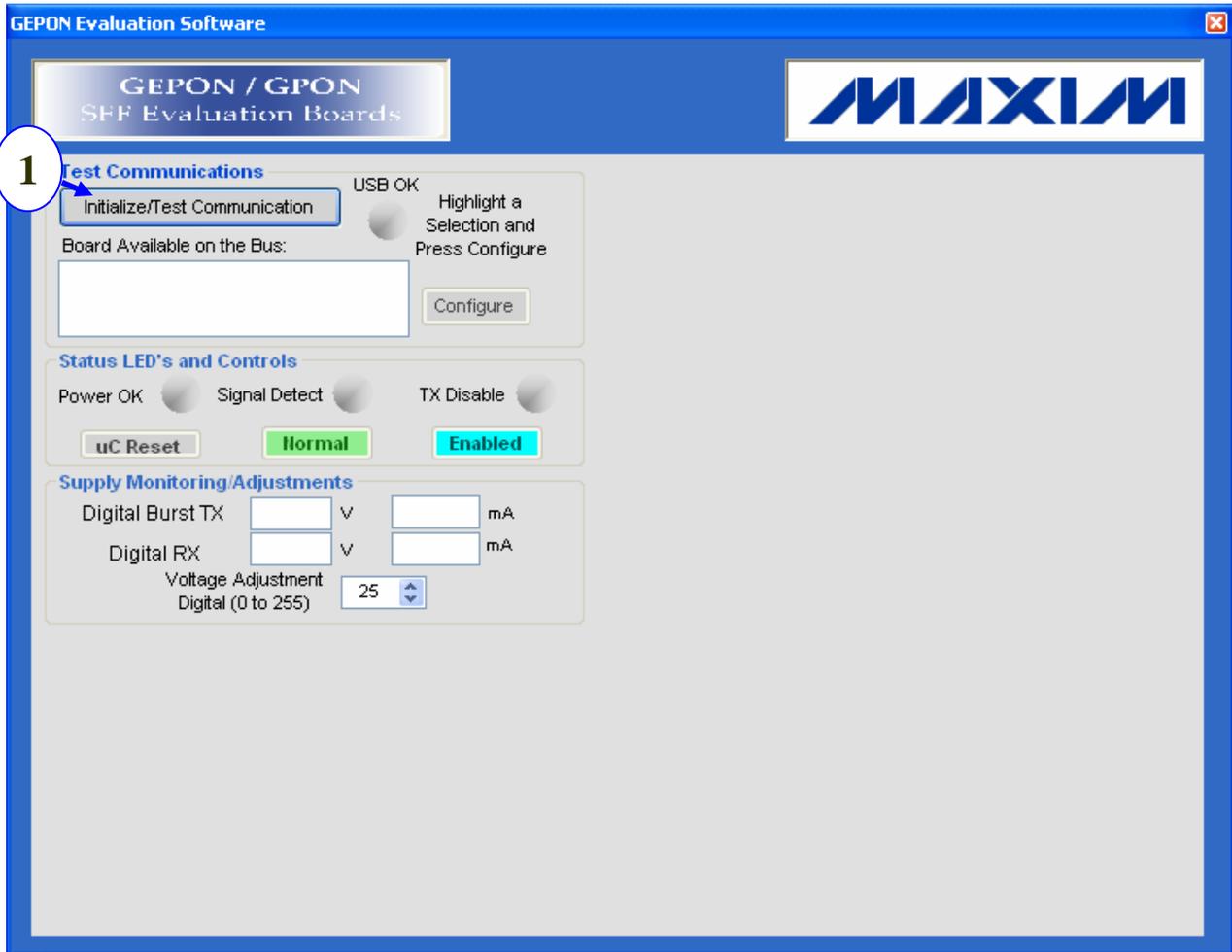


Figure 2. Initial screen.

1. **Initialize/Test Communication:** Pressing this button resets the GUI interface and initializes a test sequence to determine if the HFRD-26.0 host board and HFRD-25.2 module board are attached correctly. If the software can communicate with both boards, the features shown in Figure 3 are available to the user.

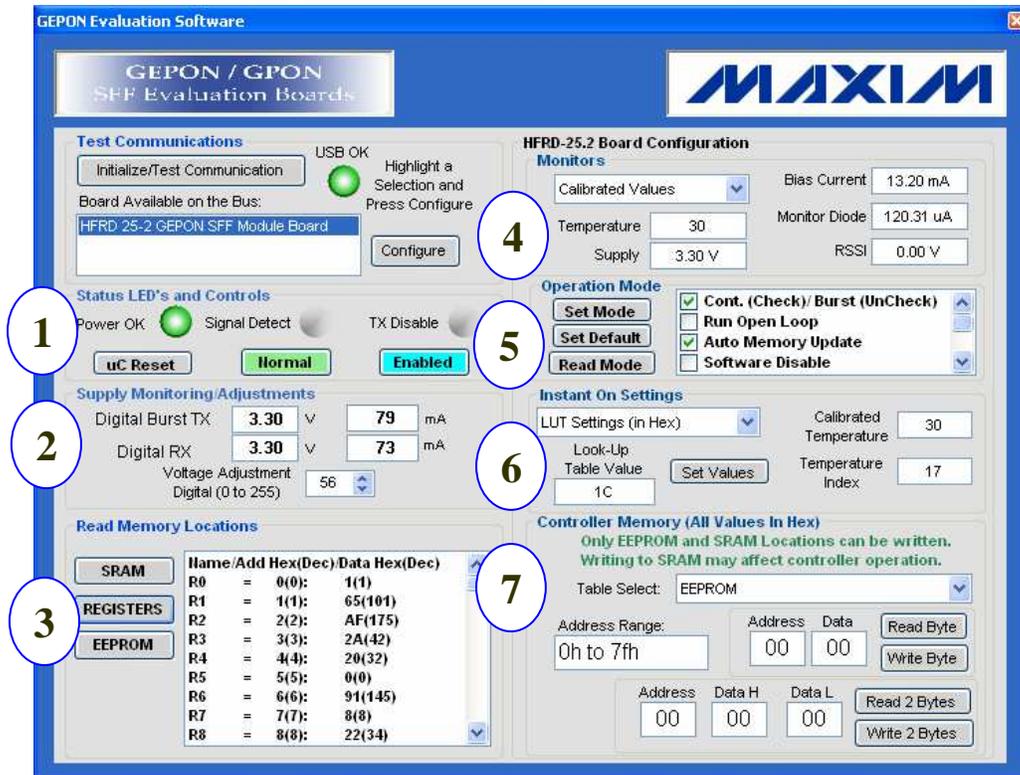


Figure 3. Overview.

1. **Status LED's and Controls:** Pressing “uC Reset” creates a reset pulse for re-initializing the μ C on the HFRD-25.2 board. Pressing “Normal” or “Program” toggles the software operation from normal operation to a programming mode (using an external ISP programmer). Pressing “Enabled” or “Disabled” enables or disables the transmitter.
2. **Supply Monitoring/Adjustments:** The transmitter and receiver supply voltage and the current on the HFRD-26.0 board are displayed. The supply voltage can be adjusted from approximately 2.9V (digital value = 255) to 3.7V (digital value = 0) by using the voltage-adjustment up and down arrows.
3. **Read Memory Locations:** This displays all of the memory locations and register values of the μ C. The standard name (e.g. SREG) is also listed when reading the register values.
4. **Monitors:** This reports the temperature, supply, bias current, monitor-diode

- current, and RSSI (if available) values that are monitored by HFRD-25.2. The values can be reported in hex, decimal, or calibrated values.
5. **Operation Mode:** Sets the mode of operation (see HFRD-25.2 document for additional details). Press “ μ C Reset” or cycle power for the new settings to take effect.
6. **Instant On Settings:** HFRD-25.2 provides an optional “Instant-On” feature that allows the laser driver to start up to the correct laser bias and modulation current values almost instantly after a power cycle or transition from disable to enable state. (See HFRD-25.2 document for additional details.) Press “Set Values” to open the window shown in Figure 4.
7. **Controller Memory:** This allows the user to read and write any of the SRAM or EEPROM memory locations, as well as read any of the internal registers.

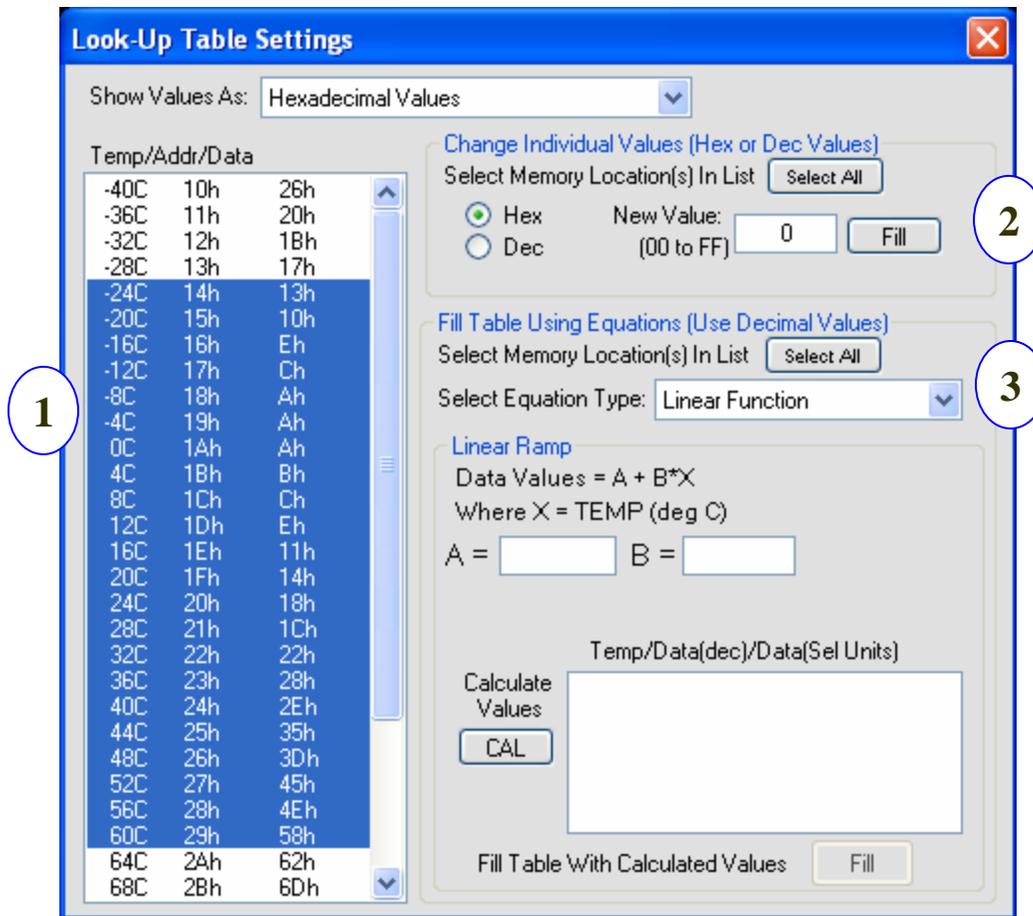


Figure 4. Overview.

1. **Temp/Addr/Data:** This list box shows the current values in the lookup table. A new table entry is allocated for every 4°C from -40°C to +100°C.
2. **Change Individual Values:** This allows the user to enter a new value in the lookup table for any location that is selected.
3. **Fill Table Using Equations:** This allows the user to fill the selected table values using an equation. The values are first calculated by pressing the “CAL” button. The user can verify the calculated values and then press the “Fill” button to write the new values to the lookup table. Options are available for linear functions, power functions, and polynomial functions (up to 4th order).

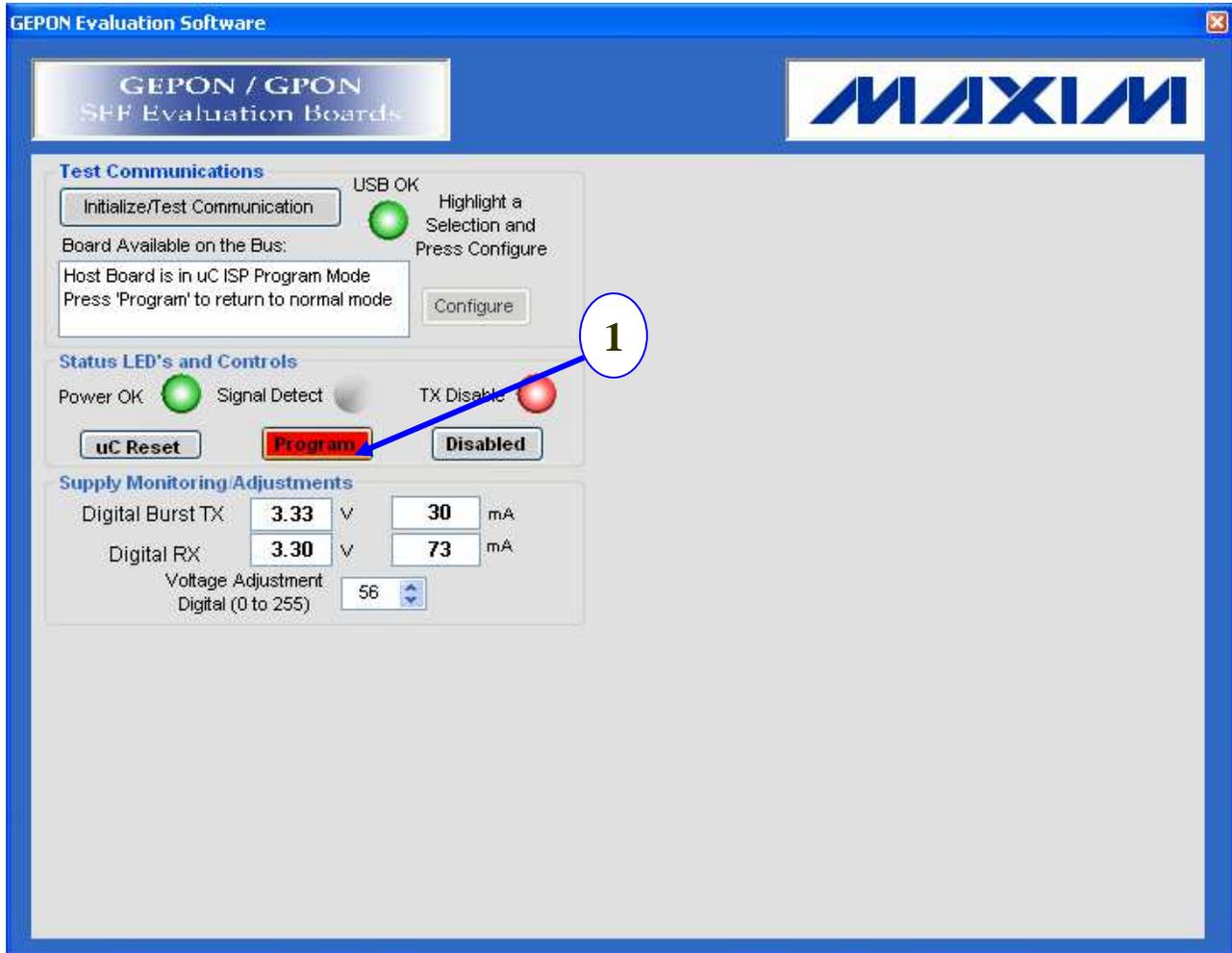


Figure 5. Programming mode.

1. **Normal/Program Button:** Pressing “Normal” or “Program” toggles the GUI operation between those modes. When in program mode (Figure 5), the μC can be programmed using an In-System Programmer (ISP) and the J9 connector. The software can be returned to normal mode by pressing either “Program” or “Initialize/Test Communications.”

6 I/O and Control Description

Component	Name	Function
J1	TX_BRST	Burst enable input. The laser driver output is enabled when the TX_BRST signal is asserted. TTL-compatible, SMA connector
J4		SFF Module Connector (See Section 7)
J9		ISP connector: Pin 1 → MISO Pin 2 → V _{CC} (+3.3V) Pin 3 → SCK Pin 4 → MOSI Pin 5 → RESET Pin 6 → GND
J10	TD+	Transmitted data noninverted input, DC-coupled, SMA connector
J15	TD-	Transmitted data inverted input, DC-coupled, SMA connector
J13	RD+	Received data noninverted output, AC-coupled, SMA connector
J11	RD-	Received data inverted output, AC-coupled, SMA connector
J14	5V_INPUT	Power supply +5V input. A LDO regulator supplies a +3.3V supply voltage to the SFF module.
J16	GND_INPUT	Power supply ground input
D6	USB_PWR	LED illuminates when the host board (HFRD-26.0) is connected to a computer through a USB cable.
D7	SD	LED illuminates when signal detect is asserted by the module.
D9	PROG	LED illuminates when the host board is in normal operation mode. The LED is not illuminated when it is in ISP programming mode.
D10	M-POK	LED illuminates when the +3.3V supply, generated by an LDO regulator, is operating properly.
D16	$\overline{\text{TX-ENABLE}}$	LED illuminates when the driver is disabled.
TP17, TP23	GND	Ground test points

7 Signal Definitions (20-Pin Connector, J4)

I/O direction assumes the SFF module as the reference.

Connector Pin (J1)	I/O Type	Name	Definition
1	LVTTTL OUTPUT	MISO	Used for ISP programming.
2	SUPPLY	GND	Ground
3	SUPPLY	GND	Ground
4		N.C.	No connection
5		N.C.	No connection
6	SUPPLY	GND	Ground
7	SUPPLY	VCCR	+3.3V receiver power-supply connection
8	LVTTTL OUTPUT	SD	Signal detect. The signal detected is asserted high when the receiver input power is above the set threshold.
9	CML OUTPUT	RD-	Inverted received data output, AC-coupled inside the SFF module
10	CML OUTPUT	RD+	Noninverted received data output, AC-coupled inside the SFF module
11	SUPPLY	VCCT	+3.3V transmitter power-supply connection.
12	SUPPLY	GND	Ground
13	LVTTTL INPUT	TDIS	Transmitter disable. The transmitter is disabled when TDIS is asserted high.
14	INPUT	TD+	Noninverted transmitter data input, DC-coupled*
15	INPUT	TD-	Inverted transmitter data input, DC-coupled*
16	SUPPLY	GND	Ground
17	LVTTTL INPUT	SCL	2-Wire serial interface clock line, pulled high inside HFRD-25.2 module. This pin is also used for ISP programming (SCK).
18	LVTTTL INPUT/OUTPUT	SDA	2-Wire serial interface bidirectional data line, pulled high inside HFRD-25.2 module. This pin is also used for ISP programming (MOSI).
19	LVTTTL COMPATIBLE INPUT	TX_BRST	High-speed burst-enable input, TTL-compatible, DC-coupled*
20	LVTTTL INPUT	RESET	Microcontroller reset input, active low, pulled high on the HFRD-25.2 module

*DC-coupled I/O. Ensure that the DC voltage on these pins is compatible with the test equipment before making any connections.

8 Component List

Designation	Qty	Description
C1-C4, C10, C25-C27, C49, C50, C57, C62, C65, C67, C69-C71, C80, C86, C90-C92	22	0.1 μ F \pm 10% Ceramic Capacitor (0402)
C18, C22	2	33pF \pm 10% Ceramic Capacitor (0402)
C24, C37, C52, C84	4	4.7 μ F \pm 10% Ceramic Capacitor (0805)
C34, C51, C64, C66, C79, C99	6	1 μ F \pm 10% Ceramic Capacitor (0603)
C58, C68, C75, C77	4	0.01 μ F \pm 10% Ceramic Capacitor (0402)
C81	1	4.7 μ F \pm 10% Ceramic Capacitor (0603)
C82, C83	2	0.01 μ F \pm 10% Ceramic Capacitor (0603)
C85	1	0.1 μ F \pm 10% Ceramic Capacitor (0603)
C87, C88	2	1 μ F \pm 20% Ceramic Capacitor (0402)
C89	1	10 μ F \pm 20% Ceramic Capacitor (0603)
D6, D7, D9, D10	4	Green LED
D16	1	Red LED
J1, J10, J11, J13, J15	5	Side-Mount SMA Connector, Tab Contact
J3	1	USB Connector, Tyco 440247-1
J4	1	SFF Socket
J9	1	2x3 Header, 0.1in Spacing
L1, L25, L26	3	1500 Ω Ferrite Bead (0603), TDK MMZ1608A152ET
L2	1	22 μ H Inductor, Taiyo-Yuden CBC3225T220M
L18	1	4.7 μ H Inductor, Taiyo-Yuden CBC3225T4R7M
Q1, Q3	2	PNP MOSFET Transistor, Fairchild FDN306P
R6, R53, R66, R68, R70, R72, R73, R75, R78, R98, R105, R109, R113, R114	15	Open (0402)

R12, R37, R41, R48	4	4.75k Ω \pm 1% Resistor (0402)
R18, R59, R61, R69	4	475 Ω \pm 1% Resistor (0402)
R24	1	1.5k Ω \pm 1% Resistor (0402)
R25, R49-R51, R60, R107, R108	7	10k Ω \pm 1% Resistor (0402)
R40	1	100 Ω \pm 1% Resistor (0402)
R52, R55, R62, R67, R74	5	49.9 Ω \pm 1% Resistor (0402)
R54	1	1k Ω \pm 1% Resistor (0402)
R56-R58, R100, R110	5	0 Ω Resistor (0403)
R63	1	49.9k Ω \pm 1% Resistor (0402)
R64	1	24.9k Ω \pm 1% Resistor (0402)
R65	1	100k Ω \pm 1% Resistor (0402)
R71, R132, R134	3	10 Ω \pm 5% Resistor (0402)
R106	1	681 Ω \pm 1% Resistor (0402)
R111, R112	2	0.1 Ω \pm 1% Resistor (1206)
R130, R131	2	100 Ω \pm 5% Resistor (0402)
TP17, TP23, J14, J15	4	Test points
U3, U13, U17	3	SPDT Analog Switch, MAX4729EXT-T
U6	1	Digital Resistor DS3902U-530
U10	1	Microcontroller, Microchip PIC16C745-I/SO
U12	1	Dual Inverter, Fairchild NC7WZ04P6X
U15	1	LDO Regulator, MAX1793EUE-33
U16	1	Dual Buffer, Fairchild NC7WZ16P6X
U18, U19	2	ADC, Max1362EUB
U20, U22	2	High-Side Current-Sense Amp., MAX4070AUA
U27, U28	2	Bidirectional Level Translator, MAX3370EXK
Y1	1	Crystal, ECS Inc. XC679CT

10 Board Dimensions/Layout

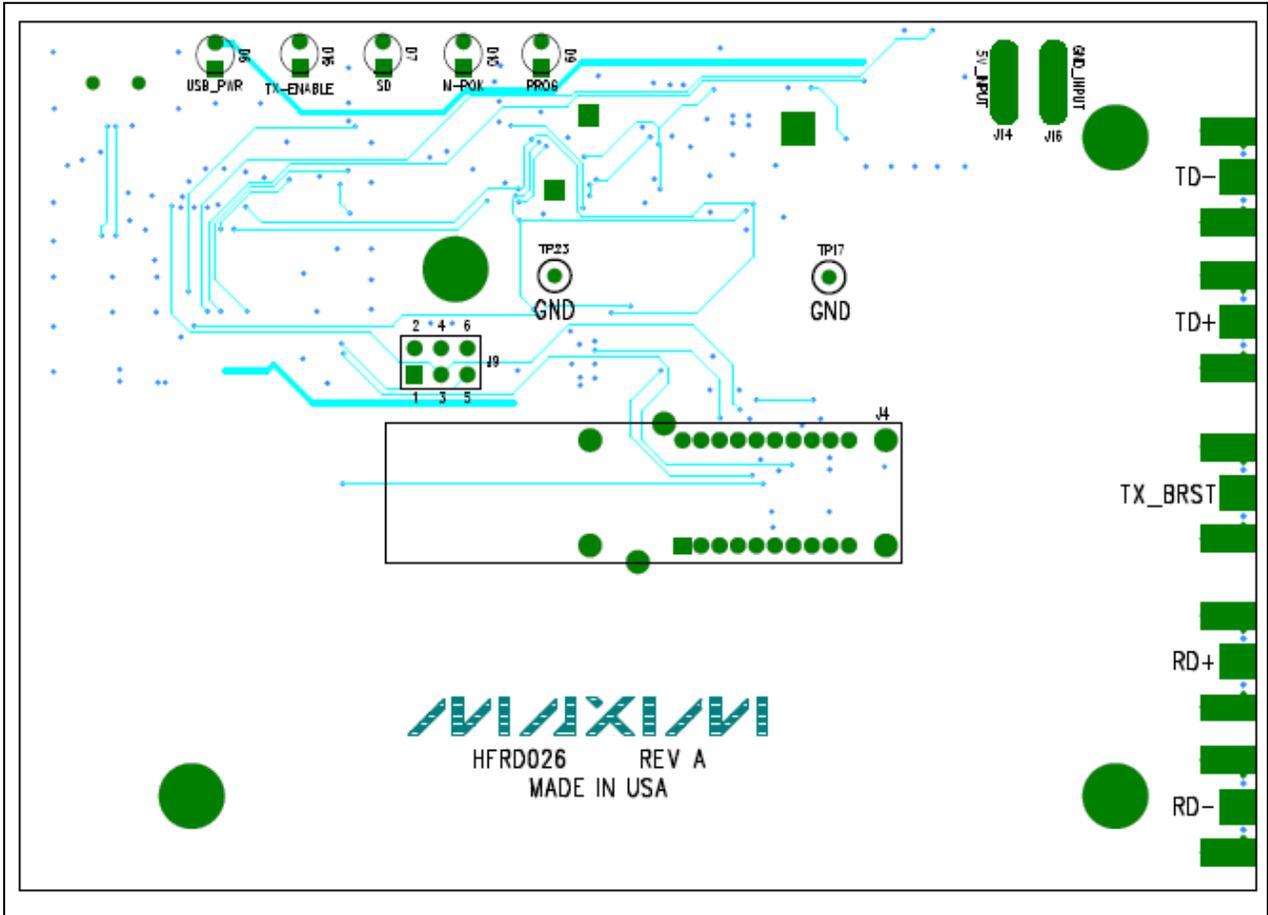


Figure 7. HFRD-26.0 application view, Layer 4.

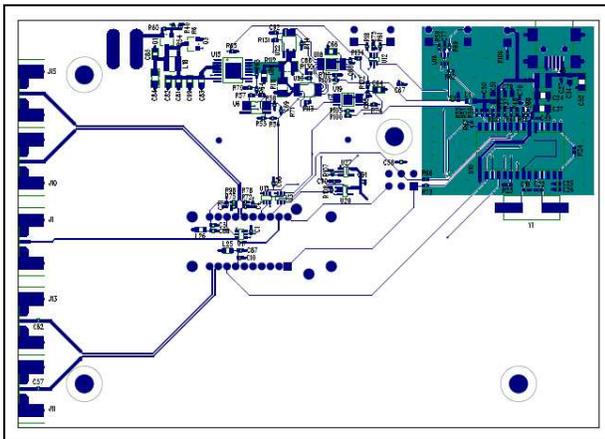


Figure 8. Board layout—component side, Layer 1.

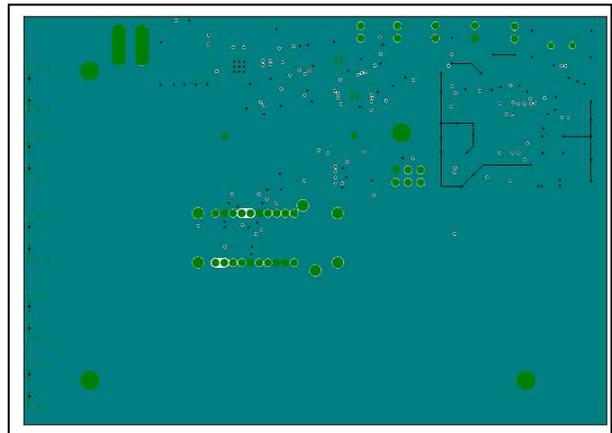


Figure 9. Board layout—ground plane, Layer 2.



Figure 10. Board layout—power plane, Layer 3.

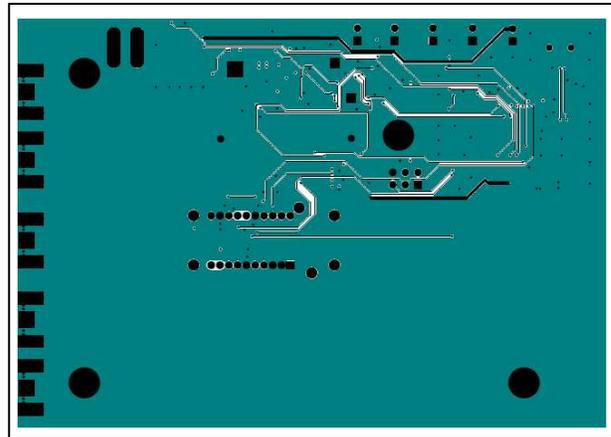


Figure 11. Board layout—solder side, Layer 4.

11 Layer Profile

The HFRD-26.0 GEAPON SFF host board includes controlled-impedance transmission lines. The layer profile is based on the following assumptions:

1. Dielectric material is FR-4 with a dielectric constant of ~ 4.5.
2. 1oz copper foil

	Single Ended	Coupled
A	N.A.	8mil
B	>50mil	10mil
C	8mil	8mil
D	As needed	As needed

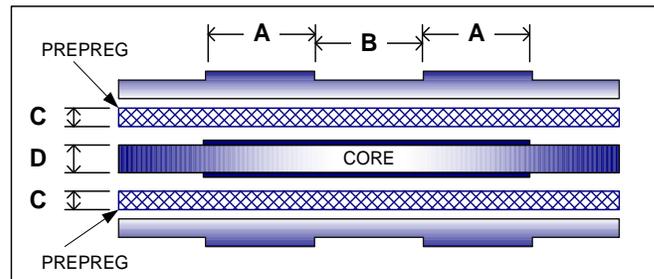


Figure 12. Layer profile.

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