



PIC16C63 → PIC16C63A Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C63 to the PIC16C63A.

TABLE 1: PIC16C63 → PIC16C63A DIFFERENCES

Functional Differences due to Errata or Module Update					
No.	Module	Difference	H/W	S/W	Prog.
1	CCP	CCP Special Event Trigger clears Timer1.	—	✓	—
2		Compare mode drives pin correctly.	—	✓	—
3	Timers	Reading or writing TMR1H or TMR1L may affect TMR1H or TMR1L unexpectedly.	—	✓	—
4		WDT/TMR0 prescaler assignment changes do not affect TMR0 count.	—	✓	—
5	SSP	TMR2 SPI™ clock synchronized to start of SPI Transmission.	—	✓	—
6		Can now transmit multiple words in SPI mode.	—	✓	—
7		Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).	—	✓	—
8		I ² C™ no longer generates ACK pulses when module is enabled.	—	✓	—
9	USART	Async receive errors due to BRGH setting corrected.	—	✓	—
10	Oscillator	TOST delay may be skipped when waking from SLEEP.	—	✓	—
11	RESET	Short $\overline{\text{MCLR}}$ pulses may cause improper operation on the PIC16C63A.	✓	—	—
12		Operating voltage and frequency ranges have been redefined.	✓	—	—

H/W - Issues may exist with regard to the application circuits.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist when writing the program to the controller.

TABLE 2: ELECTRICAL SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic	PIC16C63			PIC16C63A			Unit	
			Min	Typ†	Max	Min	Typ†	Max		
Core										
D001	VDD	Supply Voltage	4.0	—	6.0	4.0	—	5.5	V	
D001A		XT, LP and RC mode	4.5	—	5.5	4.0	—	5.5	V	
		HS mode BOR enabled (Note 1)	—	—	—	VBOR	—	5.5	V	
D005	VBOR	Brown-out Reset Voltage	3.7	4.0	4.3	3.65	—	4.35	V	
D150	VOD	Open Drain High Voltage on RA4	—	—	14.0	—	—	8.5	V	
SSP in SPI mode										
71	Tsch	SCK input high time (Slave mode)	Continuous	Tcy+20	—	—	1.25Tcy + 30	—	—	ns
71A			Single Byte							
72	TscL	SCK input low time (Slave mode)	Continuous	Tcy+20	—	—	1.25Tcy + 30	—	—	ns
72A			Single Byte							
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge	50	—	—	100	—	—	ns	
73A (Note 2)	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	—	—	—	1.5Tcy + 40	—	—	ns	
74	Tsch2diL TscL2diL	Hold time of SDI data input to SCK edge	50	—	—	100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX							
78	TscR	SCK output rise time (Master mode)	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX							
80	Tsch2doV TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	—	—	50	ns
			PIC16LCXX							
83	Tsch2ssH TscL2ssH	SS ↑ after SCK edge	—	—	—	—	1.5Tcy + 40	—	—	ns

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate until VDD drops below VBOR.

2: Specification 73A is only required if specifications 71A and 72A are used.

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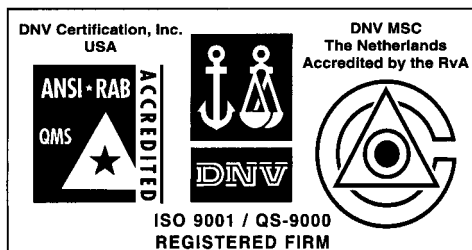
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