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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

## Graphic Display Module

### Part Number

G128ALGSGSW6WTC3XAM

### Overview

128x128(71.3x75.41), STN, Gray background, White Edge lit, Bottom view, Wide temp, Transflective (positive), 3.0V LCD, 3.3V LED, Controller=ST7528, RoHS Compliant

## 1.Features

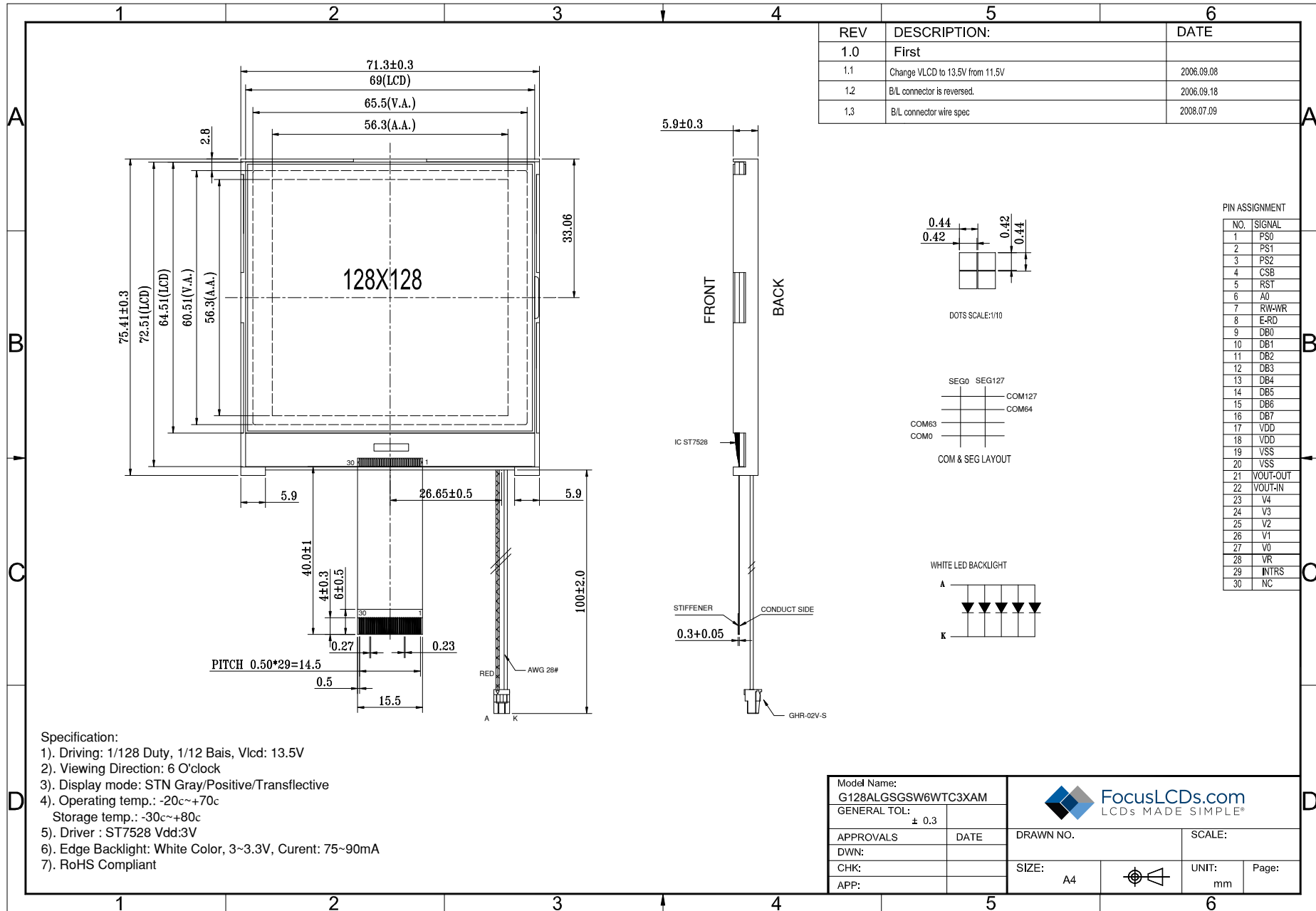
1. 128X128 dots
2. Built-in controller (ST7528)
3. +3.0V power supply
4. 1/128 duty cycle;1/12bias
5. BKL to be driven by A, K.

<b>LCD type</b>	<input type="checkbox"/> FSTN positive		<input type="checkbox"/> FSTN Negative	
	<input type="checkbox"/> STN Yellow Green	<input checked="" type="checkbox"/> STN Gray		<input type="checkbox"/> STN-Blue
<b>View direction</b>	<input checked="" type="checkbox"/> 6 O'clock		<input type="checkbox"/> 12 O'clock	
<b>Rear Polarizer</b>	<input type="checkbox"/> Reflective		<input checked="" type="checkbox"/> Transflective	<input type="checkbox"/> Transmissive
<b>Backlight Type</b>	<input type="checkbox"/> LED Array	<input type="checkbox"/> EL	<input type="checkbox"/> Internal Power	<input type="checkbox"/> 4.2V input
	<input checked="" type="checkbox"/> LED Edge	<input type="checkbox"/> CCFL	<input checked="" type="checkbox"/> External Power	<input checked="" type="checkbox"/> 3.0 input
<b>Backlight Color</b>	<input checked="" type="checkbox"/> White	<input type="checkbox"/> Amber	<input type="checkbox"/> Blue-Green	<input type="checkbox"/> Yellow-Green
<b>Temperature Range</b>	<input type="checkbox"/> Normal		<input type="checkbox"/> Wide	<input checked="" type="checkbox"/> Super Wide
<b>DC to DC circuit</b>	<input checked="" type="checkbox"/> Build-in		<input type="checkbox"/> Not Build-in	
<b>EI Driver IC</b>	<input type="checkbox"/> Build-in		<input checked="" type="checkbox"/> Not Build-in	
<b>Touch screen</b>	<input type="checkbox"/> With		<input type="checkbox"/> Without	
<b>Font type</b>	<input type="checkbox"/> English-Japanese	<input type="checkbox"/> English-European	<input type="checkbox"/> English-Russian	<input checked="" type="checkbox"/> other

## 2. MECHANICAL SPECIFICATIONS

Module size	71.3 mm(L) * 75.41mm(W) * 5.9(H)mm
Viewing area	65.5 mm(L) * 60.51 mm(W)
Dots size	0.42 mm(L) * 0.42 mm(W)
Dots pitch	0.44 mm(L) * 0.44 mm(W)
Weight	Approx.

### 3.Outline dimension



#### 4. Absolute maximum ratings

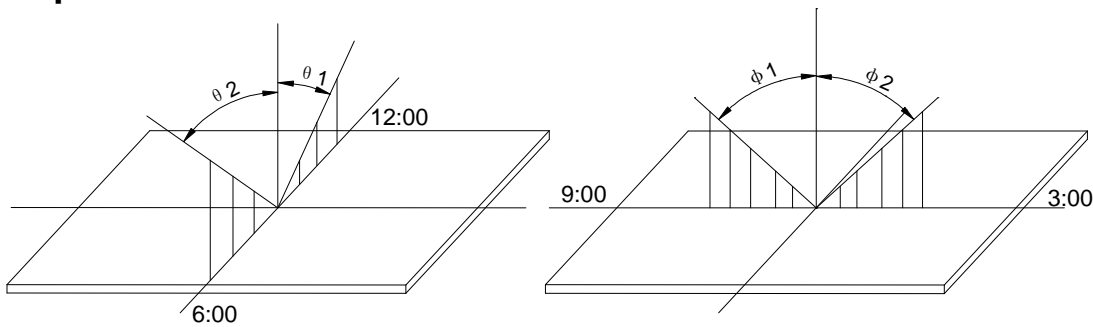
Item	Symbol	Standard			Unit
Power voltage	$V_{DD}-V_{SS}$	0.3	-	3.6	V
Input voltage	$V_{IN}$	VSS	-	VDD	
Operating temperature range	$T_{OP}$	-20	-	+70	°C
Storage temperature range	$T_{ST}$	-30	-	+80	

#### 5. Interface pin description

Recommended Connector: FH19C-30S-0.5SH(99)

Pin no.	Symbol	External connection	Function
1~3	PS0~PS2	I	Microprocessor interface select input pin - PS[2:0]=001: 8080-series parallel MPU interface - PS[2:0]=011: 68000-series parallel MPU interface - PS[2:0]=000: 3-Line-SPI MPU interface - PS[2:0]=010: 4-Line-SPI MPU interface - PS[2:0]=100: IIC-SPI MPU interface
4	CSB	I	Chip select input pins
5	RST	I	Reset input pin
6	A0	I	Register select input pin
7	RW-WR	I	Read / Write execution control pin
8	E-RD	I	Read / Write execution control pin
9~16	DB0~DB7	I/O	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
17	VDD	Power supply	Power supply for LCM (+3.0V)
18	VDD	Power supply	Power supply for LCM (+3.0V)
19	VSS	Power supply	
20	VSS	Power supply	
21	VOUT-OUT	supply	If the internal Vout voltage generator is used, the VOUT_IN & VOUT_OUT must be connected together. If an external supply is used, this pin must be left open.
22	VOUT-IN	supply	An external Vout supply voltage can be supplied using the VOUT_IN pad. In this case, VOUT_OUT has to be left open, and the internal voltage generator has to be programmed to zero.
23~27	V4~V0	I/O	LCD driver supply voltages
28	VR	I	V0 voltage adjustment pin
29	INTRS	I	Internal resistor select pin
30	NC		

## 6. Optical characteristics



STN type display module (Ta=25°C, VDD=3.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle (6 O'clock)	Left--Right	Ta=25°C	-	60	-	deg
	Top--Bottom		-	70	-	
Contrast ratio	CR	Ta=25°C	3	5	-	-
Response time	Rise		-	150	250	ms
	Tall	-	200	300		

## 7. Electrical characteristics

DC characteristics

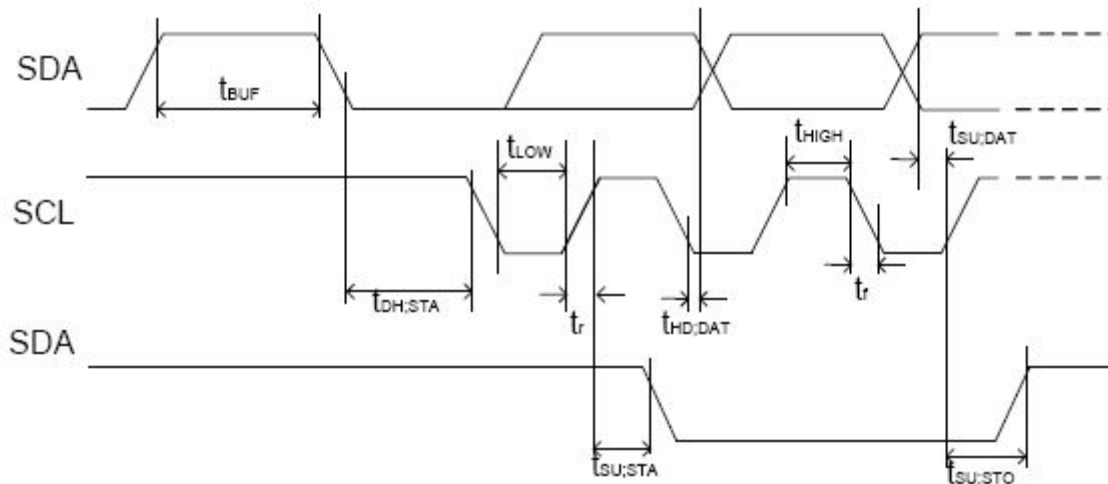
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V <sub>DD</sub> -V <sub>0</sub>	Ta =25°C	-	3.0	-	V
Input voltage	V <sub>DD</sub>		-	3.0	-	
Supply current	I <sub>DD</sub>	Ta=25°C, V <sub>DD</sub> =3.0V	-	0.25	0.45	mA
Input leakage current	I <sub>LKG</sub>		-	-	1.0	uA
“H” level input voltage	V <sub>IH</sub>		2.2	-	V <sub>DD</sub>	V
“L” level input voltage	V <sub>IL</sub>	Twice initial value or less	0	-	0.6	
“H” level output voltage	V <sub>OH</sub>	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V <sub>OL</sub>	LOH=1.6mA	-	-	0.4	

Backlight information

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I <sub>LED</sub>	Ta =25°C, V=3.0V	75	-	90	mA
Supply voltage	V <sub>f</sub>		3.0	-	3.3	V
Reverse voltage	V <sub>R</sub>	Ta=25°C,	-	5.0	-	
Luminous Intensity	I <sub>V</sub>	I <sub>LED</sub> =80mA	-	-	-	Cd/m <sup>2</sup>
Peak wavelength	V <sub>IH</sub>		-	-	-	nm

## 8. TIMING CHARACTERISTICS

### SERIAL INTERFACE(IIC Interface)



(VDD=3.3V, Ta=-30~85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
SCL clock frequency	SCL	FSCLK		-	400	kHZ
SCL clock low period	SCL	TLOW		1.3	-	us
SCL clock high period	SCL	THIGH		0.6	-	us
Data set-up time	SI	TSU;Data		100	-	ns
Data hold time	SI	THD;Data		0	0.9	us
SCL,SDA rise time	SCL	TR		20+0.1Cb	300	ns
SCL,SDA fall time	SCL	TF		20+0.1Cb	300	ns
Capacitive load represented by each bus line		Cb		-	400	pF
Setup time for a repeated START condition	SI	TSU;SUA		0.6	-	us
Start condition hold time	SI	THD;STA		0.6	-	us
Setup time for STOP ondition		TSU;STO		0.6	-	us
Tolerable spike width on bus		TSW		-	50	ns
BUS free time between a STOP and StART condition	SCL	TBUF		1.3		us

## 9. DESCRIPTION OF FUNCTIONS

### ➤ IIC Interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.

The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

### BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 3.

### START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in

Figure 4.

### SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 5.

- Transmitter: the device, which sends the data to the bus.
- Receiver: the device, which receives the data from the bus.
- Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

### ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the IIC Interface is illustrated in Figure 5.

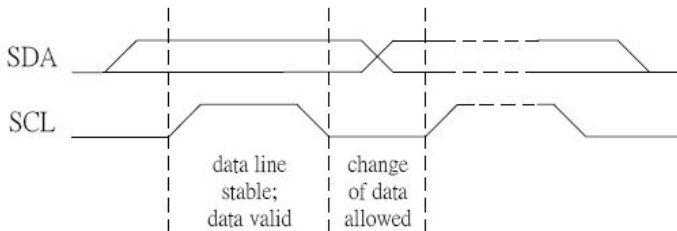


Figure 3 Bit transfer

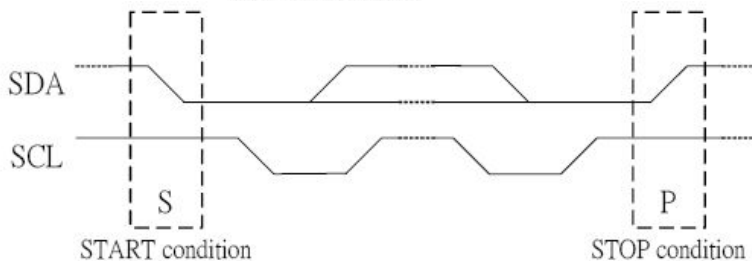


Figure 4 Definition of START and STOP conditions

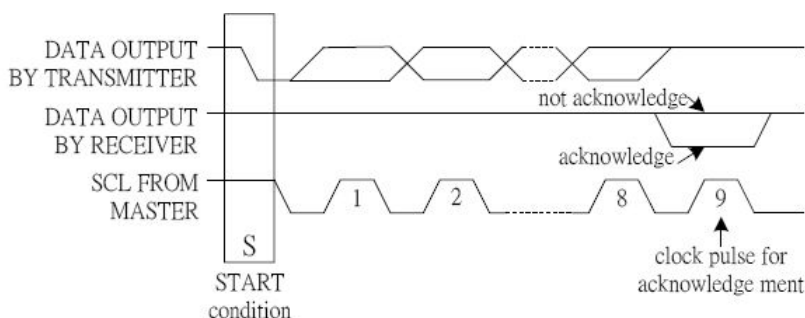


Figure 5 Acknowledgement on the 2-line Interface

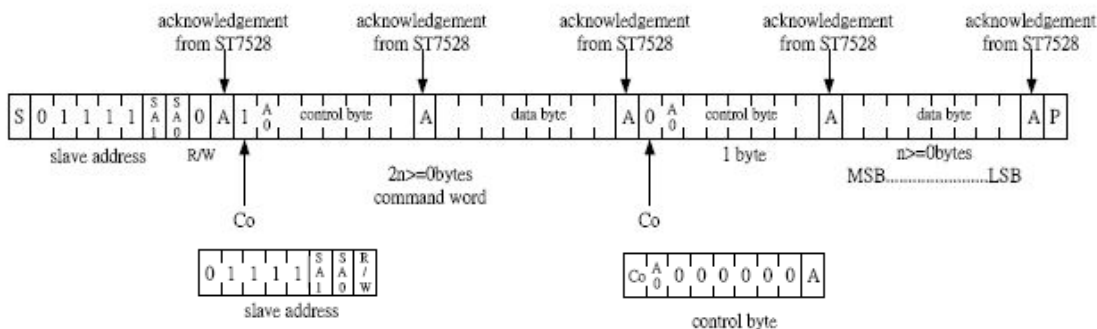
### IIC Interface protocol

The ST7528 supports command, data write addressed slaves on the bus. Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the ST7528. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (VSS) or logic 1 (VDD). The IIC Interface protocol is illustrated in Figure 6.

**Note: ST7528 IIC interface can not use with other slaver IIC device**

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and A0, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7528 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P). If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

**Write mode:**



**Figure 6 2-line Interface protocol**

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

**DISPLAY DATA RAM (DDRAM)**

*When Mode 0 is selected*

The Display Data RAM stores pixel data for the LCD. It is 129-row (17 pages by 8 bits) by 132-column addressable array.

Each pixel can be selected when the page and column addresses are specified. The 129 rows are divided into 16 pages of 8 lines and the 17th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

*When Mode 1 is selected*

The Display Data RAM stores pixel data for the LCD. It is 101-row (13 pages by 8 bits) by 160-column addressable array.

Each pixel can be selected when the page and column addresses are specified. The 101 rows are divided into 12 pages of 8 lines and the 13th page with 4 lines; the Page Address 16 (17th page) is for Icon page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

**Page Address Circuit**

*In mode 0*

It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 16 is a



special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 15, and Page 16 is for Icon page.

*In mode 1*

It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 16 is a special RAM area for the icons and display data DB0 is only valid. The page address is set from 0 to 12, and Page 16 is for Icon page.

**Line Address Circuit**

*In mode 0*

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 128-bit RAM data to the display data latch circuit. When icon is enabled by setting icon control register, display data of icons are not scrolled because the MPU can not access Line Address of icons.

*In mode 1*

The 7-bit Line Address register is set from 0 ~ 99, If the register is set from 100 ~ 127, It will be no operation. The register value will be kept in last value.

**Column Address Circuit**

*In Mode 0, 1*

Column Address Circuit has a 10-bit preset counter that provides Column Address to the Display Data RAM. When set Column Address MSB / LSB instruction is issued, 8-bit [Y9:Y2] are set and lowest 2 bit, Y[1:0] is set to “00”. Since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 9FH. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following Figure 9 and Figure 10.

(Note: in mode read or write in fourth. the column address will turn to next column address)  
 MODE 0

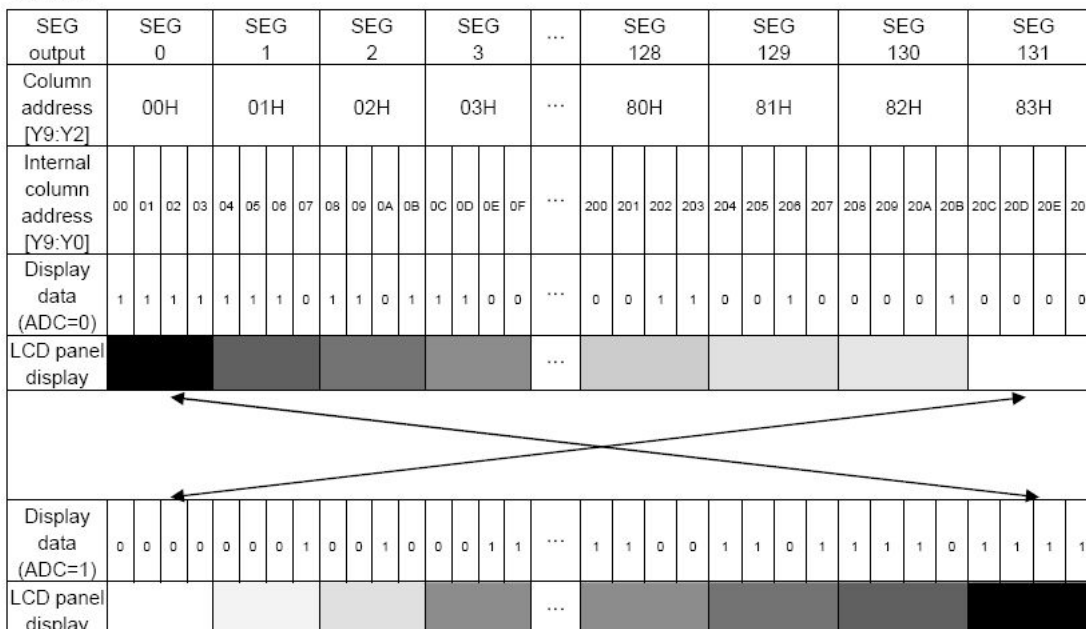


Figure 9. The Relationship between the Column Address and the Segment Outputs

**Mode-0 Display RAM Mapping diagram**



Page Address				Data		Line Address	COM
D3	D2	D1	D0				
0	0	0	0	D0	Page 0	00H	COM0
				D1		01H	COM1
				D2		02H	COM2
				D3		03H	COM3
				D4		04H	COM4
				D5		05H	COM5
				D6		06H	COM6
				D7		07H	COM7
0	0	0	1	D0	Page 1	08H	COM8
				D1		09H	COM9
				D2		0AH	COM10
				D3		0BH	COM11
				D4		0CH	COM12
				D5		0DH	COM13
				D6		0EH	COM14
				D7		0FH	COM15
0	0	1	0	D0	Page 2	10H	COM16
				D1		11H	COM17
				D2		12H	COM18
				D3		13H	COM19
				D4		14H	COM20
				D5		15H	COM21
				D6		16H	COM22
				D7		17H	COM23
⋮				⋮		⋮	
1	1	0	1	D0	Page 13	68H	COM104
				D1		69H	COM105
				D2		6AH	COM106
				D3		6BH	COM107
				D4		6CH	COM108
				D5		6DH	COM109
				D6		6EH	COM110
				D7		6FH	COM111
1	1	1	0	D0	Page 14	70H	COM112
				D1		71H	COM113
				D2		72H	COM114
				D3		73H	COM115
				D4		74H	COM116
				D5		75H	COM117
				D6		76H	COM118
				D7		77H	COM119
1	1	1	1	D0	Page 15	78H	COM120
				D1		79H	COM121
				D2		7AH	COM122
				D3		7BH	COM123
				D4		7CH	COM124
				D5		7DH	COM125
				D6		7EH	COM126
				D7		7FH	COM127
ICON				D0	Page 16	80H	COMS

ICON address just can set by  
ICON ON instruction

0083	SEG0
0182	SEG1
0281	SEG2
0380	SEG3
047F	SEG4
057E	SEG5
067D	SEG6
077C	SEG7
087B	SEG8
097A	SEG9
0A79	SEG10
0B78	SEG11
0C77	SEG12
0D76	SEG13
0E75	SEG14
0F74	SEG15
1073	SEG16
1172	SEG17
1271	SEG18
1370	SEG19
146F	SEG20
156E	SEG21
166D	SEG22
176C	SEG23
186B	SEG24
196A	SEG25
1A69	SEG26
1B68	SEG27
1C67	SEG28
1D66	SEG29
1E65	SEG30
1F64	SEG31
2063	SEG32
2162	SEG33
2261	SEG34
2360	SEG35
245F	SEG36
255E	SEG37
265D	SEG38
275C	SEG39
285B	SEG40
295A	SEG41
2A59	SEG42
2B58	SEG43
2C57	SEG44
2D56	SEG45
2E55	SEG46
2F54	SEG47
3053	SEG48
3152	SEG49
3251	SEG50
3350	SEG51
344F	SEG52
354E	SEG53
364D	SEG54
374C	SEG55
384B	SEG56
394A	SEG57
3A49	SEG58
3B48	SEG59
3C47	SEG60
3D46	SEG61
3E45	SEG62
3F44	SEG63
4043	SEG64
4142	SEG65
4241	SEG66
4340	SEG67
443F	SEG68
453E	SEG69
463D	SEG70
473C	SEG71
483B	SEG72
493A	SEG73
4A39	SEG74
4B38	SEG75
4C37	SEG76
4D36	SEG77
4E35	SEG78
4F34	SEG79
5033	SEG80
5132	SEG81
5231	SEG82
5330	SEG83
542F	SEG84
552E	SEG85
562D	SEG86
572C	SEG87
582B	SEG88
592A	SEG89
5A29	SEG90
5B28	SEG91
5C27	SEG92
5D26	SEG93
5E25	SEG94
5F24	SEG95
6023	SEG96
6122	SEG97
6221	SEG98
6320	SEG99
641F	SEG100
651E	SEG101
661D	SEG102
671C	SEG103
681B	SEG104
691A	SEG105
6A19	SEG106
6B18	SEG107
6C17	SEG108
6D16	SEG109
6E15	SEG110
6F14	SEG111
7013	SEG112
7112	SEG113
7211	SEG114
7310	SEG115
740F	SEG116
750E	SEG117
760D	SEG118
770C	SEG119
780B	SEG120
790A	SEG121
7A09	SEG122
7B08	SEG123
7C07	SEG124
7D06	SEG125
7E05	SEG126
7F04	SEG127
8003	SEG128
8102	SEG129
8201	SEG130
8300	SEG131
8400	SEG132
8500	SEG133
8600	SEG134
8700	SEG135
8800	SEG136
8900	SEG137
8A00	SEG138
8B00	SEG139
8C00	SEG140
8D00	SEG141
8E00	SEG142
8F00	SEG143
9000	SEG144
9100	SEG145
9200	SEG146
9300	SEG147
9400	SEG148
9500	SEG149
9600	SEG150
9700	SEG151
9800	SEG152
9900	SEG153
9A00	SEG154
9B00	SEG155
9C00	SEG156
9D00	SEG157
9E00	SEG158
9F00	SEG159
A000	SEG160
A100	SEG161
A200	SEG162
A300	SEG163
A400	SEG164
A500	SEG165
A600	SEG166
A700	SEG167
A800	SEG168
A900	SEG169
AA00	SEG170
AB00	SEG171
AC00	SEG172
AD00	SEG173
AE00	SEG174
AF00	SEG175
B000	SEG176
B100	SEG177
B200	SEG178
B300	SEG179
B400	SEG180
B500	SEG181
B600	SEG182
B700	SEG183
B800	SEG184
B900	SEG185
BA00	SEG186
BB00	SEG187
BC00	SEG188
BD00	SEG189
BE00	SEG190
BF00	SEG191
C000	SEG192
C100	SEG193
C200	SEG194
C300	SEG195
C400	SEG196
C500	SEG197
C600	SEG198
C700	SEG199
C800	SEG200
C900	SEG201
CA00	SEG202
CB00	SEG203
CC00	SEG204
CD00	SEG205
CE00	SEG206
CF00	SEG207
D000	SEG208
D100	SEG209
D200	SEG210
D300	SEG211
D400	SEG212
D500	SEG213
D600	SEG214
D700	SEG215
D800	SEG216
D900	SEG217
DA00	SEG218
DB00	SEG219
DC00	SEG220
DD00	SEG221
DE00	SEG222
DF00	SEG223
E000	SEG224
E100	SEG225
E200	SEG226
E300	SEG227
E400	SEG228
E500	SEG229
E600	SEG230
E700	SEG231
E800	SEG232
E900	SEG233
EA00	SEG234
EB00	SEG235
EC00	SEG236
ED00	SEG237
EE00	SEG238
EF00	SEG239
F000	SEG240
F100	SEG241
F200	SEG242
F300	SEG243
F400	SEG244
F500	SEG245
F600	SEG246
F700	SEG247
F800	SEG248
F900	SEG249
FA00	SEG250
FB00	SEG251
FC00	SEG252
FD00	SEG253
FE00	SEG254
FF00	SEG255

**MODE 1**

SEG output	SEG 0	SEG 1	SEG 2	SEG 3	...	SEG 156	SEG 157	SEG 158	SEG 159																								
Column address [Y9:Y2]	00H	01H	02H	03H	...	9CH	9DH	9EH	9FH																								
Internal column address [Y9:Y0]	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	...	270	271	272	273	274	275	276	277	278	279	27A	27B	27C	27D	27E	27F
Display data (ADC=0)	1	1	1	1	1	1	1	0	1	1	0	1	1	1	0	0	...	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
LCD panel display	[Shaded]			[Shaded]			[Shaded]			...	[Shaded]			[Shaded]			[Shaded]																
Display data (ADC=1)	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	...	1	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1
LCD panel display	[Shaded]			[Shaded]			[Shaded]			...	[Shaded]			[Shaded]			[Shaded]																

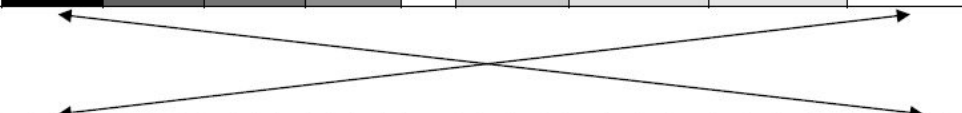


Figure 10. The Relationship between the Column Address and the Segment Outputs

**Mode-1 Display RAM Mapping diagram**



Page Address				Data		Line Address	COM	
D3	D2	D1	D0					
0	0	0	0	D0		00H	COM0	
				D1		01H	COM1	
				D2		02H	COM2	
				D3		03H	COM3	
				D4		04H	COM4	
				D5		05H	COM5	
				D6		06H	COM6	
				D7		07H	COM7	
0	0	0	1	D0		08H	COM8	
				D1		09H	COM9	
				D2		0AH	COM10	
				D3		0BH	COM11	
				D4		0CH	COM12	
				D5		0DH	COM13	
				D6		0EH	COM14	
				D7		0FH	COM15	
0	0	1	0	D0		10H	COM16	
				D1		11H	COM17	
				D2		12H	COM18	
				D3		13H	COM19	
				D4		14H	COM20	
				D5		15H	COM21	
				D6		16H	COM22	
				D7		17H	COM23	
⋮								
1	0	1	0	D0		50H	COM80	
				D1		51H	COM81	
				D2		52H	COM82	
				D3		53H	COM83	
				D4		54H	COM84	
				D5		55H	COM85	
				D6		56H	COM86	
				D7		57H	COM87	
1	0	1	1	D0		58H	COM88	
				D1		59H	COM89	
				D2		5AH	COM90	
				D3		5BH	COM91	
				D4		5CH	COM92	
				D5		5DH	COM93	
				D6		5EH	COM94	
				D7		5FH	COM95	
1	1	0	0	D0		60H	COM96	
				D1		61H	COM97	
				D2		62H	COM98	
				D3		63H	COM99	
				D4				
				D5				
				D6				
				D7				
ICON				D0		Page 16	80H	COMS

ICON address just can set by ICON ON instruction

ADC	SEG
0	01
01	SEG1 59
02	SEG1 58
03	SEG1 57
04	SEG1 56
05	SEG1 55
06	SEG1 54
07	SEG1 53
08	SEG1 52
09	SEG1 51
10	SEG1 50
11	SEG1 49
12	SEG1 48
13	SEG1 47
14	SEG1 46
15	SEG1 45
16	SEG1 44
17	SEG1 43
18	SEG1 42
19	SEG1 41
20	SEG1 40
21	SEG1 39
22	SEG1 38
23	SEG1 37
24	SEG1 36
25	SEG1 35
26	SEG1 34
27	SEG1 33
28	SEG1 32
29	SEG1 31
30	SEG1 30

### LCD DISPLAY CIRCUITS

#### FRC (Frame Rate Control) and PWM (Pulse Width Modulation) Function Circuit

The ST7528 incorporates an FRC function and a PWM function circuit to display a 16-level gray scale. The FRC function and PWM utilize liquid crystal characteristics whose transmittance is changed by an effective

value of applied voltage. The ST7528 provides palette-registers to assign the desired gray level. These registers are set by the instructions and the RESETB.


– **Gray Scale Table of 4 FRC (Frame Rate Control)**

<b>4 FRC setting</b>	<b>(DB7 to DB0)</b>
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Instruction
4th FR (FR4)	Set 4th Frame Pulse Width Modulation Data

**Gray Scale Table of 3 FRC (Frame Rate Control)**

<b>3 FRC setting</b>	<b>(DB7 to DB0)</b>
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Instruction
1st FR (FR1)	Set 1st Frame Pulse Width Modulation Data
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Instruction
2nd FR (FR2)	Set 2nd Frame Pulse Width Modulation Data
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Instruction
3rd FR (FR3)	Set 3rd Frame Pulse Width Modulation Data
4th FR (FR4)	No used
4th FR (FR4)	No used

**Gray Scale Table of 45 PWM (Pulse Width Modulation)**

Dec	Hex	6-bits	PWM (on width)	Note
0	00	000000	0(0/45)	Brighter
1	01	000001	1/45	 ↑         ↓ Darker
2	02	000010	2/45	
3	03	000011	3/45	
4	04	000100	4/45	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
42	2A	101010	42/45	
43	2B	101011	43/45	
44	2C	101100	44/45	
45	2D	101101	1(45/45)	Darker
...	...	...	...	This area is selected to OFF level (0/45 level)
61	3D	111101	0/45	
62	3E	111110	0/45	
63	3F	111111	0/45	

### -Gray Scale Table of 60 PWM (Pulse Width Modulation)

Dec	Hex	6-bits	PWM (on width)	Note
0	00	000000	0(0/60)	Brighter
1	01	000001	1/60	
2	02	000010	2/60	
3	03	000011	3/60	
4	04	000100	4/60	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
...	...	...	...	
56	39	111001	56/60	
57	3A	111010	57/60	
58	3B	111011	58/60	
59	3C	111100	59/60	
60	39	111001	1 (60/60)	Darker
61	3D	111101	0/60	This area is selected to OFF level (0/60 level)
62	3E	111110	0/60	
63	3F	111111	0/60	

### Partial Display on LCD

The ST7528 realizes the Partial Display function on LCD with low-ratio driving for saving power consumption and showing the various display ratio. To show the various display ratio on LCD, LCD driving ratio and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

*In mode 0 the partial display ratio could be set from 16 ~ 128.*

*In mode 1 could be set from 16 ~ 100.*

If the partial display region is out of the Max. Display range, it would be no operation.

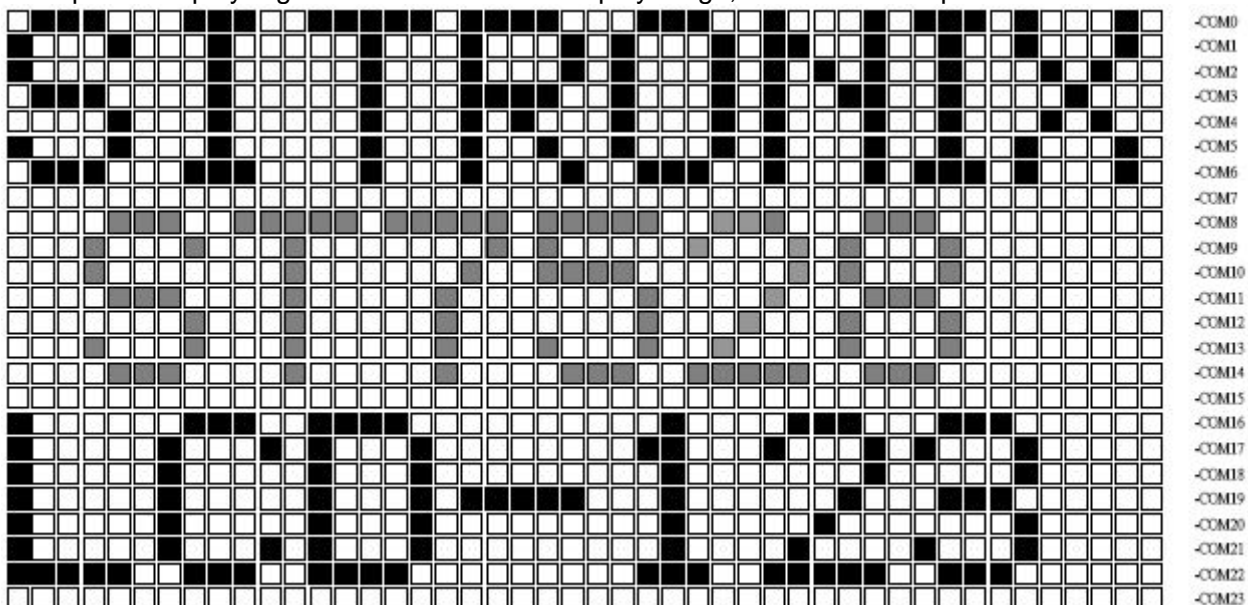


Figure 13 Reference Example for Partial Display

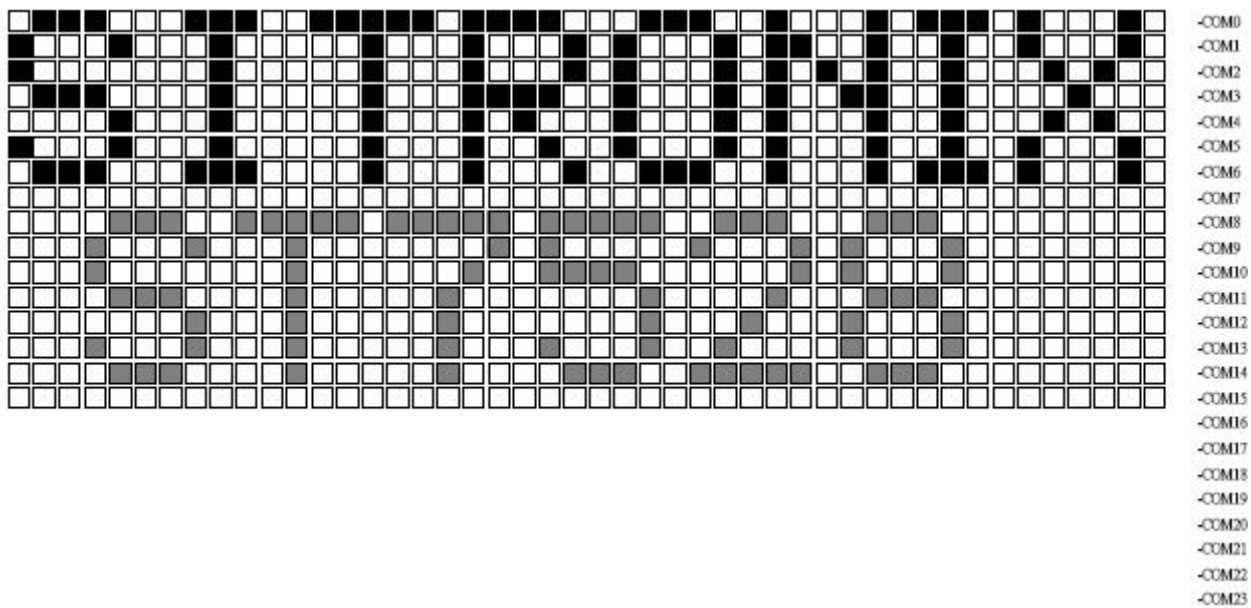


Figure 14 Partial Display (Partial Display ratio=16,initial COM0=0)

## POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control instruction. For details, refers to "Instruction Description". Table 4 shows the referenced combinations in using Power Supply circuits.

Table 4 Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT_IN	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Internal	Without capacitor	With capacitor
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Without capacitor	With capacitor
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	OPEN	External input	With capacitor
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	OPEN	External input	External input

### Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

**Note: we would like to recommend to use the external VOUT when the panel is large than 1.8 inch**

### Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of  $|V0| < |VOUT|$ . Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 16, it is necessary to be applied internally or externally. For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter a is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25°C is shown in Table 5.

$$V_0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV} [V] \text{ ----- (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{210}{(63 - \alpha)}\right) \times V_{REF} [V] \text{ ----- (Eq. 2)}$$

**Table 5 VREF Voltage at Ta = 25° C**

REF	Temp. coefficient	VREF [ V ]
1	-0.125% / °C	2.1
0	External input	VEXT

**In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")**

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

**Table 6 Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)**

	3-bit data settings (R2 R1 R0)							
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
1 + (Rb / Ra)	2.3	3.0	3.7	4.4	5.1	5.8	6.5	7.2

**RESET CIRCUIT**

Setting RESETB to "L" or Reset instruction can initialize internal function.

When RESETB becomes "L", following procedure is occurred.

Page address: 0

Column address: 0

Read-modify-write: OFF

Display ON / OFF: OFF

Initial display line: 0 (first)

Initial COM0 register: 0 (COM0)

Partial display ratio: 1/128

Reverse display ON / OFF: OFF (normal)

N-line inversion register: 0 (disable)

Entire Display ON/OFF: OFF

ICON Control register ON/OFF: OFF (ICON disable)

Power control register (VC, VR, VF) = (0, 0, 0)

DC-DC converter circuit = (0, 0)

Booster Efficiency BE = (1)

Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)

Contrast Level: 32

LCD bias ratio: 1/12

COM Scan Direction: 0

ADC Select: 0

Oscillator: OFF

Power Save Mode: Release

Display Data Length register: 0 (for SPI mode)

All Gray Level Set : OFF

In Level0, 2, 4, 6, 8, 10, 12, 14, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)

All Gray Level Set : OFF

In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)

FRC, PWM mode: 4FRC, 45PWM

When RESET instruction is issued, following procedure is occurred.

Page address: 0



Column address: 0  
Read-modify-write: OFF  
Initial display line: 0 (First)  
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)  
Contrast Level: 32  
Display Data Length register: 0 (for SPI mode)  
All Gray Level Set : OFF  
In Level0, 2, 4, 6, 8, 10, 12, 14 , the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (0,0,0,0,0)  
All Gray Level Set : OFF  
In Level1, 3, 5, 7, 9, 11, 13, 15, the Gray Level palette register (GA5, GA4, GA3, GA2, GA1, GA0) = (1,1,1,1,1)  
FRC, PWM mode: 4FRC, 45PWM  
While RESETB is "L" or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

## 10. Table of LCM commands

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
<b>EXT=0 or 1</b>											
Mode Set	0	0	0	0	1	1	1	0	0	0	2-byte instruction to set Mode and FR( Frame frequency control) BE( Booster efficiency control)
	0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT	
<b>EXT=0</b>											
Read display data	1	1	Read data								Read data into DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0	Read the internal status
ICON control register ON/OFF	0	0	1	0	1	0	0	0	1	ICON	ICON=0: ICON disable(default) ICON=1: ICON enable & set the page address to 16
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y9	Y8	Y7	Y6	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y5	Y4	Y3	Y2	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=0: Display OFF D=1: Display ON
Set initial display line register	0	0	0	1	0	0	0	0	x'	x'	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	x'	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	x'	x'	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	x'	C6	C5	C4	C3	C2	C1	C0	
Select partial display line	0	0	0	1	0	0	1	0	x'	x'	2-byte instruction to set partial display ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	x'	x'	2-byte instruction to set N-line inversion register
	0	0	x'	x'	x'	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line inversion mode
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV	REV=0: normal display REV=1: reverse display
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON	EON=0: normal display EON=1: entire display ON

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
<b>Ext=0</b>											
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of internal voltage converter
Select regulator register	0	0	0	0	1	0	0	R2	R1	R0	Select the internal resistance ratio of the regulator resistor
Select electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the reference voltage
	0	0	x'	x'	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
Set Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save Save the Bias current consumption
	0	0	0	0	0	0	0	0	0	0	
Release Bias Power Save Mode	0	0	1	1	1	1	0	0	1	1	Bias Power save release set the Bias power to normal
	0	0	0	0	0	0	0	1	0	0	
SHL select	0	0	1	1	0	0	SHL	x'	x'	x'	COM bi-directional selection SHL=0: normal direction SHL=1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0: normal direction ADC=1: reverse direction
Oscillator on start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P=0: normal mode P=1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	initial the internal function
Set data direction & display data length(DDL)	x'	x'	1	1	1	0	1	0	0	0	2-byte instruction to specify the number of data bytes. (SPI mode)
	x'	x'	D7	D6	D5	D4	D3	D2	D1	D0	
Select FRC and PWM mode	0	0	1	0	0	1	0	FRC	PWM1	PWM0	FRC(1:3FRC, 0:4FRC) PWM1 PWM0 0 0 45PWM 0 1 45 PWM 1 0 60PWM 1 1 ---
NOP	0	0	1	1	1	0	0	0	1	1	<i>No operation</i>
Test Instruction	0	0	1	1	1	1	x'	x'	x'	x'	<i>Don't use this instruction</i>

Instruction	A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
<b>EXT=1</b>											
Set white mode and 1 <sup>st</sup> frame, set pulse width	0	0	1	0	0	0	0	0	0	0	Set white mode and 1st frame
	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 2 <sup>nd</sup> frame, set pulse width	0	0	1	0	0	0	0	0	0	1	Set white mode and 2nd frame
	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 3 <sup>rd</sup> frame, set pulse width	0	0	1	0	0	0	0	0	1	0	Set white mode and 3rd frame
	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set white mode and 4 <sup>th</sup> frame, set pulse width	0	0	1	0	0	0	0	0	1	1	Set white mode and 4th frame
	0	0	X'	X'	GA05	GA04	GA03	GA02	GA01	GA00	
Set gray level 1 mode	0	0	84H~87H (4 bytes)								Set gray level1
Set gray level 2 mode	0	0	88H~8BH (4 bytes)								Set gray level2
Set gray level 3 mode	0	0	8CH~8FH (4bytes)								Set gray level3
Set gray level 4 mode	0	0	90H~93H (4bytes)								Set gray level4
Set gray level 5 mode	0	0	94H~97H (4bytes)								Set gray level5
Set gray level 6 mode	0	0	98H~9BH (4 bytes)								Set gray level6
Set gray level 7 mode	0	0	9CH~9FH (4 bytes)								Set gray level7
Set gray level 8 mode	0	0	A0H~A3H (4 bytes)								Set gray level8
Set gray level 9 mode	0	0	A4H~A7H (4 bytes)								Set gray level9
Set gray level 10 mode	0	0	A8H~ABH (4 bytes)								Set gray level10
Set gray level 11mode	0	0	ACH~AFH (4 bytes)								Set gray level11
Set gray level 12 mode	0	0	B0H~B3H (4 bytes)								Set gray level12
Set gray level 13 mode	0	0	B4H~B7H (4 bytes)								Set gray level13
Set gray level 14 mode	0	0	B8H~BBH (4 bytes)								Set gray level14
Set Dark mode and 1st frame, set pulse width	0	0	1	0	1	1	1	1	0	0	Set Dark mode and 1st frame, set pulse width
	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 2nd frame, set pulse width	0	0	1	0	1	1	1	1	0	1	Set Dark mode and 2nd frame, set pulse width
	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 3rd frame, set pulse width	0	0	1	0	1	1	1	1	1	0	Set Dark mode and 3rd frame, set pulse width
	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	
Set Dark mode and 4th frame, set pulse width	0	0	1	0	1	1	1	1	1	1	Set Dark mode and 4th frame, set pulse width
	0	0	X'	X'	GAF5	GAF4	GAF3	GAF2	GAF1	GAF0	

### Set Mode Register

2-byte instruction to set Mode (EXT) and FR (Frame frequency control), BE (Booster efficiency control).

#### The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

#### The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	FR3	FR2	FR1	FR0	0	BE	x'	EXT

### Frame frequency

This command is used to set the frame frequency. This table is suitable for no partial display

FR3	FR2	FR1	FR0	FR frequency
0	0	0	0	77 Hz $\pm 5\%$
0	0	0	1	51 Hz $\pm 20\%$
0	0	1	0	55 Hz $\pm 20\%$
0	0	1	1	58 Hz $\pm 20\%$
0	1	0	0	63 Hz $\pm 20\%$
0	1	0	1	67 Hz $\pm 20\%$
0	1	1	0	68 Hz $\pm 20\%$
0	1	1	1	70 Hz $\pm 20\%$
1	0	0	0	73 Hz $\pm 20\%$
1	0	0	1	75 Hz $\pm 20\%$
1	0	1	0	80 Hz $\pm 20\%$
1	0	1	1	85 Hz $\pm 20\%$
1	1	0	0	91 Hz $\pm 20\%$
1	1	0	1	102 Hz $\pm 20\%$
1	1	1	0	113 Hz $\pm 20\%$
1	1	1	1	123 Hz $\pm 20\%$

### Booster Efficiency

The ST7528 incorporates software configurable Booster Efficiency Command. It could be used with Voltage multiplier to get the suitable Vout and Power consumption. Default setting is Level 2

Flag	Description	
BE	0	Booster Efficiency Level 1
	1	Booster Efficiency Level 2

### Mode Set

Flag	Description	
EXT	Default	EXT=0
	EXT=0	The Instruction of EXT=0 Mode is available
	EXT=1	The Instruction of EXT=1 Mode is available

### Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

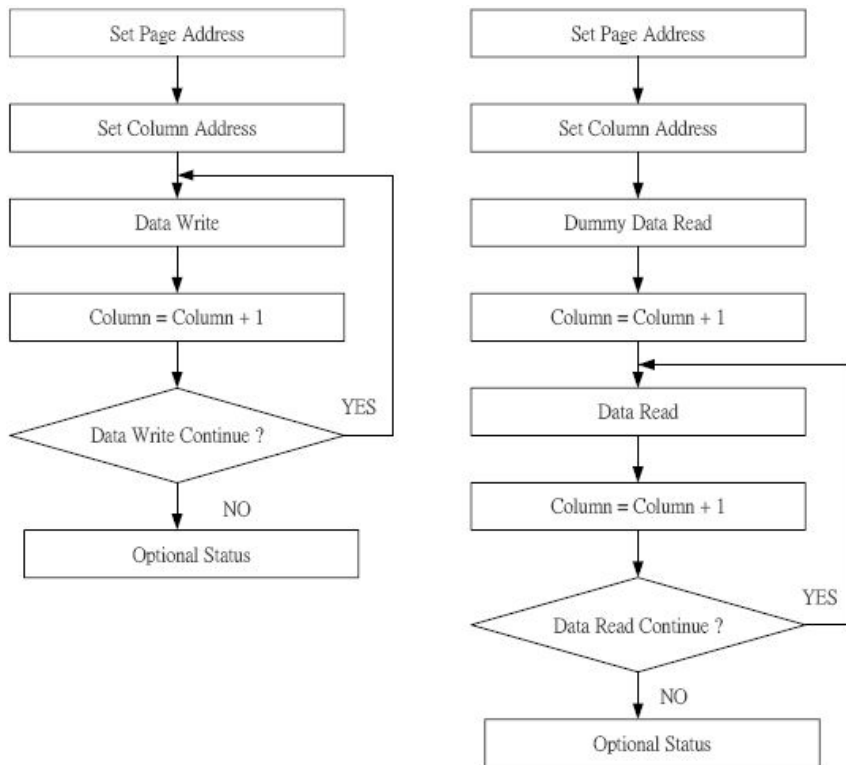
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

### Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor

can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Write data							



**Figure 18 Sequence for Writing Display Data (Left) and Sequence for Reading Display Data (Right) Read Status**

Indicates the internal status of the ST7528

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ON	RES	MF2	MF1	MF0	DS1	DS0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy
ON	Indicates display ON / OFF status 0: display OFF, 1: display ON
RESET	Indicates the initialization is in progress by RESET signal. 0: chip is active, 1: chip is being reset
MF	Manufacturer ID; suggest value: MF2 MF1 MF0 = [0 0 0] The value of MF2, MF1 and MF0 will follow the hardware selection.
DS	Display size ID; suggest value: DS1 DS0 = [1 0] The value of DS1 and DS2 will follow the hardware selection.

### Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. Set Page Address instruction can not be used to set the page address to "16". Use ICON control register ON/OFF instruction to set the page address to "16".

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	1	1	0	14
1	1	1	1	15

### Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

### Set Column Address MSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y9	Y8	Y7	Y6

### Set Column Address LSB

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y5	Y4	Y3	Y2

Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Column address[Y9:Y2]
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	0	126
0	1	1	1	1	1	1	1	127
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159

### Set Modify-Read

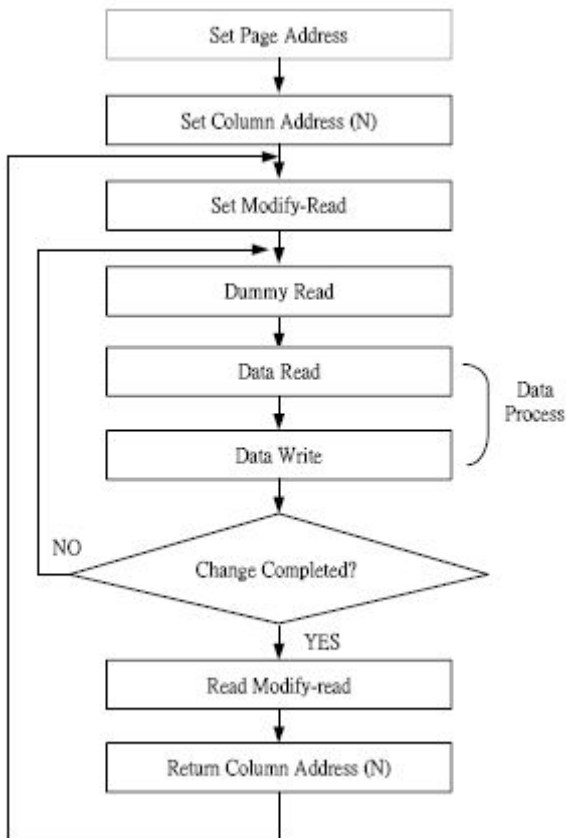
This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-Read instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

### Reset Modify-Read

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Modify-Read instruction is started.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0



**Figure 19 Sequence for Cursor Display**

### Display ON / OFF

Turns the display ON or OFF.

This command has priority over Entire Display On/Off and Reverse Display On/Off. Commands are accepted while the display is off, but the visual state of the display does not change.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON

DON = 0: display OFF

### Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

#### The 1st Instruction

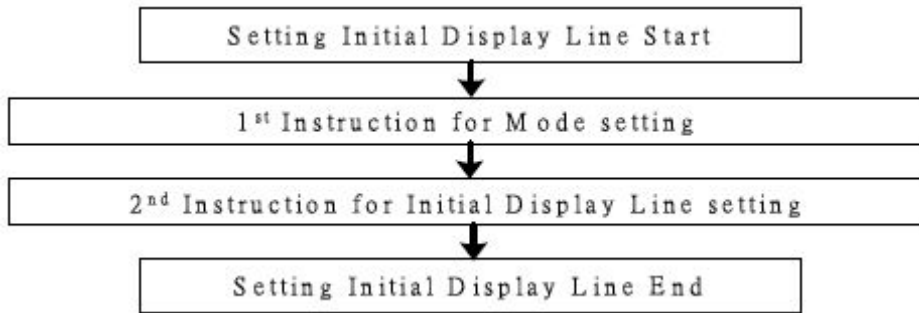
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	x	x

#### The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	125
							126
1	1	1	1	1	1	1	127





**Figure 20 Sequence For Setting Initial Display Line**

### Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

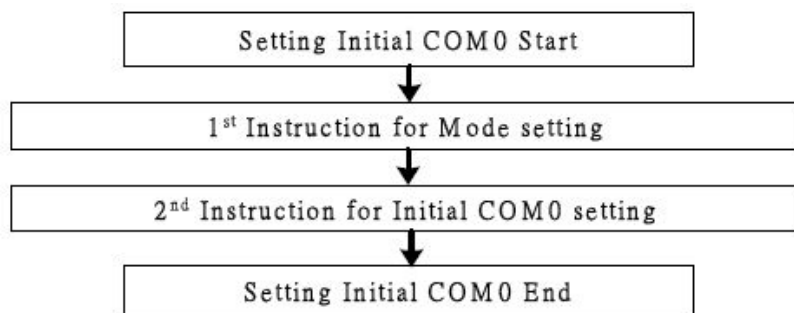
#### The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	x	x

#### The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
0	0	0	0	0	1	1	COM3
:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	COM124
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127



**Figure 21 Sequence For Setting Initial COM**

### Select partial display line

Sets the ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

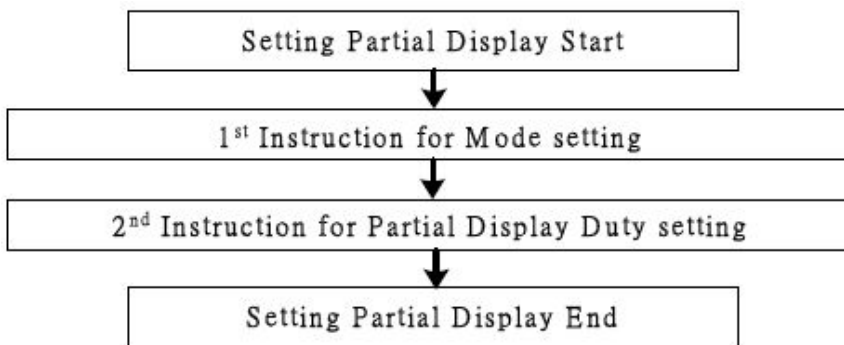
#### The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	x	x

**The 2nd Instruction**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial Display line mode 0	Selected partial Display line mode 1
0	0	0	0	0	0	0	0	No operation	No operation
:	:	:	:	:	:	:	:		
0	0	0	0	1	1	1	1		
0	0	0	1	0	0	0	0	1/16	1/16
0	0	0	1	0	0	0	1	1/17	1/17
:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	1	0	0	1/100	1/100
:	:	:	:	:	:	:	:	:	1/100
0	1	1	1	1	1	1	1	1/127	1/100
1	0	0	0	0	0	0	0	1/128	1/100
1	0	0	0	0	0	0	1	No Operation	No Operation
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	1		


**Figure 22 Sequence For Setting Partial Display**
**Set N-line Inversion Register**

Sets the inverted line number within range of 3 to 33 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction. The DC-bias problem could be occurred if K is even number. So, we recommend customers to set K to be odd number. K :

D/N

D : The number of display ratio (D is selectable by customers)

N : N for N-line inversion (N is selectable by customers).

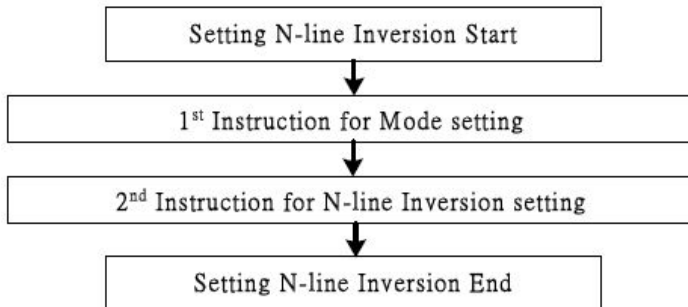
**The 1st Instruction**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	x	x

**The 2st Instruction**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	x	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	3-line inversion
0	0	0	1	0	4-line inversion
0	0	0	1	1	5-line inversion
:	:	:	:	:	:
1	1	1	0	1	31-line inversion
1	1	1	1	0	32-line inversion
1	1	1	1	1	33-line inversion



**Figure 23 Sequence For N-line Inversion**

### Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

### Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	White	Gray level 1	.....	Gray level 14	- Dark
0 (normal)	White ("0000")	Gray 1 ("0001")	.....	Gray 14 ("1110")	Dark ("1111")
1 (reverse)	Dark ("1111")	Gray 14 ("1110")	.....	Gray 1 ("0001")	White ("0000")

### Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

Entire	White	Gray level 1	.....	Gray level 14	- Dark
0 (normal)	White ("0000")	Gray 1 ("0001")	.....	Gray 14 ("1110")	Dark ("1111")
1 (Entire)	Dark ("1111")	Dark ("1111")	Dark ("1111")	Dark ("1111")	Dark ("1111")

### Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

### Set Bias Power Save Mode

Consist of 2-byte Instructions

#### The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

#### The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

This command is for saving the IC current consumption by Bias Power Saving  
 After this Instruction is set, Bias function is also working

### Release Bias Power Save Mode

Consist of 2-byte Instructions

#### The 1st Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1

#### The 2nd Instruction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	0	0

This command is for release Bias Power Save

### Select DC-DC Step-up

Selects one of 4 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

### Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the Table 6.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+ (Rb / Ra)
0	0	0	2.3
0	0	1	3.0
0	1	0	3.7
0	1	1	4.4
1	0	0	5.1
1	0	1	5.8
1	1	0	6.5
1	1	1	7.2

### Set Electronic Volume Register

Consist of 2-byte Instructions

The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, Reference Voltage mode is released.

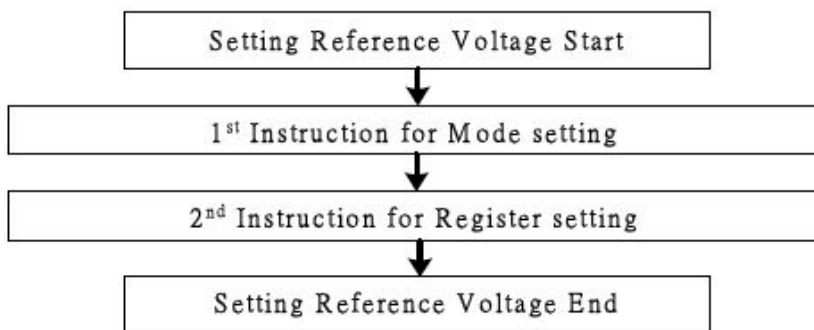
**The 1st Instruction: Set Reference Voltage Select Mode**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

**The 2nd Instruction: Set Reference Voltage Register**

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	x	x	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63


**Figure 24 Sequence For Setting the Electronic Volume**
**Select LCD Bias**

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

**SHL Select**

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	x	x	x

In Mode 0

SHL = 0: normal direction (COM0 -&gt; COM127)      SHL = 1: reverse direction (COM127-&gt; COM0)

In Mode 1

SHL = 0: normal direction (COM0 -&gt; COM99)      SHL = 1: reverse direction (COM99 -&gt; COM0)

### ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

In Mode 0

ADC = 0: normal direction (SEG0 -> SEG127)    ADC = 1: reverse direction (SEG127 -> SEG0)

In Mode 1

ADC = 0: normal direction (SEG0-> SEG159)    ADC = 1: reverse direction (SEG159 -> SEG)

### Oscillator ON Start

This instruction enables the built-in oscillator circuit.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

### Power Save

The ST7528 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

#### Set Power Save Mode

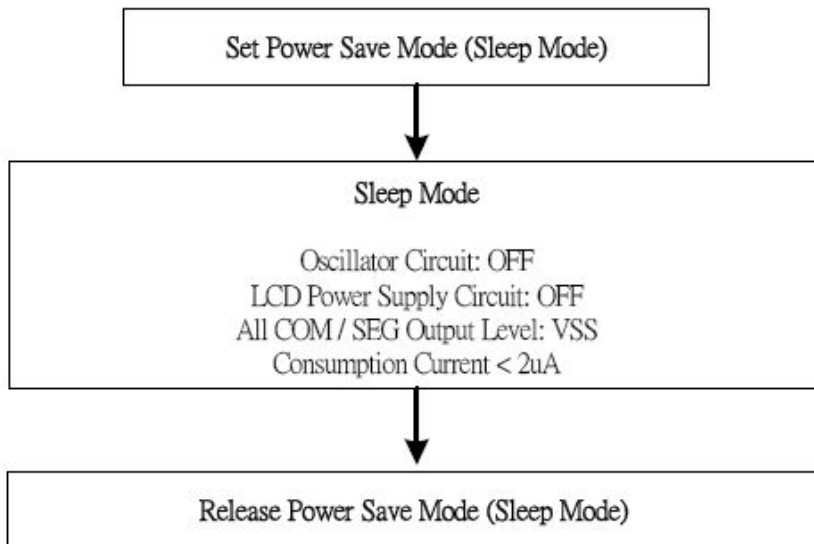
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: normal mode

P = 1: sleep mode

#### Release Power Save Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1



**Figure 25 Power Save Routine**

### Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

### Set Data Direction & Display Data Length (3-Line SPI Mode)

Consists of 2 bytes instruction.

This command is used in 3-Line SPI mode only (PS0 = "L" and PS1 = "L" ). It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

#### The 1st Instruction: Set Data Direction (Only Write Mode)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	1	1	1	0	1	0	0	0

#### The 2nd Instruction: Set Display Data Length (DDL) Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
x	x	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

### NOP

No operation

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

### Test Instruction

This instruction is for testing IC. Please do not use it.

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	x	x	x	x

### Set FRC & PWM mode

Selects 3/4 FRC and 45 / 60 PWM

FRC	PWM1	PWM0	Status of PWM & FRC
0			4FRC
1			3FRC
	0	0	45PWM
	0	1	45PWM
	1	0	60PWM
	1	1	---

**NOTE: the value of register could not set [PWM1:PWM0]=[1:1]**

### Set Gray Scale Mode & Register

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

#### - Set Gray Scale Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0

GRAY3	GRAY2	GRAY1	GRAY0	FRAMX1	FRAMX0	Description
0	0	0	0	0	0	In case of setting whit mode and 1 <sup>st</sup> frame
0	0	0	0	0	1	In case of setting whit mode and 2 <sup>nd</sup> frame
0	0	0	0	1	0	In case of setting whit mode and 3 <sup>rd</sup> frame
0	0	0	0	1	1	In case of setting whit mode and 4 <sup>th</sup> frame
0	0	0	1	0	0	In case of setting GRAY LEVEL 1 mode and 1 <sup>st</sup> frame
0	0	0	1	0	1	In case of setting GRAY LEVEL 1 mode and 2 <sup>nd</sup> frame
0	0	0	1	1	0	In case of setting GRAY LEVEL 1 mode and 3 <sup>rd</sup> frame
:	:	:	:	:	:	:
1	1	1	0	0	1	In case of setting GRAY LEVEL 14 mode and 2 <sup>nd</sup> frame
1	1	1	0	1	0	In case of setting GRAY LEVEL 14 mode and 3 <sup>rd</sup> frame
1	1	1	0	1	1	In case of setting GRAY LEVEL 14 mode and 4 <sup>th</sup> frame
1	1	1	1	0	0	In case of setting dark mode and 1 <sup>st</sup> frame
1	1	1	1	0	1	In case of setting dark mode and 2 <sup>nd</sup> frame
1	1	1	1	1	0	In case of setting dark mode and 3 <sup>rd</sup> frame
1	1	1	1	1	1	In case of setting dark mode and 4 <sup>th</sup> frame

#### Set Gray Scale Register

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	GAX5	GAX4	GAX3	GAX2	GAX1	GAX0

GAX5	GAX4	GAX3	GAX2	GAX1	GAX0	Pulse width (45 PWM)	Pulse width (60 PWM)
0	0	0	0	0	0	0/45	0/60
0	0	0	0	0	1	1/45	1/60
0	0	0	0	1	0	2/45	2/60
0	0	0	0	1	1	3/45	3/60
0	0	0	1	0	0	4/45	4/60
:	:	:	:	:	:	:	:
1	0	1	0	1	1	43/45	43/60
1	0	1	1	0	0	44/45	44/60
1	0	1	1	0	1	45/45	45/60
1	0	1	1	1	0	0/45	46/60
1	0	1	1	1	1	0/45	47/60
:	:	:	:	:	:	:	:
1	1	1	0	1	1	0/45	59/60
1	1	1	1	0	0	0/45	60/60
1	1	1	1	0	1	0/45	0/60
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0/45	0/60



## COMMAND DESCRIPTION

### Referential Instruction Setup Flow: Initializing with the built-in Power Supply Circuits

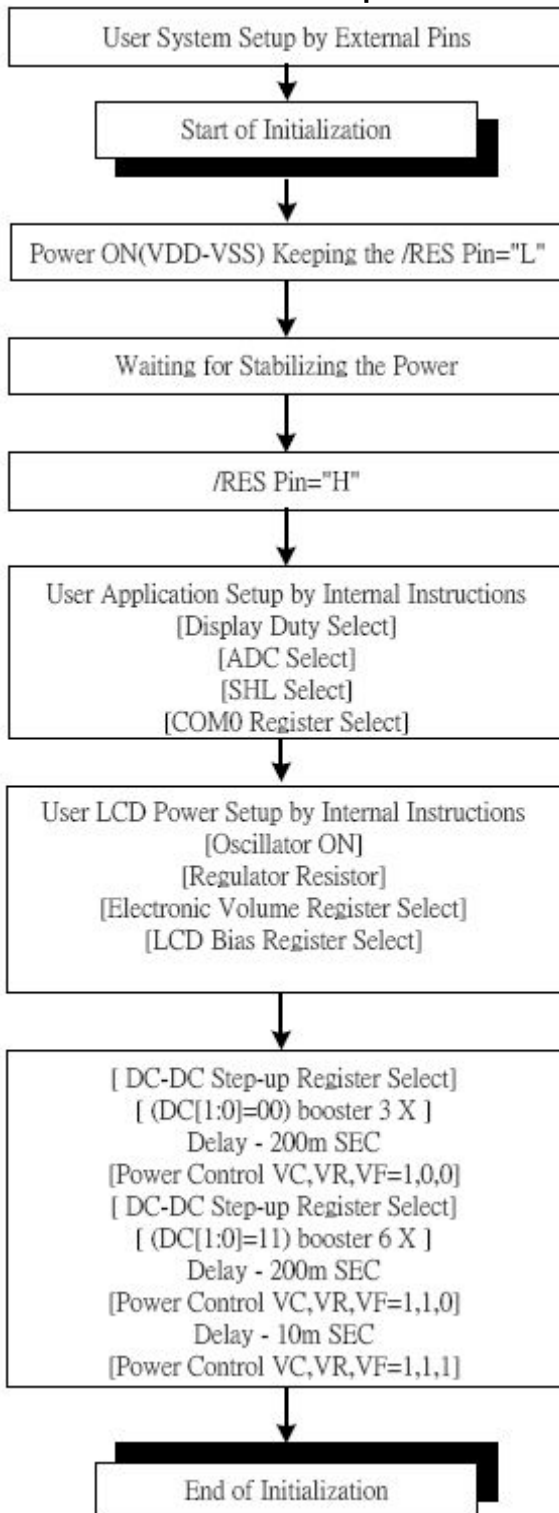


Figure 26 Initializing with the Built-in Power Supply Circuits

### Referential Instruction Setup Flow: Initializing without the built-in Power Supply Circuits

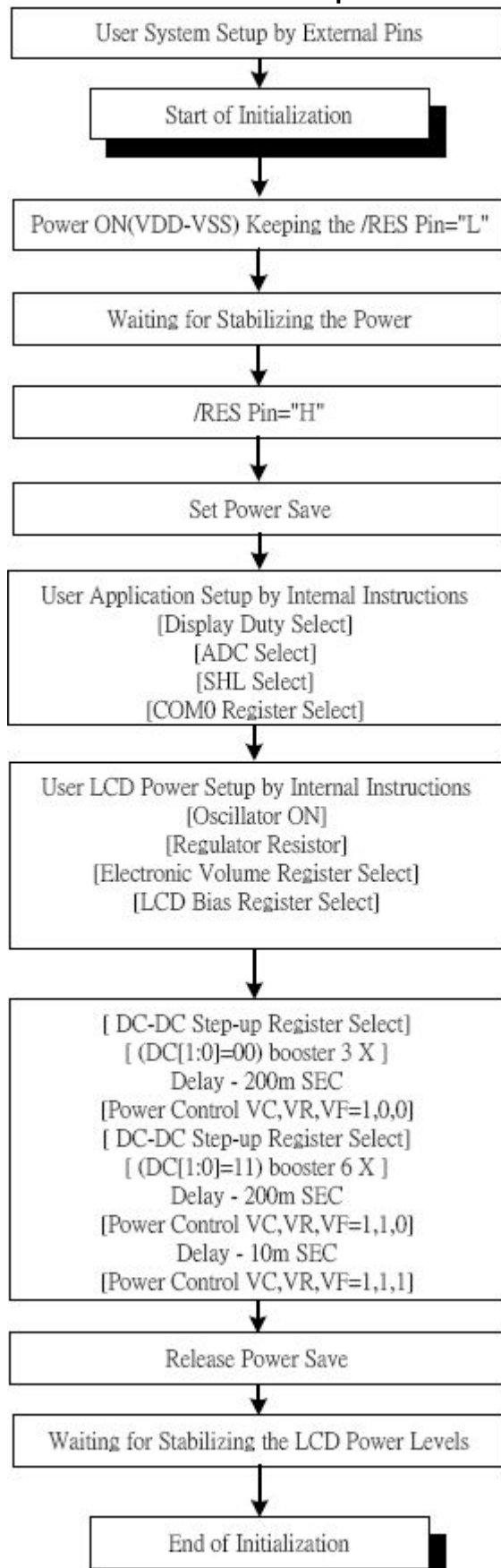
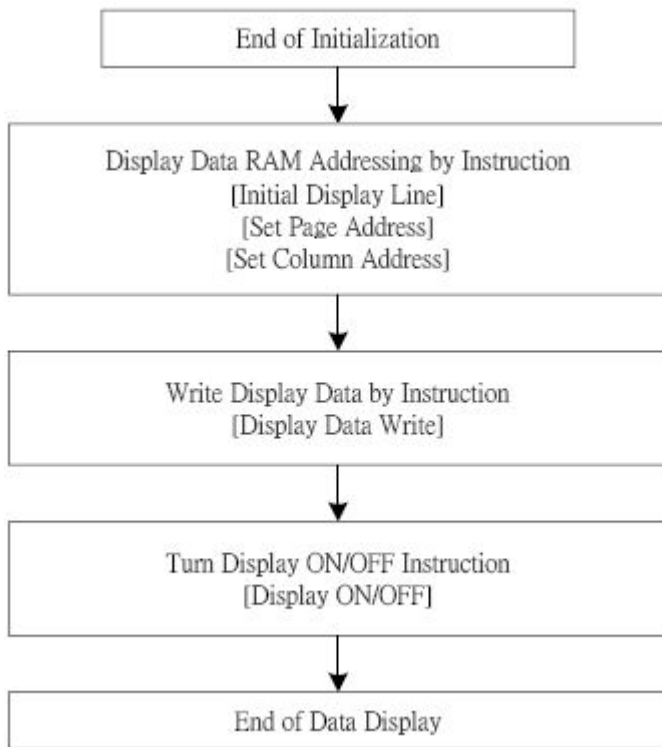


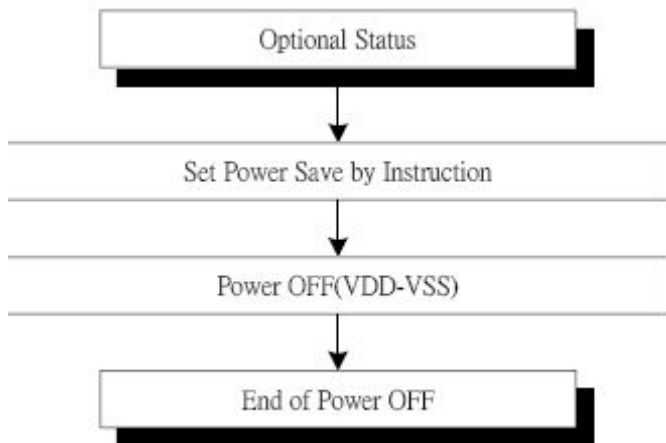
Figure 27 Initializing without Built-in Power Supply Circuits

**Referential Instruction Setup Flow: Data Displaying**



**Figure 28 Data Displaying**

**Referential Instruction Setup Flow: Power OFF**



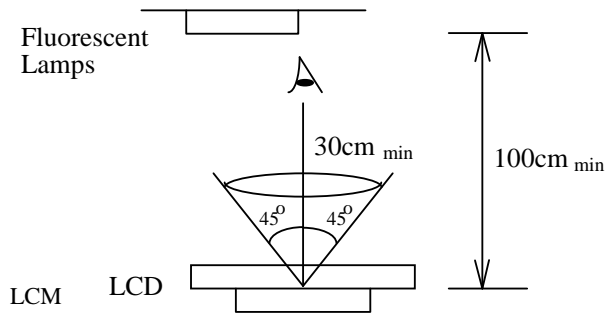
**Figure 29 Power OFF**

## 11.QUALITY SPECIFICATIONS

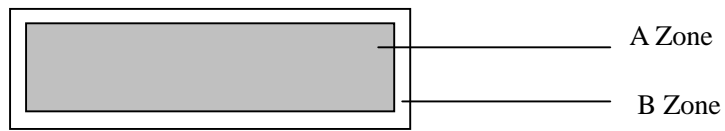
### 11.1 Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps.  
Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).

B Zone: Non-active display area (outside viewing area).

## 11.2 Specification of quality assurance

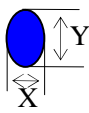
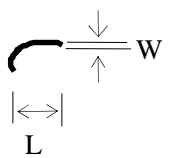
AQL inspection standard

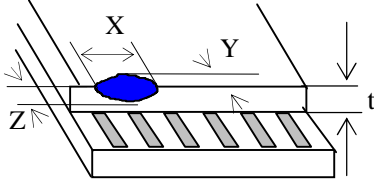
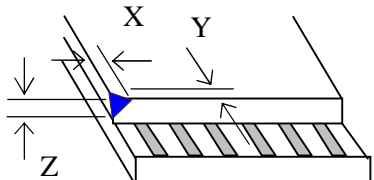
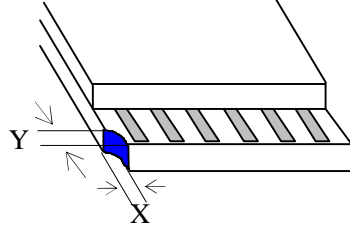
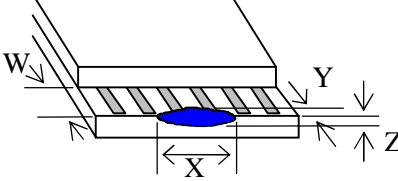
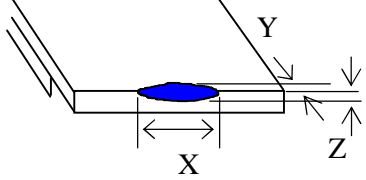
Sampling method: MIL-STD-105E, Level II, single sampling

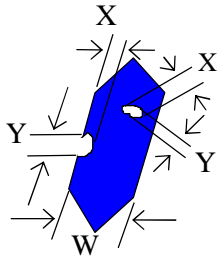
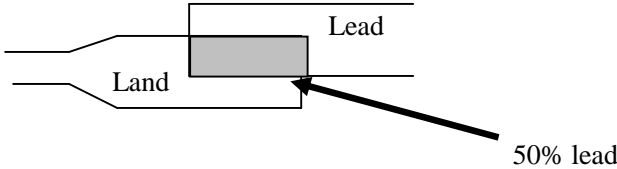
Defect classification **(Note: \* is not including)**

Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
Wrong or missing component		11		
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

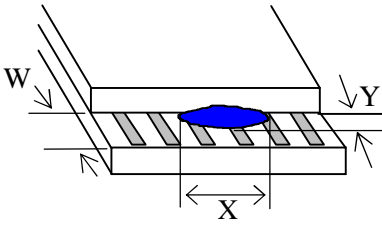
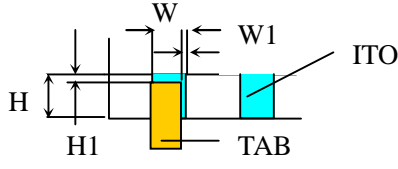
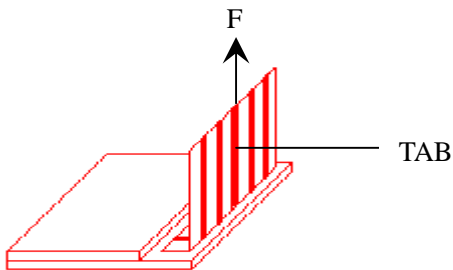
**Note on defect classification**

No.	Item	Criterion																				
1	Short or open circuit	Not allow																				
	LC leakage																					
	Flickering																					
	No display																					
	Wrong viewing direction																					
	Wrong Back-light																					
2	Contrast defect	Refer to approval sample																				
	Background color deviation																					
3	Point defect, Black spot, dust (including Polarizer)  $\phi = (X+Y)/2$	 <table border="1" data-bbox="861 996 1300 1299"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty.</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 0.10</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.10 &lt; \phi \leq 0.20</math></td> <td>3</td> </tr> <tr> <td><math>0.20 &lt; \phi \leq 0.25</math></td> <td>2</td> </tr> <tr> <td><math>0.25 &lt; \phi \leq 0.30</math></td> <td>1</td> </tr> <tr> <td><math>\phi &gt; 0.30</math></td> <td>0</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Point Size	Acceptable Qty.	$\phi \leq 0.10$	Disregard	$0.10 < \phi \leq 0.20$	3	$0.20 < \phi \leq 0.25$	2	$0.25 < \phi \leq 0.30$	1	$\phi > 0.30$	0								
Point Size	Acceptable Qty.																					
$\phi \leq 0.10$	Disregard																					
$0.10 < \phi \leq 0.20$	3																					
$0.20 < \phi \leq 0.25$	2																					
$0.25 < \phi \leq 0.30$	1																					
$\phi > 0.30$	0																					
4	Line defect, Scratch	 <table border="1" data-bbox="790 1433 1340 1691"> <thead> <tr> <th colspan="2">Line</th> <th>Acceptable Qty.</th> </tr> <tr> <th>L</th> <th>W</th> <th></th> </tr> </thead> <tbody> <tr> <td>---</td> <td><math>0.015 \geq W</math></td> <td>Disregard</td> </tr> <tr> <td><math>3.0 \geq L</math></td> <td><math>0.03 \geq W</math></td> <td rowspan="2">2</td> </tr> <tr> <td><math>2.0 \geq L</math></td> <td><math>0.05 \geq W</math></td> </tr> <tr> <td><math>1.0 \geq L</math></td> <td><math>0.1 &gt; W</math></td> <td>1</td> </tr> <tr> <td>---</td> <td><math>0.05 &lt; W</math></td> <td>Applied as point defect</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Line		Acceptable Qty.	L	W		---	$0.015 \geq W$	Disregard	$3.0 \geq L$	$0.03 \geq W$	2	$2.0 \geq L$	$0.05 \geq W$	$1.0 \geq L$	$0.1 > W$	1	---	$0.05 < W$	Applied as point defect
Line		Acceptable Qty.																				
L	W																					
---	$0.015 \geq W$	Disregard																				
$3.0 \geq L$	$0.03 \geq W$	2																				
$2.0 \geq L$	$0.05 \geq W$																					
$1.0 \geq L$	$0.1 > W$	1																				
---	$0.05 < W$	Applied as point defect																				
5	Rainbow	Not more than two color changes across the viewing area.																				

No	Item	Criterion																																	
6	Chip  Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width	 <p>Acceptable criterion</p> <table border="1" data-bbox="933 414 1324 492"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td><math>\leq 2</math></td> <td>0.5mm</td> <td><math>\leq t/2</math></td> </tr> </tbody> </table>  <p>Acceptable criterion</p> <table border="1" data-bbox="917 728 1324 806"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td><math>\leq 2</math></td> <td>0.5mm</td> <td><math>\leq t</math></td> </tr> </tbody> </table>  <p>Acceptable criterion</p> <table border="1" data-bbox="933 1019 1324 1131"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td><math>\leq 3</math></td> <td><math>\leq 2</math></td> <td><math>\leq t</math></td> </tr> <tr> <td colspan="2">shall not reach to ITO</td> <td></td> </tr> </tbody> </table>  <p>Acceptable criterion</p> <table border="1" data-bbox="917 1400 1324 1478"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>Disregard</td> <td><math>\leq 0.2</math></td> <td><math>\leq t</math></td> </tr> </tbody> </table>  <p>Acceptable criterion</p> <table border="1" data-bbox="917 1680 1292 1758"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td><math>\leq 5</math></td> <td><math>\leq 2</math></td> <td><math>\leq t/3</math></td> </tr> </tbody> </table>	X	Y	Z	$\leq 2$	0.5mm	$\leq t/2$	X	Y	Z	$\leq 2$	0.5mm	$\leq t$	X	Y	Z	$\leq 3$	$\leq 2$	$\leq t$	shall not reach to ITO			X	Y	Z	Disregard	$\leq 0.2$	$\leq t$	X	Y	Z	$\leq 5$	$\leq 2$	$\leq t/3$
X	Y	Z																																	
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Disregard	$\leq 0.2$	$\leq t$																																	
X	Y	Z																																	
$\leq 5$	$\leq 2$	$\leq t/3$																																	

No.	Item	Criterion								
7	Segment pattern $W = \text{Segment width}$ $\phi = (X+Y)/2$	(1) Pin hole $\phi < 0.10\text{mm}$ is acceptable.  <table border="1" data-bbox="853 564 1316 734"> <thead> <tr> <th>Point Size</th> <th>Acceptable Qty</th> </tr> </thead> <tbody> <tr> <td><math>\phi \leq 1/4W</math></td> <td>Disregard</td> </tr> <tr> <td><math>1/4W &lt; \phi \leq 1/2W</math></td> <td>1</td> </tr> <tr> <td><math>\phi &gt; 1/2W</math></td> <td>0</td> </tr> </tbody> </table> <p style="text-align: right;">Unit: mm</p>	Point Size	Acceptable Qty	$\phi \leq 1/4W$	Disregard	$1/4W < \phi \leq 1/2W$	1	$\phi > 1/2W$	0
Point Size	Acceptable Qty									
$\phi \leq 1/4W$	Disregard									
$1/4W < \phi \leq 1/2W$	1									
$\phi > 1/2W$	0									
8	Back-light	(1) The color of backlight should correspond its specification. (2) Not allow flickering								
9	Soldering	(1) Not allow heavy dirty and solder ball on PCB. (The size of dirty refer to point and dust defect) (2) Over 50% of lead should be soldered on Land. 								
10	Wire	(1) Copper wire should not be rusted (2) Not allow crack on copper wire connection. (3) Not allow reversing the position of the flat cable. (4) Not allow exposed copper wire inside the flat cable.								
11*	PCB	(1) Not allow screw rust or damage. (2) Not allow missing or wrong putting of component.								



No	Item	Criterion
12	Protruded W: Terminal Width	 <p>Acceptable criteria: <math>Y \leq 0.4</math></p>
13	TAB	<p>1. Position</p>  <div style="border: 1px solid black; padding: 5px; width: fit-content; margin-left: auto;"> <math>W1 \leq 1/3W</math>  <math>H1 \leq 1/3H</math> </div> <p>2. TAB bonding strength test</p>  <p><math>P (=F/TAB \text{ bonding width}) \geq 650\text{gf/cm}</math> ,(speed rate: 1mm/min)            5pcs per SOA (shipment)</p>
14	Total no. of acceptable Defect	<p>A. Zone</p> <p>Maximum 2 minor non-conformities per one unit.            Defect distance: each point to be separated over 10mm</p> <p>B. Zone</p> <p>It is acceptable when it is no trouble for quality and assembly in customer's end product.</p>

### 11.3 Reliability of LCM

Reliability test condition:

Item	Condition	Time (hrs)	Assessment
High temp. Storage	80°C	48	No abnormalities in functions and appearance
High temp. Operating	70°C	48	
Low temp. Storage	-30°C	48	
Low temp. Operating	-20°C	48	
Humidity	40°C/ 90%RH	48	
Temp. Cycle	0°C ← 25°C → 50°C (30 min ← 5 min → 30min)	10cycles	

Recovery time should be 24 hours minimum. Moreover, functions, performance and appearance shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (20±8°C), normal humidity (below 65% RH), and in the area not exposed to direct sun light.

### 11.4 Precaution for using LCD/LCM

LCD/LCM is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification. The followings should be noted.

#### General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isopropyl alcohol, ethyl alcohol or trichlorotrifluoroethane, do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting Focus LCDs
5. When mounting a LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and also cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

#### Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and

- the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
  4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
  5. Only properly grounded soldering irons should be used.
  6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
  7. The normal static prevention measures should be observed for work clothes and working benches.
  8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

### **Soldering Precautions:**

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature:  $280^{\circ}\text{C}\pm 10^{\circ}\text{C}$
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

### **Operation Precautions:**

1. The viewing angle can be adjusted by varying the LCD driving voltage  $V_o$ .
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage over  $40^{\circ}\text{C}$  is required, the relative humidity should be kept below 60%, and avoid direct sunlight.