

# USB Type-C Port Controller with Power Delivery

## General Description

CCG1 provides a complete USB Type-C and USB Power Delivery port control solution. The core architecture of CCG1 enables a base Type-C solution that can scale to a complete 100-W USB Power Delivery with Alternate Mode multiplex support. CCG1 is also a Type-C cable ID IC for active and passive cables. The CCG1 controller detects connector insert, plug orientation and VCONN switching signals. CCG1 makes it easier to add USB Power Delivery to any architecture because it provides control signals to manage external VBUS and V<sub>CONN</sub> power management solutions and external mux controls for most single cable-docking solutions.

The CCG1 family of devices are fixed-function parts that use a configuration table to control their operation in different applications. The functionality is implemented in firmware and will be certified against USB Implementers Forum (USB-IF) compliance tests when available. The programmability allows CCG1 devices to track any USB Specification changes. For information on accessing the source code, contact [Cypress support](#).

## Applications

- Notebooks, tablets, monitors, docking stations
- Power adapters, USB Type-C cables

## Features

### 32-bit MCU Subsystem

- 48-MHz ARM Cortex-M0 CPU with 32-KB flash and 4-KB SRAM

### Integrated analog blocks

- 12-bit, 1-Msps ADC for VBUS voltage and current monitoring
- Dynamic overcurrent and overvoltage protection

### Integrated digital blocks

- Two configurable 16-bit TCPWM blocks
- One I<sup>2</sup>C master or slave

## Type-C Support

- Integrated transceiver (BB PHY)
- Supports up to two USB ports with PD
- Supports routing of all protocols through an external mux

## PD Support

- Supports Provider and Consumer roles
- Supports all power profiles

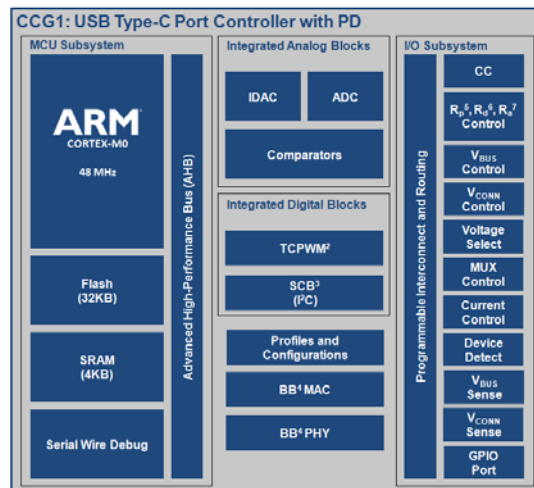
## Low-Power Operation

- 3.2 V to 5.5 V operation
- Sleep 1.3 mA, Deep Sleep 1.3 μA<sup>[1]</sup>

## Packages

- 40-pin QFN
- 16-pin SOIC
- 35-ball wafer-level CSP (WLCSP)

Figure 1. CCG1 Block Diagram<sup>[2, 3, 4, 5, 6, 7]</sup>



### Notes

1. Values measured for CCG1 silicon only. Application specific power numbers may be higher.
2. Timer, counter, pulse-width modulation block.
3. Serial communication block configurable as I<sup>2</sup>C.
4. Base band.
5. Termination resistor denoting a Downstream Facing Port (DFP).
6. Termination resistor denoting an Upstream Facing Port (UFP).
7. Termination resistor denoting an Electronically Marked Cable Assembly (EMCA).

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## Functional Definition

### CPU and Memory Subsystem

#### CPU

The Cortex-M0 CPU in the CCG1 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for CCG1 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

The CCG1 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

#### SRAM

A supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) or interrupts (Low Voltage Detect (LVD)). The CCG1 operates with a single external supply over the range of 3.2 V to 5.5 V operation and has three different power modes: Active, Sleep, and Deep Sleep; transitions between modes are managed by the power system.

#### Serial Communication Blocks (SCB)

The CCG1 has one SCB, which can implement an I<sup>2</sup>C interface. The hardware I<sup>2</sup>C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZ-I<sup>2</sup>C that creates a mailbox address range in the memory of the CCG1 and effectively reduces I<sup>2</sup>C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep

FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I<sup>2</sup>C peripheral is compatible with the I<sup>2</sup>C Standard-mode, Fast-mode, and Fast-mode Plus devices, as defined in the NXP I<sup>2</sup>C-bus specification and user manual (UM10204). The I<sup>2</sup>C bus I/O is implemented with GPIO in open-drain modes.

The CCG1 is not completely compliant with the I<sup>2</sup>C spec in the following respects:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I<sup>2</sup>C system.
- Fast-mode Plus has an I<sub>OL</sub> specification of 20 mA at a V<sub>OL</sub> of 0.4 V. The GPIO cells can sink a maximum of 8 mA I<sub>OL</sub> with a V<sub>OL</sub> maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.
- When the SCB is an I<sup>2</sup>C Master, it interposes an IDLE state between NACK and Repeated Start; the I<sup>2</sup>C spec defines Bus free as following a Stop condition so other Active Masters do not intervene but a Master that has just become activated may start an Arbitration cycle.
- When the SCB is in the I<sup>2</sup>C Slave mode, and Address Match on External Clock is enabled (EC\_AM = 1) along with operation in the internally clocked mode (EC\_OP = 0), then its I<sup>2</sup>C address must be even.

### GPIO

The CCG1 has up to 30 GPIOs, which are configured for various functions. Refer to the pinout tables for the definitions. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control to improve EMI.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network, known as a high-speed I/O matrix, is used to multiplex between various signals that may connect to an I/O pin.

## Pin Definitions

Table 1 provides the pin definition for 35-Ball WLCSP for the Cable/EMCA application. Refer to Table 23 for part numbers to package mapping.

**Table 1. Pin Definitions for 35-ball WLCSP for EMCA Cable Application**

| Functional Pin Name | CYPD1103-35FNXIT Balls                             | Type  | Description  |
|---------------------|--|-------|--|
| CC1_RX              | C4   | I     | CC1 control<br>0: TX enabled<br>z: RX sense  |
| CC1_TX              | D7   | O     | Configuration Channel 1  |
| SWD_IO              | D1   | I/O   | SWD I/O  |
| SWD_CLK             | C1   | I     | SWD clock  |
| I2C_SCL             | B1   | I/O   | I <sup>2</sup> C clock signal  |
| I2C_SDA             | B2   | I/O   | I <sup>2</sup> C data signal   |
| XRES                | B6   | I     | Reset  |
| VCCD                | A7   | POWER | Regulated digital supply output. Connect a 1 to 1.6- $\mu$ F capacitor. No external source should be connected               |
| VDDD                | C7   | POWER | Power supply for both analog and digital sections  |
| VSSA                | B7   | GND   | Analog ground  |
| CC_VREF             | C5   | I     | Data reference signal for CC lines   |
| TX_U                | B3   | O     | Signals for internal use only. The TX_U output signal should be connected to the TX_M signal                                 |
| TX_M                | B5   | I     | –  |
| TX_REF_IN           | D3   | I     | Reference signal for internal use. Connect to TX_REF output via a 2.4K 1% resistor   |
| TX_GND              | A3   | I     | Connect to GND via 2K 1% resistor  |
| TX_REF_OUT          | D4   | O     | Reference signal generated by connecting internal current source to two 1K external resistors                                |
| RA_DISCONNECT       | E4   | O     | Optional control signal to remove RA after assertion of VCONN<br>0: RA disconnected<br>1: RA connected                       |
| VCONN_DET           | C6   | I     | Local VCONN detection signal<br>0: VCONN is not locally applied<br>1: VCONN is locally applied                               |
| CC1_LPREF           | A5   | I     | Reference signal for internal use. Connect to the output of resistor divider from VDDD.                                      |
| RA_FAR_DISCONNECT   | E5   | O     | Optional control signal to remove RA after assertion of VCONN (NC for 2 chip/cable)<br>0: RA disconnected<br>1: RA connected |
| BYPASS              | D5   | I     | Bypass capacitor for internal analog circuits  |
| CC1_LPRX            | C3   | I     | Configuration channel 1 RX signal for Low Power States   |
| GPIO                | A1, A2, A4, A6, B4, C2, D2, D6, E1, E2, E3, E6, E7 | –     | General-purpose I/Os   |

Table 2 provides the pin definitions for 40-pin QFN and 35-ball WLCSP for the notebook, tablet, smartphone, and monitor applications. Refer to Table 23 on page 23 for part numbers to package mapping.

**Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications**

| Functional Pins | CYPD 1122-40LQXI Pins <sup>[8]</sup> | CYPD 1121-40LQXI Pins <sup>[9]</sup> | CYPD 1131-35FNXIT Balls <sup>[10]</sup> | Type | Description  |
|-----------------|--------------------------------------|--------------------------------------|---|------|--|
| MUXSEL_1        | 1                                    | 1                                    | D5                                      | O    | External Data Mux Select signal 1  |
| MUXSEL_2        | 2                                    | 2                                    | D6                                      | O    | External Data Mux Select signal 2  |
| CC1_CTRL        | 3                                    | 3                                    | D3                                      | I/O  | CC1 control<br>0: TX enabled<br>z: RX sense  |
| CC2_CTRL        | 4                                    | 4                                    | E4                                      | I/O  | CC2 control<br>0: TX enabled<br>z: RX sense  |
| MUXSEL_3        | 5                                    | 5                                    | E5                                      | O    | External Data Mux Select signal 3  |
| MUXSEL_4        | 6                                    | 6                                    | E6                                      | O    | External Data Mux Select signal 4  |
| CS_P            | 7                                    | 7                                    | E3                                      | I    | Current Sensing Plus input   |
| CS_M            | 8                                    | 8                                    | E2                                      | I    | Current Sensing Minus input I  |
| VSS             | 9                                    | 9                                    | –                                       | GND  | Ground   |
| CC1             | 10                                   | 10                                   | –                                       | I/O  | Configuration Channel 1  |
| CC_SEL_REF_1    | 11                                   | 11                                   | E1                                      | O    | CC Reference Select signal   |
| SWD_IO          | 12                                   | 12                                   | D1                                      | I/O  | SWD IO   |
| SWD_CLK         | 13                                   | 13                                   | C1                                      | I    | SWD Clock  |
| HOTPLUG_DET     | 14                                   | 14                                   | C2                                      | I/O  | HotPlug Detection for Display Port Alternate Mode  |
| GPIO1           | 15                                   | –                                    | –                                       | I/O  | General-purpose I/O  |
| VSEL2           | –                                    | 15                                   | –                                       | O    | Voltage Select signal 2 for selecting output voltage   |
| GPIO2           | 16                                   | –                                    | –                                       | I/O  | General-purpose I/O  |
| GPIO3           | 17                                   | –                                    | –                                       | I/O  | General-purpose I/O  |
| IFault          | –                                    | 17                                   | –                                       | I    | Current Fault Indication<br>0: No fault<br>1: Current fault  |
| I2C_SCL         | 18                                   | 18                                   | B1                                      | I/O  | I2C Clock signal   |
| I2C_SDA         | 19                                   | 19                                   | B2                                      | I/O  | I2C Data signal  |
| I2C_INT         | 20                                   | 20                                   | A2                                      | O    | I2C Interrupt  |
| CC_SEL_REF_2    | 21                                   | 21                                   | A1                                      | O    | CC Reference Select signal   |
| CC1_RD          | 22                                   | 22                                   | C3                                      | O    | Open Drain signal to connect RD to CC 1 line<br>z: RD not connected<br>0: RD connected for Monitor application<br>1: RD connected for Notebook application |
| CC1_RP          | 23                                   | 23                                   | A5                                      | O    | Open Source signal to connect RP to CC 1 line<br>z: RP not connected<br>1: RP connected  |

**Notes**

- 8. Pinout for Notebook DRP application for 40-QFN.
- 9. Pinout for Monitor DRP application for 40-QFN.
- 10. Pinout for Notebook DRP application for 35-CSP.

**Table 2. Pin Definitions for 40-QFN and 35-ball WLCSP for Notebook, Tablet, SmartPhone and Monitor Applications (continued)**

| Functional Pins | CYPD 1122-40LQXI Pins <sup>[8]</sup> | CYPD 1121-40LQXI Pins <sup>[9]</sup> | CYPD 1131-35FNXIT Balls <sup>[10]</sup> | Type  | Description  |
|-----------------|--------------------------------------|--------------------------------------|---|-------|--|
| CC1_VCONN_CTRL  | 24                                   | 24                                   | A4                                      | O     | Open Drain signal to control a PFET power switch for VCONN on CC 1 line<br>0: VCONN switch closed<br>z: VCONN switch open                                  |
| VBUS_DISCHARGE  | 25                                   | 25                                   | A3                                      | O     | Signal used for discharging VBUS line during voltage change  |
| CC2             | 26                                   | 26                                   | B3                                      | O     | Configuration Channel 2  |
| CC2_RD          | 27                                   | 27                                   | A6                                      | O     | Open Drain signal to connect RD to CC 2 line<br>z: RD not connected<br>0: RD connected for Monitor application<br>1: RD connected for Notebook application |
| CC2_RP          | 28                                   | 28                                   | B4                                      | O     | Open Source signal to connect RP to CC 2 line<br>z: RP not connected<br>1: RP connected  |
| CC2_VCONN_CTRL  | 29                                   | 29                                   | B5                                      | O     | Open Drain signal to control a PFET power switch for VCONN on CC 2 line<br>0: VCONN switch closed<br>z: VCONN switch open                                  |
| XRES            | 30                                   | 30                                   | B6                                      | I     | Reset  |
| VCCD            | 31                                   | 31                                   | A7                                      | POWER | Regulated digital supply output. Connect a 1 to 1.6- $\mu$ F capacitor. No external source should be connected   |
| VDDD            | 32                                   | 32                                   | C7                                      | POWER | Power supply for digital sections  |
| VDDA            | 33                                   | 33                                   | C7                                      | POWER | Power Supply for analog sections   |
| VSSA            | 34                                   | 34                                   | B7                                      | GND   | Analog ground pin  |
| VBUS_VMON       | 35                                   | 35                                   | C4                                      | I     | VBUS Overvoltage Protection monitoring signal  |
| VBUS_VREF       | 36                                   | 36                                   | C5                                      | I     | VBUS reference signal for Overvoltage Protection detection   |
| VSEL1           | –                                    | 37                                   | –                                       | O     | Voltage Select signal 1 for selecting the output voltage   |
| CC_SEL_REF_3    | 37                                   | 16                                   | C6                                      | O     | CC Reference Select signal   |
| VBUS_C_CTRL     | 38                                   | –                                    | D7                                      | O     | Full rail control signal for enabling/disabling Consumer load FET  |
| VBUS_OK         | –                                    | 38                                   | –                                       |       | VBUS_OK=1 - VBUS Voltage ok<br>VBUS_OK=0 - VBUS Overvoltage detected   |
| CC_VREF         | 39                                   | 39                                   | D4                                      | I     | Data reference signal for CC lines   |
| VBUS_P_CTRL     | 40                                   | 40                                   | E7                                      | O     | Full rail control signal for enabling/disabling Provider load FET  |

**Notes**

8. Pinout for Notebook DRP application for 40-QFN.
9. Pinout for Monitor DRP application for 40-QFN.
10. Pinout for Notebook DRP application for 35-CSP.

Table 3 provides the pin definition for 40-pin QFN for Notebook (DFP) application. Refer to Table 23 for part numbers to package mapping.

**Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP)**

| Functional Pin Name | Active HIGH/LOW | Drive Mode                            | CYPD 1134-40LQXI Pins | Type | Description   |
|---------------------|-----------------|---------------------------------------|-----------------------|------|---|
| MUXSEL_1            | –               | Open drain, drives low                | 1                     | O    | External Data Mux Select signal 1   |
| MUXSEL_2            | –               | Open drain, drives low                | 2                     | O    | External Data Mux Select signal 2   |
| CC1_CTRL            | –               | Analog input/Strong drive (push pull) | 3                     | IO   | CC1 control<br>0:Tx enabled<br>z: RX sense  |
| CC2_CTRL            | –               | Analog input/Strong drive (push pull) | 4                     | IO   | CC2 control<br>0: TX enabled<br>z: RX sense   |
| MUXSEL_3            | –               | Open drain, drives low                | 5                     | O    | External Data Mux Select signal 3   |
| MUXSEL_4            | –               | Open drain, drives low                | 6                     | O    | External Data Mux Select signal 4   |
| CS_P                | –               | Analog input                          | 7                     | I    | Current Sensing Plus input  |
| CS_M                | –               | Analog input                          | 8                     | I    | Current Sensing Minus input   |
| VSS                 | –               | –                                     | 9                     | GND  | Ground  |
| CC1                 | –               | Strong drive (push pull)              | 10                    | O    | Configuration Channel 1   |
| CC1_RP_1.5          | Active HIGH     | Open drain, drives high               | 11                    | O    | Open Drain signal to connect RP to CC1 line (1.5A current)<br>z: RP not connected<br>1: RP connected    |
| SWD_IO              | –               | –                                     | 12                    | IO   | SWD IO  |
| SWD_CLK             | –               | –                                     | 13                    | I    | SWD Clock   |
| CC1_RP_3.0          | Active HIGH     | Open drain, drives high               | 14                    | O    | Open Source signal to connect RP to CC1 line (3A current)<br>z: RP not connected<br>1: RP connected     |
| CC1_RP_DEF          | Active HIGH     | Open drain, drives high               | 15                    | O    | Open Drain signal to connect RP to CC1 line (Default current)<br>z: RP not connected<br>1: RP connected |
| CC2_RP_DEF          | Active HIGH     | Open drain, drives high               | 16                    | O    | Open Drain signal to connect RP to CC2 line (Default current)<br>z: RP not connected<br>1: RP connected |
| CC2_RP_1.5          | Active HIGH     | Open drain, drives high               | 17                    | O    | Open Drain signal to connect RP to CC2 line (1.5A current)<br>z: RP not connected<br>1: RP connected    |
| I2C_SCL             | Active LOW      | Open drain, drives low                | 18                    | IO   | I <sup>2</sup> C Clock signal   |
| I2C_SDA             | Active LOW      | Open drain, drives low                | 19                    | IO   | I <sup>2</sup> C Data signal  |

**Table 3. Pin Definitions for 40-Pin QFN for Notebook (DFP) (continued)**

| Functional Pin Name        | Active HIGH/<br>LOW | Drive Mode                               | CYPD<br>1134-40LQXI<br>Pins | Type  | Description  |
|----------------------------|---------------------|--|-----------------------------|-------|--|
| I2C_INT                    | Active LOW          | Open drain, drives low                   | 20                          | O     | I <sup>2</sup> C Interrupt   |
| CC2_RP_3.0                 | Active HIGH         | Open drain, drives high                  | 21                          | O     | Open Source signal to connect RP to CC2 line (3A current)<br>z: RP not connected<br>1: RP connected                      |
| CC1_LPRX                   | –                   | Analog input                             | 22                          | I     | Configuration channel 1 RX signal for Low Power states   |
| CC1_LPREF                  | –                   | Analog input                             | 23                          | I     | Reference signal for internal use.   |
| CC2_LPRX                   | –                   | Analog input                             | 24                          | I     | Configuration channel 2 RX signal for Low Power states   |
| CC2_LPREF                  | –                   | Analog input                             | 25                          | I     | Reference signal for internal use.   |
| CC2                        | –                   | Strong drive (push pull)                 | 26                          | O     | Configuration Channel 2  |
| CC1_VCONN_CTRL             | Active LOW          | Open drain, drives low                   | 27                          | O     | Open Drain signal to control a PFET power switch for VCONN on CC1 line<br>0: VCONN switch closed<br>z: VCONN switch open |
| CC2_VCONN_CTRL             | Active LOW          | Open drain, drives low                   | 28                          | O     | Open Drain signal to control a PFET power switch for VCONN on CC2 line<br>0: VCONN switch closed<br>z: VCONN switch open |
| IFault                     | Active HIGH         | Digital input                            | 29                          | I     | Current Fault Indication on VBUS<br>0: No fault<br>1: Over Current fault   |
| XRES                       | Active LOW          | Analog input                             | 30                          | I     | Reset  |
| VCCD                       | –                   | –  | 31                          | POWER | Connect 1uf Capacitor between VCCD and Ground  |
| VDDD                       | –                   | –  | 32                          | POWER | 5-V Supply   |
| VDDA                       | –                   | –  | 33                          | POWER | 5-V Supply   |
| VSSA                       | –                   | –  | 34                          | GND   | –  |
| E-PAD                      | –                   | –  | E-PAD                       | GND   | –  |
| VBUS_VMON                  | –                   | Analog input                             | 35                          | I     | VBUS Over-voltage Protection monitoring signal   |
| VBUS_VREF                  | –                   | Analog input                             | 36                          | I     | VBUS reference signal for Over-voltage Protection detection  |
| VBUS_P_CTRL                | Active HIGH         | Strong drive (Push Pull)                 | 37                          | O     | Full rail control signal for enabling/disabling Provider load FET  |
| HOTPLUG_DET                | Active HIGH         | Open drain, drives low                   | 38                          | IO    | HotPlug Detection for Display Port Alternate Mode  |
| CC_VREF/<br>VBUS_DISCHARGE | -/Active<br>HIGH    | Analog input/Strong<br>drive (Push Pull) | 39                          | IO    | Data reference signal for CC lines /<br>Signal used for discharging VBUS line during voltage change                      |
| MUXSEL_5                   | –                   | Open drain, drives low                   | 40                          | O     | External Data Mux Select signal 5  |



Table 4 provides the pin definition for 16-pin SOIC for the Power Adapter application. Refer to Table 23 on page 23 for part numbers to package mapping.

**Table 4. Pin Definitions for 16-pin SOIC for Power Adapter Application**

| Functional Pin Name    | CYPD 1132-16SXI Pins | Type | Description   |
|------------------------|----------------------|------|---|
| SWD_CLK                | 1                    | I    | SWD Clock   |
| VBUS_P_CTRL            | 2                    | O    | Full rail control signal for enabling/disabling provider load FET   |
| VBUS_VMON              | 3                    | I    | VBUS over-voltage protection monitoring signal  |
| VBUS_VREF              | 4                    | I    | VBUS reference signal for over-voltage protection detection   |
| XRES                   | 5                    | –    | Active Low Reset  |
| VCCD                   | 6                    | –    | Connect 1 $\mu$ F capacitor between VCCD and GROUND   |
| VSSD                   | 7                    | –    | Ground  |
| VDDD                   | 8                    | –    | Power 3.3 V/5 V   |
| VSSA                   | 9                    | –    | Ground  |
| CC_VREF/VBUS_DISCHARGE | 10                   | I/O  | Data reference signal for CC line (0.55 Volt) / Signal used for discharging VBUS line during voltage decrease |
| CC_CTRL                | 11                   | I/O  | CC1 control<br>0: TX enabled<br>z: RX sense   |
| CS                     | 12                   | I    | Low Side Current Sense  |
| VSEL1                  | 13                   | O    | Voltage select signal for selecting the output voltage 5/12/20 V  |
| VSEL2                  | 14                   | O    | Voltage select signal for selecting the output voltage 5/12/20 V  |
| CC                     | 15                   | I/O  | Configuration Channel TX/RX   |
| SWD_IO                 | 16                   | I/O  | SWD I/O   |

Pinouts

Figure 2. Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI

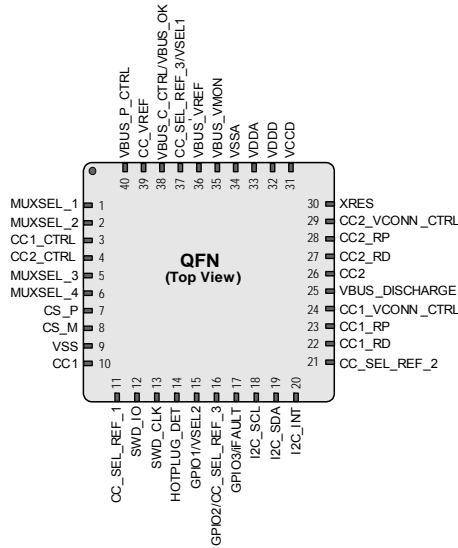


Figure 3. Pinout for CYPD1134-40LQXI

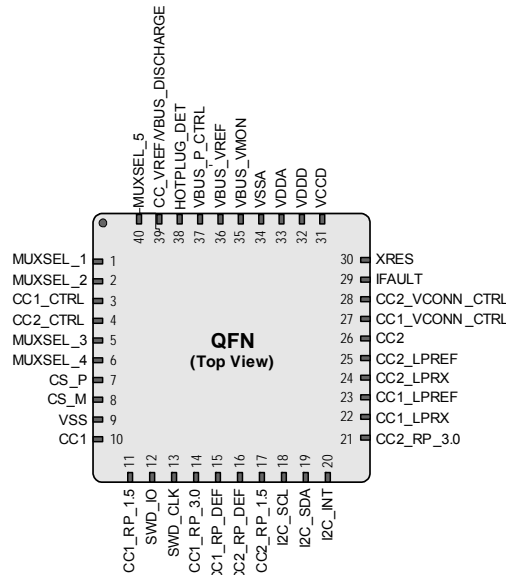


Figure 4. Pinout for CYPD1132-16SXI

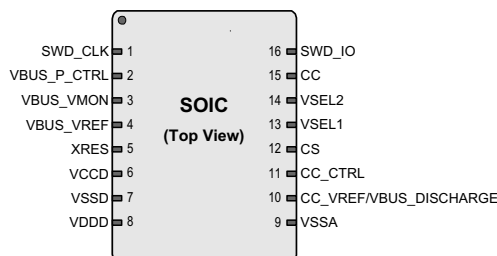
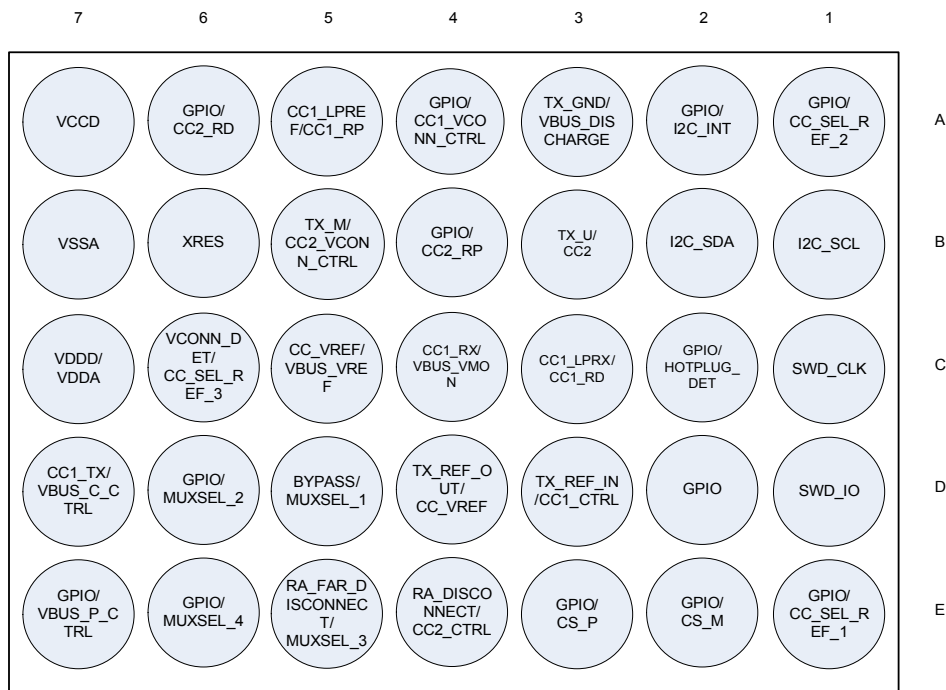


Figure 5. Pinout for CYPD1103-35FNXIT/CYPD1131-FNXIT



## Power

The following power system diagram shows the minimum set of power supply pins as implemented for the CCG1. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input. There is a separate regulator for the Deep Sleep mode. There is a separate low-noise regulator for the bandgap. The supply voltage range is 3.2 V to 5.5 V with all functions and circuits operating over that range.

VDDA and VDDD must be shorted together; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu$ F range in parallel with a smaller capacitor (0.1  $\mu$ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Refer to Application Diagrams for bypassing schemes.

## Electrical Specifications

### Absolute Maximum Ratings

**Table 5. Absolute Maximum Ratings<sup>[11]</sup>**

| Spec ID | Parameter                   | Description  | Min     | Typ | Max                    | Units | Details/<br>Conditions                 |
|---------|-----------------------------|--|---------|-----|------------------------|-------|--|
| SID1    | V <sub>DDD_ABS</sub>        | Digital supply relative to V <sub>SSD</sub>  | -0.50   | -   | 6.00                   | V     | Absolute max                           |
| SID2    | V <sub>CCD_ABS</sub>        | Direct digital core voltage input relative to V <sub>SSD</sub>   | -0.50   | -   | 1.95                   | V     | Absolute max                           |
| SID3    | V <sub>GPIO_ABS</sub>       | GPIO voltage   | -0.50   | -   | V <sub>DDD</sub> +0.50 | V     | Absolute max                           |
| SID4    | I <sub>GPIO_ABS</sub>       | Maximum current per GPIO   | -25.00  | -   | 25.00                  | mA    | Absolute max                           |
| SID5    | I <sub>GPIO_injection</sub> | GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub> | -0.50   | -   | 0.50                   | mA    | Absolute max, current injected per pin |
| BID44   | ESD_HBM                     | Electrostatic discharge human body model   | 2200.00 | -   | -                      | V     | -                                      |
| BID45   | ESD_CDM                     | Electrostatic discharge charged device model   | 500.00  | -   | -                      | V     | -                                      |
| BID46   | LU                          | Pin current for latch-up   | -200.00 | -   | 200.00                 | mA    | -                                      |

### Device-Level Specifications

All specifications are valid for -40 °C ≤ T<sub>A</sub> ≤ 85 °C and T<sub>J</sub> ≤ 100 °C for 35-CSP and 40-QFN package options. Specifications are valid for -40 °C ≤ T<sub>A</sub> ≤ 105 °C and T<sub>J</sub> ≤ 120 °C for 16-SOIC package options. Specifications are valid for 3.2 V to V<sub>DD</sub>'s maximum value, depending on the type of application.

**Table 6. DC Specifications**

| Spec ID  | Parameter          | Description                                | Min  | Typ   | Max   | Units | Details/<br>Conditions                                   |
|--|--------------------|--|------|-------|-------|-------|--|
| SID53  | V <sub>DDD</sub>   | Power supply input voltage                 | 3.20 | -     | 5.20  | V     | Notebook, tablet, monitor and power adapter applications |
| SID53_A  | V <sub>DDD</sub>   | Power supply input voltage                 | 3.20 | -     | 5.50  | V     | EMCA applications  |
| SID54  | V <sub>CCD</sub>   | Output voltage (for core logic)            | -    | 1.80  | -     | V     | -  |
| SID55  | C <sub>EFC</sub>   | External regulator voltage bypass          | 1.00 | 1.30  | 1.60  | μF    | X5R ceramic or better                                    |
| SID56  | C <sub>EXC</sub>   | Power supply decoupling capacitor          | -    | 1.00  | -     | μF    | X5R ceramic or better                                    |
| <b>Active Mode, V<sub>DDD</sub> = 3.2 to 5.5 V. Typical values measured at V<sub>DD</sub> = 3.3 V.</b> |                    |  |      |       |       |       |  |
| SID19  | I <sub>DD14</sub>  | Execute from flash; CPU at 48 MHz          | -    | 12.80 | -     | mA    | T = 25 °C  |
| SID20  | I <sub>DD15</sub>  | Execute from flash; CPU at 48 MHz          | -    | -     | 13.80 | mA    | -  |
| <b>Sleep Mode, V<sub>DDD</sub> = 3.2 to 5.5 V</b>  |                    |  |      |       |       |       |  |
| SID25A   | I <sub>DD20A</sub> | I <sup>2</sup> C wakeup and comparators on | -    | 1.70  | 2.20  | mA    | -  |
| <b>Deep Sleep Mode, V<sub>DDD</sub> = 3.2 to 3.6 V (Regulator on)</b>                                  |                    |  |      |       |       |       |  |
| SID31  | I <sub>DD26</sub>  | I <sup>2</sup> C wakeup on                 | -    | 1.30  | -     | μA    | T = 25 °C, 3.6 V   |
| SID32  | I <sub>DD27</sub>  | I <sup>2</sup> C wakeup on                 | -    | -     | 50.00 | μA    | T = 85 °C  |
| <b>Deep Sleep Mode, V<sub>DDD</sub> = 3.6 to 5.5 V</b>   |                    |  |      |       |       |       |  |
| SID34  | I <sub>DD29</sub>  | I <sup>2</sup> C wakeup                    | -    | 15.00 | -     | μA    | T = 25 °C, 5 V   |
| <b>XRES Current</b>  |                    |  |      |       |       |       |  |
| SID307   | I <sub>DD_XR</sub> | Supply current while XRES asserted         | -    | 2.00  | 5.00  | mA    | -  |

**Note**

11. Usage above the absolute maximum conditions listed in Table 5 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

**Table 7. AC Specifications**

| Spec ID | Parameter               | Description                 | Min  | Typ  | Max   | Units | Details/<br>Conditions                     |
|---------|-------------------------|-----------------------------|------|------|-------|-------|--|
| SID48   | F <sub>CPU</sub>        | CPU frequency               | DC   | –    | 48.00 | MHz   | 3.2 ≤ V <sub>DD</sub> ≤ 5.5                |
| SID49   | T <sub>SLEEP</sub>      | Wakeup from sleep mode      | –    | 0.00 | –     | μs    | Guaranteed by characterization             |
| SID50   | T <sub>DEEPSLEEP</sub>  | Wakeup from Deep Sleep mode | –    | –    | 25.00 | μs    | 24-MHz IMO. Guaranteed by characterization |
| SID52   | T <sub>RESETWIDTH</sub> | External reset pulse width  | 1.00 | –    | –     | μs    | Guaranteed by characterization             |

I/O

**Table 8. I/O DC Specifications**

| Spec ID | Parameter                       | Description  | Min                       | Typ   | Max                     | Units | Details/<br>Conditions                                   |
|---------|---------------------------------|--|---------------------------|-------|-------------------------|-------|--|
| SID57   | V <sub>IH</sub> <sup>[12]</sup> | Input voltage high threshold   | 0.70 × V <sub>DDD</sub>   | –     | –                       | V     | CMOS Input   |
| SID58   | V <sub>IL</sub>                 | Input voltage low threshold  | –                         | –     | 0.30 × V <sub>DDD</sub> | V     | CMOS Input   |
| SID243  | V <sub>IH</sub> <sup>[12]</sup> | LVTTL input  | 2.00                      | –     | –                       | V     | –  |
| SID244  | V <sub>IL</sub>                 | LVTTL input  | –                         | –     | 0.80                    | V     | –  |
| SID59   | V <sub>OH</sub>                 | Output voltage high level  | V <sub>DDD</sub><br>–0.60 | –     | –                       | V     | I <sub>OH</sub> = 4 mA at 3 V V <sub>DDD</sub>           |
| SID62   | V <sub>OL</sub>                 | Output voltage low level   | –                         | –     | 0.60                    | V     | I <sub>OL</sub> = 8 mA at 3 V V <sub>DDD</sub>           |
| SID62A  | V <sub>OL</sub>                 | Output voltage low level   | –                         | –     | 0.40                    | V     | I <sub>OL</sub> = 3 mA at 3 V V <sub>DDD</sub>           |
| SID63   | R <sub>PULLUP</sub>             | Pull-up resistor   | 3.50                      | 5.60  | 8.50                    | kΩ    | –  |
| SID64   | R <sub>PULLDOWN</sub>           | Pull-down resistor   | 3.50                      | 5.60  | 8.50                    | kΩ    | –  |
| SID65   | I <sub>IL</sub>                 | Input leakage current (absolute value)                               | –                         | –     | 2.00                    | nA    | 25 °C, V <sub>DDD</sub> = 3.0 V                          |
| SID65A  | I <sub>IL_CTBM</sub>            | Input leakage current (absolute value) for analog pins               | –                         | –     | 4.00                    | nA    | –  |
| SID66   | C <sub>IN</sub>                 | Input capacitance  | –                         | –     | 7.00                    | pF    | –  |
| SID67   | V <sub>HYSTTL</sub>             | Input hysteresis LVTTL   | 15.00                     | 40.00 | –                       | mV    | V <sub>DDD</sub> ≥ 2.7 V. Guaranteed by characterization |
| SID68   | V <sub>HYS CMOS</sub>           | Input hysteresis CMOS  | 200.00                    | –     | –                       | mV    | V <sub>DDD</sub> ≥ 4.5 V. Guaranteed by characterization |
| SID69   | I <sub>DIODE</sub>              | Current through protection diode to V <sub>DD</sub> /V <sub>SS</sub> | –                         | –     | 100.00                  | μA    | Guaranteed by characterization                           |
| SID69A  | I <sub>TOT_GPIO</sub>           | Maximum Total Source or Sink Chip Current                            | –                         | –     | 200.00                  | mA    | Guaranteed by characterization                           |

**Table 9. I/O AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter          | Description | Min  | Typ | Max   | Units | Details/<br>Conditions                  |
|---------|--------------------|-------------|------|-----|-------|-------|---|
| SID70   | T <sub>RISEF</sub> | Rise time   | 2.00 | –   | 12.00 | ns    | 3.3-V V <sub>DDD</sub> , Clload = 25 pF |
| SID71   | T <sub>FALLF</sub> | Fall time   | 2.00 | –   | 12.00 | ns    | 3.3-V V <sub>DDD</sub> , Clload = 25 pF |

**Note**

 12. V<sub>IH</sub> must not exceed V<sub>DDD</sub> + 0.2 V.

XRES

**Table 10. XRES DC Specifications**

| Spec ID | Parameter            | Description   | Min                     | Typ    | Max                     | Units | Details/<br>Conditions         |
|---------|----------------------|---|-------------------------|--------|-------------------------|-------|--------------------------------|
| SID77   | V <sub>IH</sub>      | Input voltage high threshold  | 0.70 × V <sub>DDD</sub> | –      | –                       | V     | CMOS input                     |
| SID78   | V <sub>IL</sub>      | Input voltage low threshold   | –                       | –      | 0.30 × V <sub>DDD</sub> | V     | CMOS input                     |
| SID79   | R <sub>PULLUP</sub>  | Pull-up resistor  | 3.50                    | 5.60   | 8.50                    | kΩ    | –                              |
| SID80   | C <sub>IN</sub>      | Input capacitance   | –                       | 3.00   | –                       | pF    | –                              |
| SID81   | V <sub>HYSXRES</sub> | Input voltage hysteresis  | –                       | 100.00 | –                       | mV    | Guaranteed by characterization |
| SID82   | I <sub>DIODE</sub>   | Current through protection diode to V <sub>DDD</sub> /V <sub>SS</sub> | –                       | –      | 100.00                  | μA    | Guaranteed by characterization |

### Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

*Pulse Width Modulation (PWM) for VSEL and CUR\_LIM Pins*

**Table 11. PWM AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter               | Description                   | Min   | Typ | Max   | Units | Details/<br>Conditions |
|---------|-------------------------|-------------------------------|-------|-----|-------|-------|------------------------|
| SID140  | T <sub>PWMFREQ</sub>    | Operating frequency           | –     | –   | 48.00 | MHz   | –                      |
| SID141  | T <sub>PWMPWINT</sub>   | Pulse width (internal)        | 42.00 | –   | –     | ns    | –                      |
| SID142  | T <sub>PWMEXT</sub>     | Pulse width (external)        | 42.00 | –   | –     | ns    | –                      |
| SID143  | T <sub>PWMKILLINT</sub> | Kill pulse width (internal)   | 42.00 | –   | –     | ns    | –                      |
| SID144  | T <sub>PWMKILLEXT</sub> | Kill pulse width (external)   | 42.00 | –   | –     | ns    | –                      |
| SID145  | T <sub>PWMEINT</sub>    | Enable pulse width (internal) | 42.00 | –   | –     | ns    | –                      |
| SID146  | T <sub>PWMENEXT</sub>   | Enable pulse width (external) | 42.00 | –   | –     | ns    | –                      |
| SID147  | T <sub>PWMRESWINT</sub> | Reset pulse width (internal)  | 42.00 | –   | –     | ns    | –                      |
| SID148  | T <sub>PWMRESWEXT</sub> | Reset pulse width (external)  | 42.00 | –   | –     | ns    | –                      |

$I^2C$ 
**Table 12. Fixed I<sup>2</sup>C DC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter         | Description                                 | Min | Typ | Max    | Units | Details/Conditions |
|---------|-------------------|---|-----|-----|--------|-------|--------------------|
| SID149  | I <sub>I2C1</sub> | Block current consumption at 100 kHz        | –   | –   | 50     | μA    | –                  |
| SID150  | I <sub>I2C2</sub> | Block current consumption at 400 kHz        | –   | –   | 135.00 | μA    | –                  |
| SID151  | I <sub>I2C3</sub> | Block current consumption at 1 Mbps         | –   | –   | 310.00 | μA    | –                  |
| SID152  | I <sub>I2C4</sub> | I <sup>2</sup> C enabled in Deep Sleep mode | –   | –   | 1.40   | μA    | –                  |

**Table 13. Fixed I<sup>2</sup>C AC Specifications**

(Guaranteed by Characterization)

| Spec ID | Parameter         | Description | Min | Typ | Max  | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|------|-------|--------------------|
| SID153  | F <sub>I2C1</sub> | Bit rate    | –   | –   | 1.00 | Mbps  | –                  |

**Memory**
**Table 14. Flash DC Specifications**

| Spec ID | Parameter       | Description               | Min  | Typ | Max  | Units | Details/Conditions |
|---------|-----------------|---------------------------|------|-----|------|-------|--------------------|
| SID173  | V <sub>PE</sub> | Erase and program voltage | 3.20 | –   | 5.50 | V     | –                  |

**Table 15. Flash AC Specifications**

| Spec ID | Parameter                               | Description  | Min   | Typ | Max   | Units   | Details/Conditions             |
|---------|---|--|-------|-----|-------|---------|--------------------------------|
| SID174  | T <sub>ROWWRITE</sub> <sup>[13]</sup>   | Row (block) write time (erase and program)                       | –     | –   | 20.00 | ms      | Row (block) = 128 bytes        |
| SID175  | T <sub>ROWERASE</sub> <sup>[13]</sup>   | Row erase time   | –     | –   | 13.00 | ms      | –                              |
| SID176  | T <sub>ROWPROGRAM</sub> <sup>[13]</sup> | Row program time after erase                                     | –     | –   | 7.00  | ms      | –                              |
| SID178  | T <sub>BULKERASE</sub> <sup>[13]</sup>  | Bulk erase time (32 KB)  | –     | –   | 35.00 | ms      | –                              |
| SID180  | T <sub>DEVPROG</sub> <sup>[13]</sup>    | Total device program time  | –     | –   | 7.00  | seconds | Guaranteed by characterization |
| SID181  | F <sub>END</sub>                        | Flash endurance  | 100 K | –   | –     | cycles  | Guaranteed by characterization |
| SID182  | F <sub>RET</sub> <sup>[14]</sup>        | Flash retention. T <sub>A</sub> ≤ 55 °C, 100 K P/E cycles        | 20    | –   | –     | years   | Guaranteed by characterization |
| SID182A | –                                       | Flash retention. T <sub>A</sub> ≤ 85 °C, 10 K P/E cycles         | 10    | –   | –     | years   | Guaranteed by characterization |
| SID182B | –                                       | Flash retention. 85 °C < T <sub>A</sub> ≤ 105 °C, 10K P/E cycles | 3     | –   | –     | years   | Guaranteed by characterization |

**Notes**

13. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
14. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact [customer care@cypress.com](mailto:customer care@cypress.com).

**System Resources**
*Power-on-Reset (POR) with Brown Out*
**Table 16. Imprecise Power On Reset (PRES)**

| Spec ID | Parameter               | Description          | Min  | Typ | Max   | Units | Details/Conditions             |
|---------|-------------------------|----------------------|------|-----|-------|-------|--------------------------------|
| SID185  | V <sub>RISEIPOR</sub>   | Rising trip voltage  | 0.80 | –   | 1.45  | V     | Guaranteed by characterization |
| SID186  | V <sub>FALLIPOR</sub>   | Falling trip voltage | 0.75 | –   | 1.40  | V     | Guaranteed by characterization |
| SID187  | V <sub>IPOPORHYST</sub> | Hysteresis           | 15.0 | –   | 200.0 | mV    | Guaranteed by characterization |

**Table 17. Precise Power On Reset (POR)**

| Spec ID | Parameter              | Description                                | Min  | Typ | Max | Units | Details/Conditions             |
|---------|------------------------|--|------|-----|-----|-------|--------------------------------|
| SID190  | V <sub>FALLPPOR</sub>  | BOD trip voltage in active and sleep modes | 1.64 | –   | –   | V     | Guaranteed by characterization |
| SID192  | V <sub>FALLDPSLP</sub> | BOD trip voltage in Deep Sleep             | 1.40 | –   | –   | V     | Guaranteed by characterization |

*SWD Interface*
**Table 18. SWD Interface Specifications**

| Spec ID | Parameter                | Description   | Min             | Typ | Max             | Units | Details/Conditions                    |
|---------|--------------------------|---|-----------------|-----|-----------------|-------|---------------------------------------|
| SID213  | F <sub>_SWDCLK1</sub>    | $3.2\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ | –               | –   | 14.00           | MHz   | SWDCLK $\leq 1/3$ CPU clock frequency |
| SID215  | T <sub>_SWDI_SETUP</sub> | $T = 1/f$ SWDCLK                                    | $0.25 \times T$ | –   | –               | ns    | Guaranteed by characterization        |
| SID216  | T <sub>_SWDI_HOLD</sub>  | $T = 1/f$ SWDCLK                                    | $0.25 \times T$ | –   | –               | ns    | Guaranteed by characterization        |
| SID217  | T <sub>_SWDO_VALID</sub> | $T = 1/f$ SWDCLK                                    | –               | –   | $0.50 \times T$ | ns    | Guaranteed by characterization        |
| SID217A | T <sub>_SWDO_HOLD</sub>  | $T = 1/f$ SWDCLK                                    | 1               | –   | –               | ns    | Guaranteed by characterization        |

*Internal Main Oscillator*
**Table 19. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter         | Description                     | Min | Typ | Max     | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|---------|-------|--------------------|
| SID218  | I <sub>IMO1</sub> | IMO operating current at 48 MHz | –   | –   | 1000.00 | μA    | –                  |

**Table 20. IMO AC Specifications**

| Spec ID | Parameter               | Description          | Min | Typ    | Max   | Units | Details/Conditions          |
|---------|-------------------------|----------------------|-----|--------|-------|-------|-----------------------------|
| SID223  | F <sub>IMOTOL1</sub>    | Frequency variation  | –   | –      | ±2.00 | %     | With API-called calibration |
| SID226  | T <sub>STARTIMO</sub>   | IMO startup time     | –   | –      | 12.00 | μs    | –                           |
| SID229  | T <sub>JITRMSIMO3</sub> | RMS Jitter at 48 MHz | –   | 139.00 | –     | ps    | –                           |



*Internal Low-Speed Oscillator*
**Table 21. ILO DC Specifications**

(Guaranteed by Design)

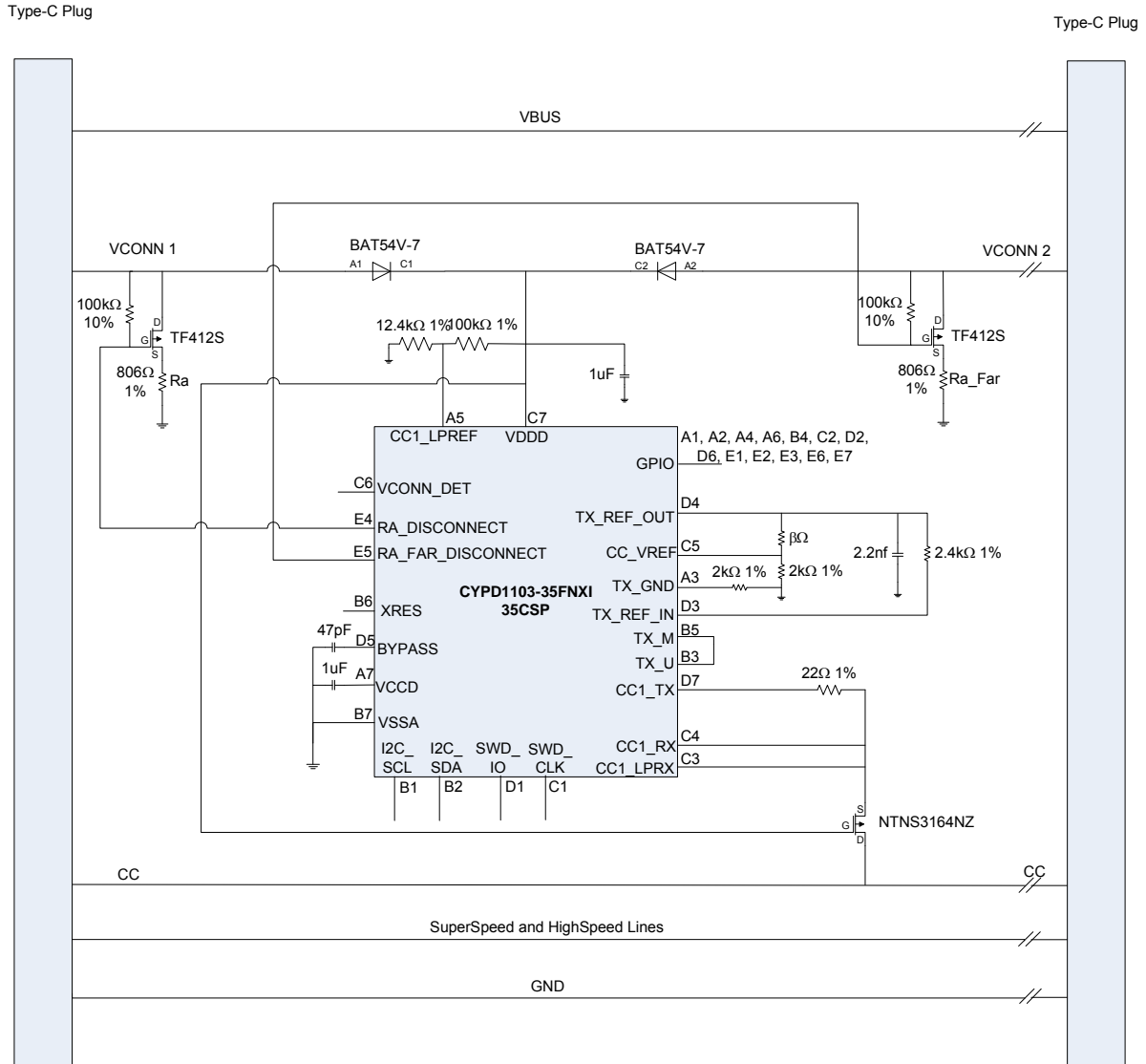
| Spec ID | Parameter            | Description                     | Min | Typ  | Max   | Units | Details/Conditions             |
|---------|----------------------|---------------------------------|-----|------|-------|-------|--------------------------------|
| SID231  | I <sub>ILO1</sub>    | ILO operating current at 32 kHz | –   | 0.30 | 1.05  | μA    | Guaranteed by characterization |
| SID233  | I <sub>ILOLEAK</sub> | ILO leakage current             | –   | 2.00 | 15.00 | nA    | Guaranteed by design           |

**Table 22. ILO AC Specifications**

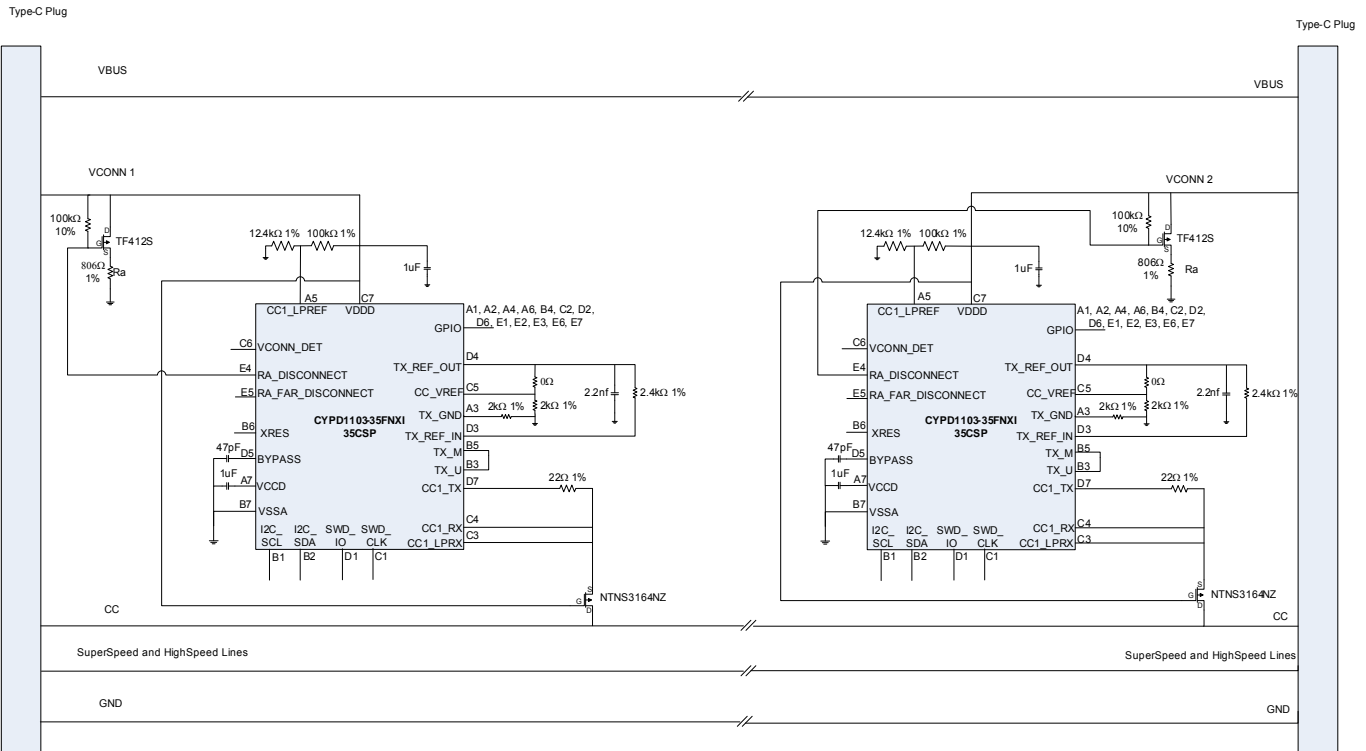
| Spec ID | Parameter              | Description              | Min   | Typ   | Max   | Units | Details/Conditions             |
|---------|------------------------|--------------------------|-------|-------|-------|-------|--------------------------------|
| SID234  | T <sub>STARTILO1</sub> | ILO startup time         | –     | –     | 2.00  | ms    | Guaranteed by characterization |
| SID236  | T <sub>ILODUTY</sub>   | ILO duty cycle           | 40.00 | 50.00 | 60.00 | %     | Guaranteed by characterization |
| SID237  | F <sub>ILOTRIM1</sub>  | 32-kHz trimmed frequency | 15.00 | 32.00 | 50.00 | kHz   | ±60% with trim                 |

Applications in Detail

Figure 6. Single Chip/Cable, Component Count = 19



**Figure 7. Two Chip/Cable, Component Count = 15/paddle**



**Figure 8. 16-pin SOIC Power Adapter Application Diagram**

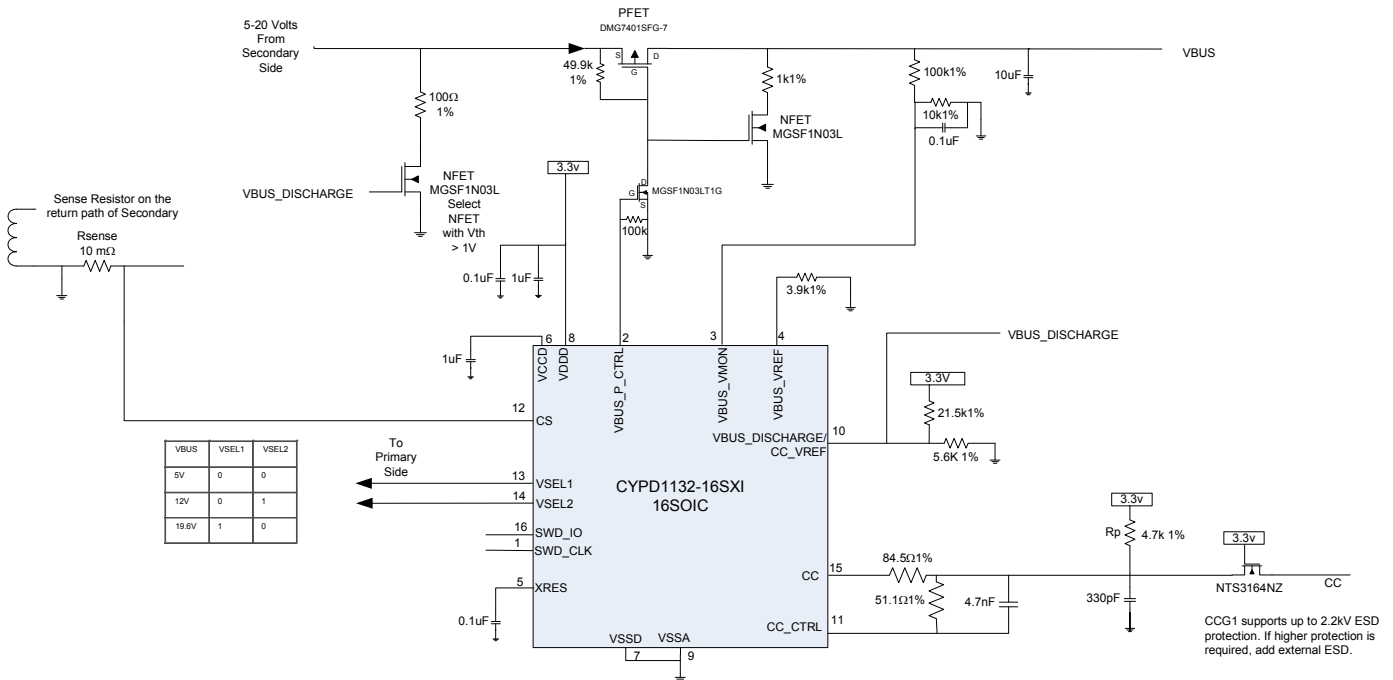
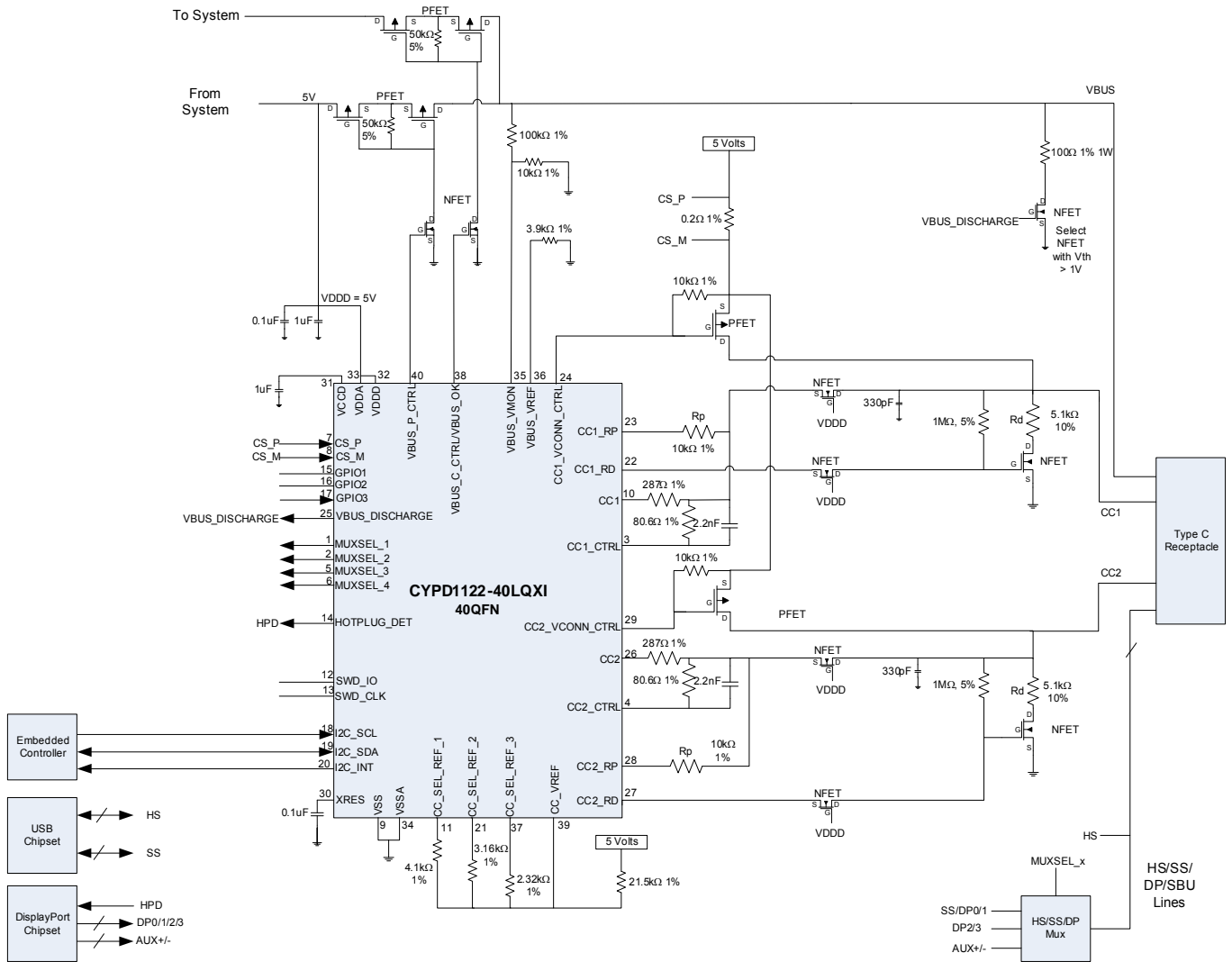
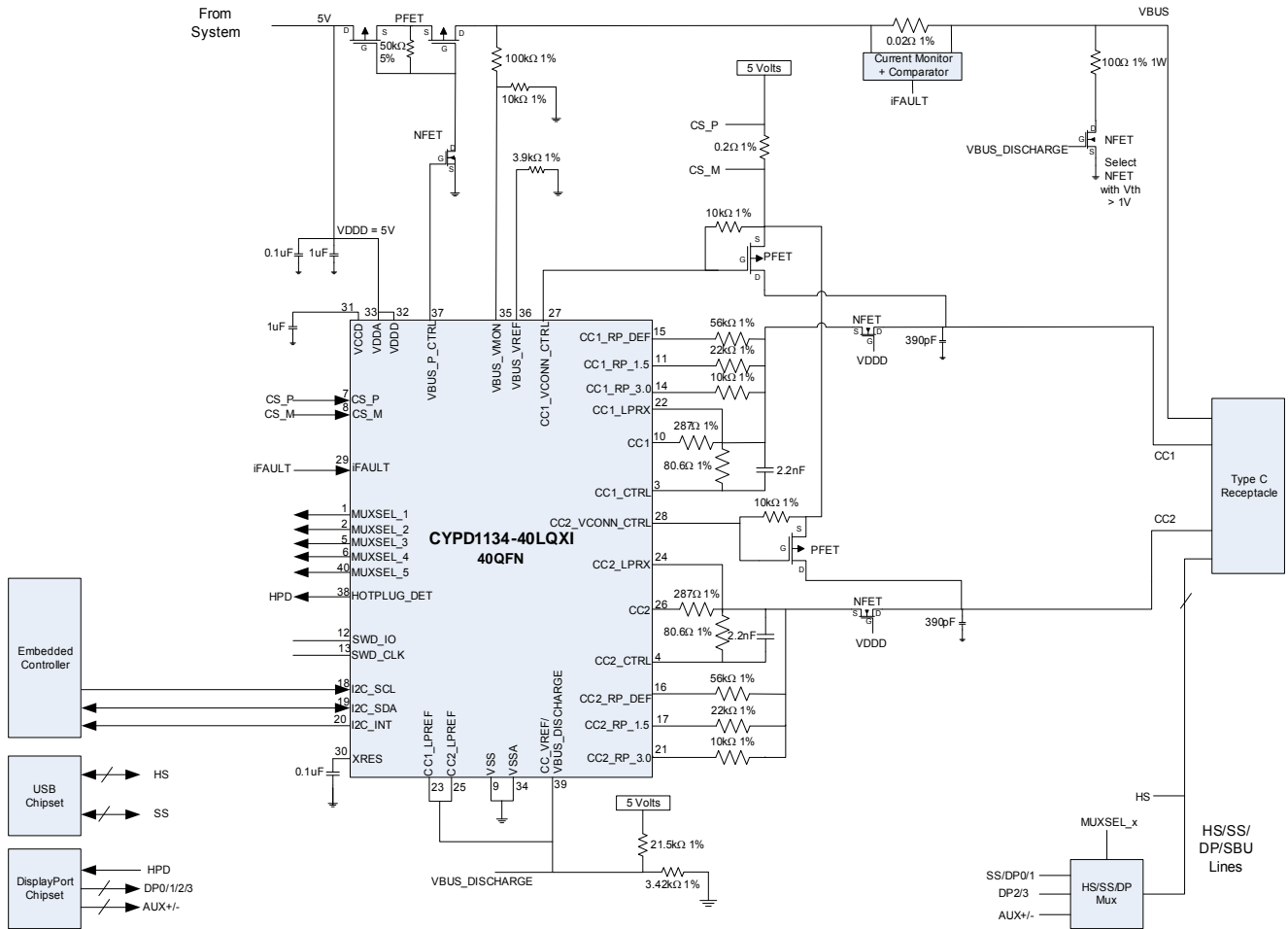


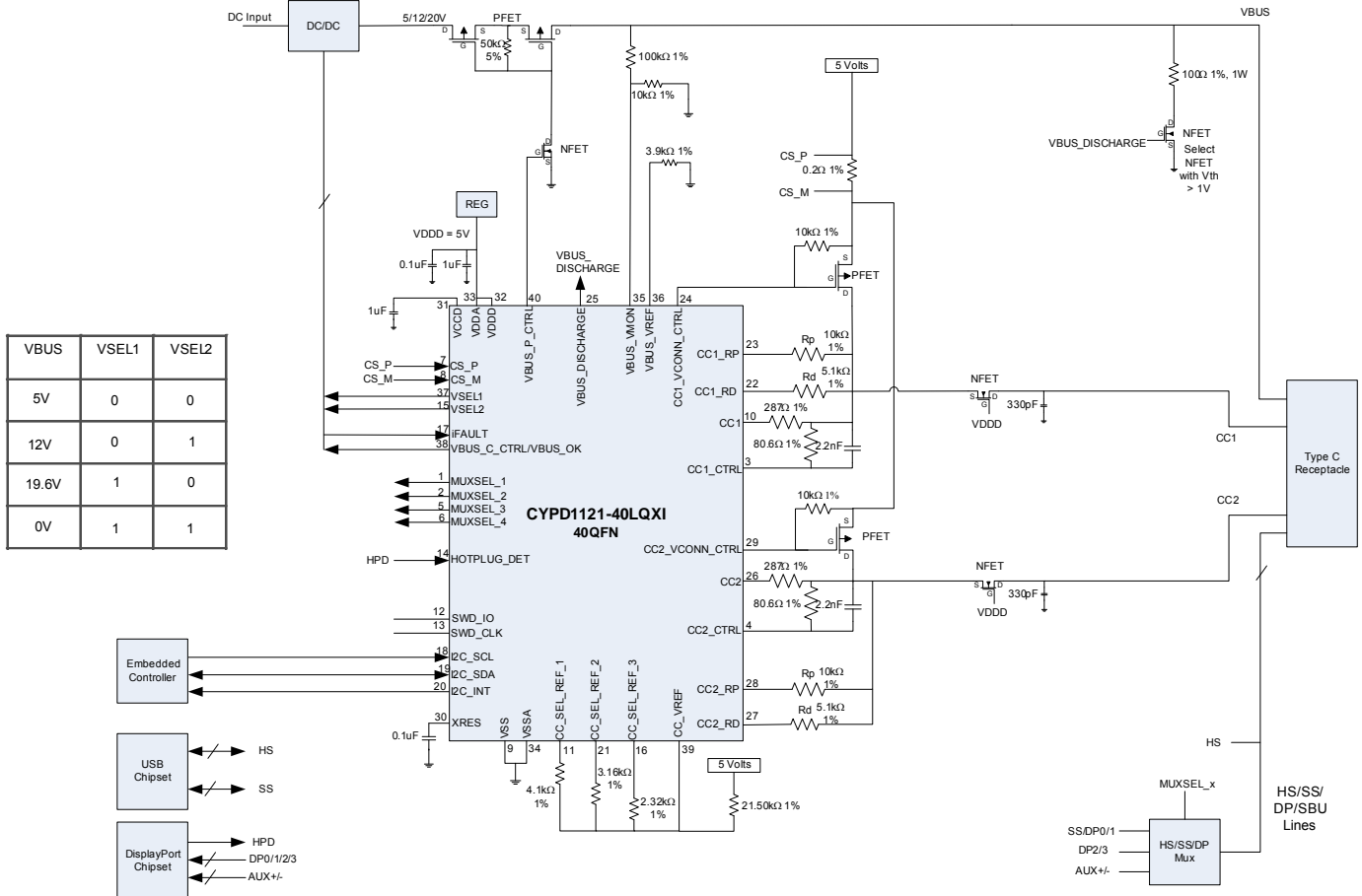
Figure 9. Notebook (DRP) Application Diagram



**Figure 10. Notebook (DFP) Application Diagram**



**Figure 11. Monitor Application Block Diagram**



## Ordering Information

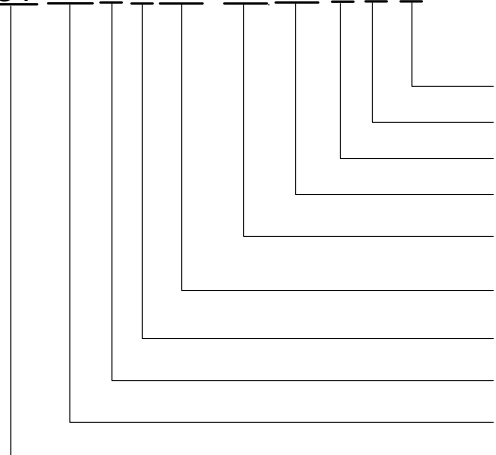
The CCG1 part numbers and features are listed in the following table.

**Table 23. CCG1 Ordering Information**

| Part Number <sup>[15]</sup> | Application                  | Type-C Ports <sup>[16]</sup> | Overcurrent Protection | Overvoltage Protection | Termination Resistor <sup>[17]</sup>          | Role <sup>[18]</sup> | Package                  | Si ID |
|-----------------------------|------------------------------|------------------------------|------------------------|------------------------|---|----------------------|--------------------------|-------|
| CYPD1103-35FNXIT            | Cable, EMCA                  | 1                            | No                     | No                     | $R_a$ <sup>[19]</sup>                         | Cable                | 35-WLCSP <sup>[20]</sup> | 0490  |
| CYPD1131-35FNXIT            | Notebook, Tablet, Smartphone | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup> , $R_d$ <sup>[21]</sup> | DRP <sup>[24]</sup>  | 35-WLCSP <sup>[22]</sup> | 0491  |
| CYPD1121-40LQXI             | Monitor                      | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup> , $R_d$ <sup>[21]</sup> | DRP <sup>[24]</sup>  | 40-QFN                   | 0489  |
| CYPD1122-40LQXI             | Notebook                     | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup> , $R_d$ <sup>[21]</sup> | DRP <sup>[24]</sup>  | 40-QFN                   | 048A  |
| CYPD1134-40LQXI             | Notebook, Desktop            | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup>                         | DFP                  | 40-QFN                   | 048B  |
| CYPD1132-16SXI              | Power Adapter                | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup>                         | DFP                  | 16-SOIC                  | 0498  |
| CYPD1132-16SXQ              | Power Adapter                | 1                            | Yes                    | Yes                    | $R_p$ <sup>[23]</sup>                         | DFP                  | 16-SOIC                  | 0498  |

## Ordering Code Definitions

CY PD X X XX- XX XX X X X



- T = Tape and reel for CSP, N/A for other packages
- Temperature Range: I = Industrial, Q = Extended industrial
- Lead: X = Pb-free
- Package Type: LQ = QFN, FN = CSP, S = SOIC
- Number of pins in the package
- 0X: OCP and OVP not supported, 1X: reserved, 2X, 3X: OCP and OVP supported
- Number of Type-C Ports: 1 = 1 Port, 2 = 2 Port
- Product Type: 1 = First-generation product family, CCG1
- Marketing Code: PD = Power delivery product family
- Company ID: CY = Cypress

### Notes

15. All part numbers support: Input voltage range from 3.2 V to 5.5 V. Industrial parts support -40 °C to +85 °C, Extended Industrial parts support -40 °C to 105 °C.
16. Number of USB Type-C Ports supported .
17. Default  $V_{CONN}$  termination.
18. PD Role.
19. Type-C Cable Termination.
20. 35-WLCSP #1 pinout.
21. USB Device Termination.
22. 35-WLCSP #2 pinout.
23. USB Host Termination.
24. Dual Role Port.

## Packaging

**Table 24. Package Characteristics**

| Parameter                       | Description                          | Conditions | Min | Typ   | Max    | Units   |
|---------------------------------|--------------------------------------|------------|-----|-------|--------|---------|
| T <sub>A</sub> (40-QFN, 35-CSP) | Operating ambient temperature        | –          | –40 | 25.00 | 85.00  | °C      |
| T <sub>J</sub> (40-QFN, 35-CSP) | Operating junction temperature       | –          | –40 | –     | 100.00 | °C      |
| T <sub>A</sub> (16-SOIC)        | Operating ambient temperature        | –          | –40 | 25.00 | 105.00 | °C      |
| T <sub>J</sub> (16-SOIC)        | Operating junction temperature       | –          | –40 | –     | 120.00 | °C      |
| T <sub>JA</sub>                 | Package θ <sub>JA</sub> (40-pin QFN) | –          | –   | 15.34 | –      | °C/Watt |
| T <sub>JA</sub>                 | Package θ <sub>JA</sub> (35-CSP)     | –          | –   | 28.00 | –      | °C/Watt |
| T <sub>JA</sub>                 | Package θ <sub>JA</sub> (16-SOIC)    | –          | –   | 85.00 | –      | °C/Watt |
| T <sub>JC</sub>                 | Package θ <sub>JC</sub> (40-pin QFN) | –          | –   | 02.50 | –      | °C/Watt |
| T <sub>JC</sub>                 | Package θ <sub>JC</sub> (35-CSP)     | –          | –   | 00.40 | –      | °C/Watt |
| T <sub>JC</sub>                 | Package θ <sub>JC</sub> (16-SOIC)    | –          | –   | 49.00 | –      | °C/Watt |

**Table 25. Solder Reflow Peak Temperature**

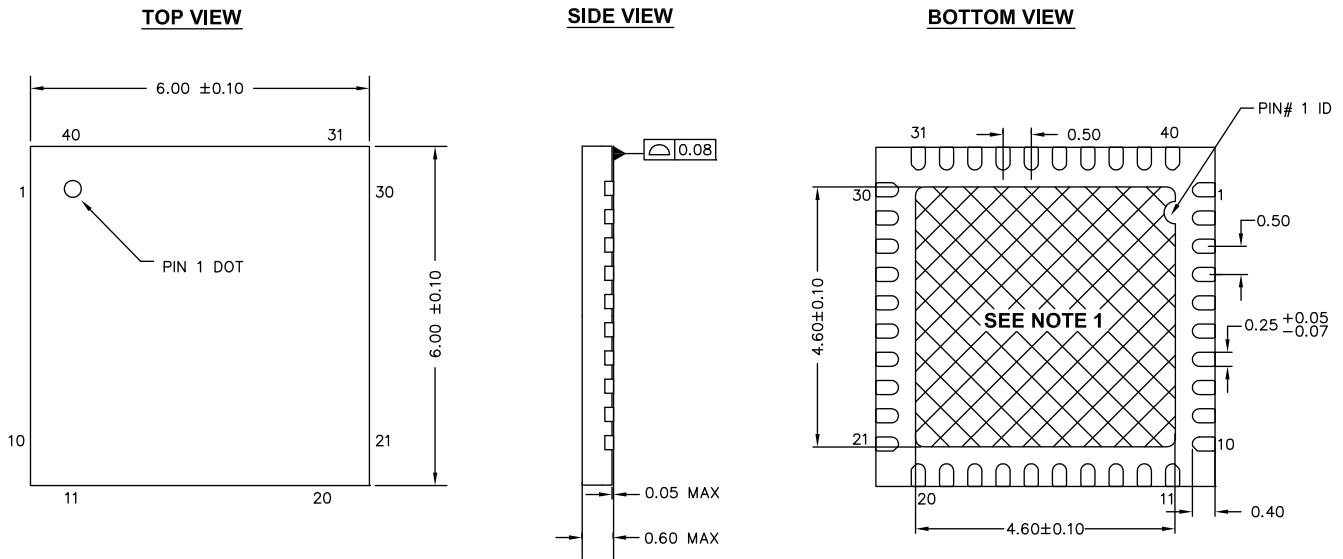
| Package       | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---------------|--------------------------|----------------------------------|
| 16-pin SOIC   | 260 °C                   | 30 seconds                       |
| 40-pin QFN    | 260 °C                   | 30 seconds                       |
| 35-ball WLCSP | 260 °C                   | 30 seconds                       |

**Table 26. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package       | MSL   |
|---------------|-------|
| 16-pin SOIC   | MSL 3 |
| 40-pin QFN    | MSL 3 |
| 35-ball WLCSP | MSL 1 |



Figure 12. 40-pin QFN Package Outline, 001-80659



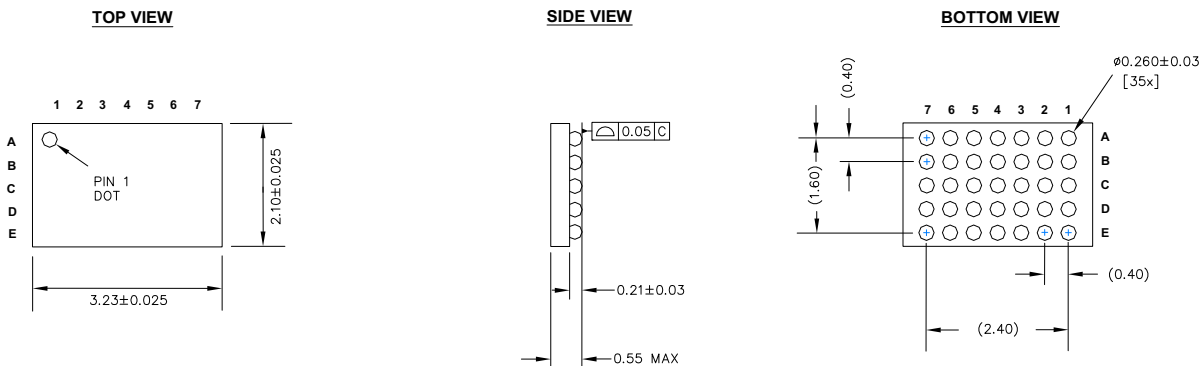
**NOTES:**

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 \*A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 13. 35-Ball WLCSP Package Outline, 001-93741

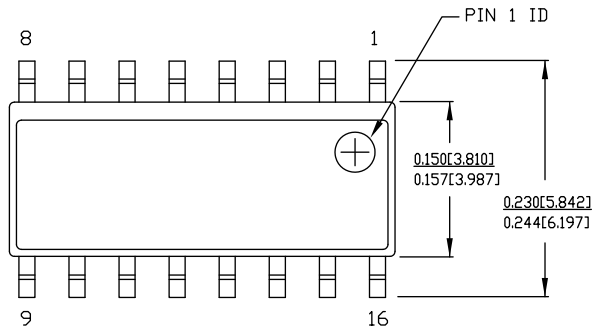


**NOTES:**

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-93741 \*\*

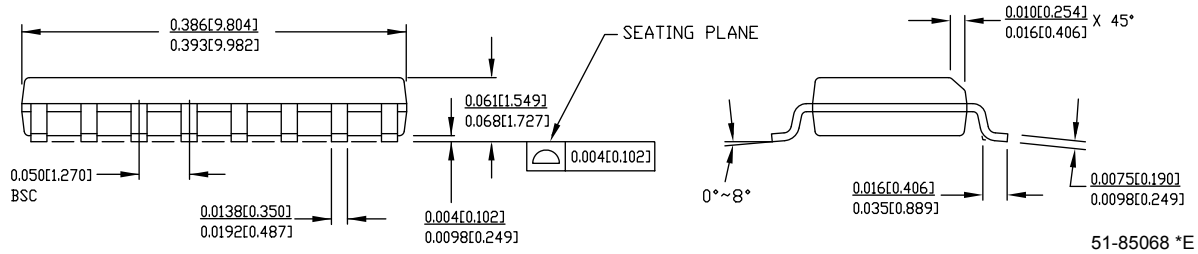
**Figure 14. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068**



**NOTE:**

1. DIMENSIONS IN INCHES[MM] **MAX.**
2. REFERENCE JEDEC MS-012
3. PACKAGE WEIGHT : refer to PMDD spec. 001-04308

| PART #  |                |
|---------|----------------|
| S16.15  | STANDARD PKG.  |
| SZ16.15 | LEAD FREE PKG. |



51-85068 \*E

## Acronyms

**Table 27. Acronyms Used in this Document**

| Acronym                  | Description   |
|--------------------------|---|
| ADC                      | analog-to-digital converter   |
| API                      | application programming interface   |
| ARM®                     | advanced RISC machine, a CPU architecture                                       |
| CC                       | Configuration Channel   |
| CPU                      | central processing unit   |
| CRC                      | cyclic redundancy check, an error-checking protocol                             |
| CS                       | Current Sense   |
| DFP                      | downstream facing port  |
| DIO                      | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| EEPROM                   | electrically erasable programmable read-only memory                             |
| EMI                      | electromagnetic interference  |
| ESD                      | electrostatic discharge   |
| FPB                      | flash patch and breakpoint  |
| FS                       | full-speed  |
| GPIO                     | general-purpose input/output, applies to a PSoC pin                             |
| IC                       | integrated circuit  |
| IDE                      | integrated development environment  |
| I <sup>2</sup> C, or IIC | Inter-Integrated Circuit, a communications protocol                             |
| ILO                      | internal low-speed oscillator, see also IMO                                     |
| IMO                      | internal main oscillator, see also ILO  |
| I/O                      | input/output, see also GPIO, DIO, SIO, USBIO                                    |
| LVD                      | low-voltage detect  |
| LVTTL                    | low-voltage transistor-transistor logic   |
| MCU                      | microcontroller unit  |
| NC                       | no connect  |
| NMI                      | nonmaskable interrupt   |
| NVIC                     | nested vectored interrupt controller  |

**Table 27. Acronyms Used in this Document** *(continued)*

| Acronym | Description  |
|---------|--|
| opamp   | operational amplifier  |
| OCP     | Overcurrent protection   |
| OVP     | Overvoltage protection   |
| PCB     | printed circuit board  |
| PGA     | programmable gain amplifier  |
| PHY     | physical layer   |
| POR     | power-on reset   |
| PRES    | precise power-on reset   |
| PSoC®   | Programmable System-on-Chip™   |
| PWM     | pulse-width modulator  |
| RAM     | random-access memory   |
| RISC    | reduced-instruction-set computing                                      |
| RMS     | root-mean-square   |
| RTC     | real-time clock  |
| RX      | receive  |
| SAR     | successive approximation register                                      |
| SCL     | I <sup>2</sup> C serial clock  |
| SDA     | I <sup>2</sup> C serial data   |
| S/H     | sample and hold  |
| SPI     | Serial Peripheral Interface, a communications protocol                 |
| SRAM    | static random access memory  |
| SWD     | serial wire debug, a test protocol                                     |
| TX      | transmit   |
| UART    | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UFP     | upstream facing port   |
| USB     | Universal Serial Bus   |
| USBIO   | USB input/output, PSoC pins used to connect to a USB port              |
| XRES    | external reset I/O pin   |

## Document Conventions

### Units of Measure

Table 28. Units of Measure

| Symbol | Unit of Measure        |
|--------|------------------------|
| °C     | degrees Celsius        |
| Hz     | hertz                  |
| KB     | 1024 bytes             |
| kHz    | kilohertz              |
| kΩ     | kilo ohm               |
| Mbps   | megabits per second    |
| MHz    | megahertz              |
| MΩ     | mega-ohm               |
| Msps   | megasamples per second |
| μA     | microampere            |
| μF     | microfarad             |
| μs     | microsecond            |
| μV     | microvolt              |
| μW     | microwatt              |
| mA     | milliampere            |
| ms     | millisecond            |
| mV     | millivolt              |
| nA     | nanoampere             |
| ns     | nanosecond             |
| Ω      | ohm                    |
| pF     | picofarad              |
| ppm    | parts per million      |
| ps     | picosecond             |
| s      | second                 |
| sps    | samples per second     |
| V      | volt                   |

**Revision History**

| Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery<br>Document Number: 001-93639 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change  |
| **   | 4520316 | MSMI            | 09/30/2014      | New datasheet  |
| *A   | 4531795 | SJH             | 10/13/2014      | Updated <a href="#">Functional Definition</a> .<br>Updated <a href="#">Figure 8</a> , <a href="#">Figure</a> , <a href="#">Figure 7</a> , <a href="#">Figure</a> , <a href="#">Figure 14</a> , <a href="#">Figure 9</a> .<br>Added <a href="#">Figure 11</a> .<br>Updated <a href="#">Pinouts</a> .<br>Updated <a href="#">Power</a> .<br>Updated <a href="#">Figure</a> , <a href="#">Figure 8</a> .<br>Updated <a href="#">Ordering Information</a><br>Added Note 24 and referred the same note in 40-pin QFN corresponding to CYPD1122-40LQXI.<br>Added Note 27 and referred the same note in 40-pin QFN corresponding to CYPD1134-40LQXI.  |
| *B   | 4569912 | SJH             | 11/21/2014      | Updated <a href="#">Features</a> .<br>Added 16-pin SOIC related information.<br>Updated <a href="#">Functional Definition</a> .<br>Updated <a href="#">Pin Definitions</a> .<br>Added <a href="#">Table 2</a> .<br>Updated <a href="#">Pinouts</a> .<br>Updated <a href="#">Figure 2</a> , <a href="#">Figure 5</a> .<br>Added <a href="#">Figure 4</a> .<br>Updated <a href="#">Power</a> .<br>Updated <a href="#">Figure</a> , <a href="#">Figure 8</a> .<br>Added <a href="#">Figure 6</a> .<br>Updated <a href="#">Electrical Specifications</a> .<br>Updated <a href="#">Device-Level Specifications</a> .<br>Updated <a href="#">Memory</a> .<br>Added Note 14 and referred the same note in $F_{RET}$ parameter.<br>Added details corresponding to spec ID SID182B under $F_{RET}$ parameter.<br>Updated <a href="#">Figure 14</a> , <a href="#">Figure 9</a> , <a href="#">Figure 11</a> . Added <a href="#">Figure 8</a> and <a href="#">Figure 10</a> .<br>Updated <a href="#">Ordering Information</a> .<br>Updated part numbers.<br>Added a column "Si ID".<br>Updated <a href="#">Packaging</a> .<br>Updated <a href="#">Table 24</a> .<br>Updated details in maximum value column corresponding to $T_A$ and $T_J$ parameters.<br>Added 16-pin SOIC related information.<br>Updated <a href="#">Table 25</a> . |
| *C   | 4596141 | SJH             | 12/14/2014      | Updated <a href="#">Figure 6</a> , <a href="#">Figure 14</a> , <a href="#">Figure 16</a> .<br>Updated <a href="#">Table 8</a> , <a href="#">Table 23</a> .   |
| *D   | 4646123 | SJH             | 02/04/2015      | Updated pin definitions for 40-pin QFN and 35-ball WLCSP.<br>Updated <a href="#">Pinout for CYPD1122-40LQXI/CYPD1121-40LQXI</a> and <a href="#">Ordering Information</a> .<br>Updated conditions for <a href="#">Device-Level Specifications</a> .<br>Updated diagrams in <a href="#">Applications in Detail</a> section.  |
| *E   | 4686050 | VGT             | 03/13/2015      | Removed information about 28-pin SSOP.<br>Updated <a href="#">Table 3</a> , <a href="#">Table 23</a> , <a href="#">Table 24</a> , <a href="#">Table 25</a> , <a href="#">Table 26</a> , <a href="#">Table 27</a> .<br>Updated <a href="#">Figure 2</a> , <a href="#">Figure</a> .  |
| *F   | 4747272 | VGT             | 05/13//2015     | Updated <a href="#">General Description</a> .<br>Added Note 1 and referenced it in <a href="#">Features</a> .<br>Updated <a href="#">Figure 6</a> , <a href="#">Figure 8</a> through <a href="#">Figure 11</a> .<br>Removed <a href="#">Figure 9</a> . Single Chip/Cable, Component Count = 13.<br>Removed <a href="#">Figure 11</a> . Two Chip/Cable, Component Count = 11/paddle.  |

**Revision History** *(continued)*

| Description Title: CCG1 Datasheet USB Type-C Port Controller with Power Delivery<br>Document Number: 001-93639 |         |                 |                 |  |
|--|---------|-----------------|-----------------|--|
| Revision   | ECN     | Orig. of Change | Submission Date | Description of Change  |
| *G   | 4800534 | VGT             | 07/02/2015      | Updated <a href="#">Low-Power Operation</a> .<br>Updated the number of GPIOs to “up to 30” in <a href="#">GPIO</a> .<br>Updated “1.8 to 5.5 V” to “3.2 V to 5.5 V” in <a href="#">Low-Power Operation</a> , <a href="#">Power System</a> , <a href="#">Power</a> , <a href="#">Device-Level Specifications</a> and <a href="#">Note 15</a> .<br>Updated <a href="#">Table 2</a> , <a href="#">Table 4</a> , <a href="#">Table 5</a> , <a href="#">Table 6</a> , <a href="#">Table 7</a> , <a href="#">Table 8</a> , <a href="#">Table 14</a> and <a href="#">Table 18</a> .<br>Added table footnotes <a href="#">8</a> , <a href="#">9</a> and <a href="#">10</a> .<br>Deleted footnotes <a href="#">25</a> through <a href="#">28</a> .<br>Updated <a href="#">Figure 2</a> and <a href="#">Figure 8</a> through <a href="#">Figure 11</a> .<br>Added <a href="#">Figure 3</a> .<br>Updated the following in <a href="#">Power</a> : Removed <a href="#">Figures 5</a> through <a href="#">8</a> . Updated the section. |
| *H   | 4939764 | VGT             | 09/29/2015      | Removed specs <a href="#">SID241</a> and <a href="#">242</a> .<br>Updated 40-pin QFN package to current revision.  |
| *I   | 5179365 | KISB            | 03/17/2016      | Updated max value of $I_{I2C1}$ from 10.50 $\mu$ A to 50 $\mu$ A.<br>Updated copyright information and sales links at the end of the document.   |
| *J   | 5459633 | VGT             | 10/03/2016      | Added compliance information regarding the USB Specification.<br>Updated copyright notice to include WICED.<br>Added IoT link in <a href="#">Sales, Solutions, and Legal Information</a> .   |
| *K   | 5725038 | VGT             | 05/03/2017      | Updated Cypress logo.<br>Updated Copyright information.  |

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