

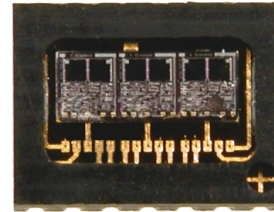
Optical Comparator Array

OPR5011



Features:

- Precise active area location
- Surface mountable
- TTL compatible output
- Wide supply voltage range
- Wide operating temperature range



Description:

Each **OPR5011** device is a hybrid sensor array that consists of three channels of the OPTEK differential optical comparator (“TRI-DOC”) IC. The single chip construction ensures very tight dimensional tolerances between active areas.

Specifically designed for high-speed/high-resolution encoder applications, the open collector output switches based on the comparison of the input photodiode’s light current levels. Logarithmic amplification of the input signals facilitates operation over a wide range of light levels.

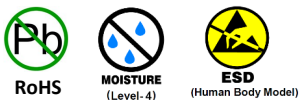
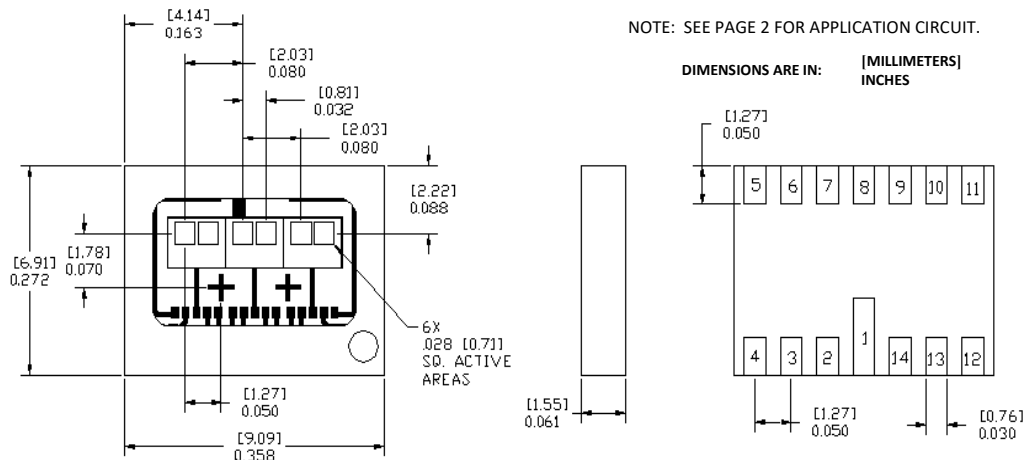
The surface-mountable opaque polyimide package shields the photodiodes from stray light and can withstand multiple exposures to the most demanding soldering conditions, while the gold-plated wraparound contacts provide exceptional storage and wetting characteristics.

See Application Bulletin 237 for handling instructions.

Applications:

- High-speed applications
- High-resolution applications
- Applications requiring a wide range of light levels

Warning: Front Window is pressure sensitive. Do not apply pressure or high vacuum to window.

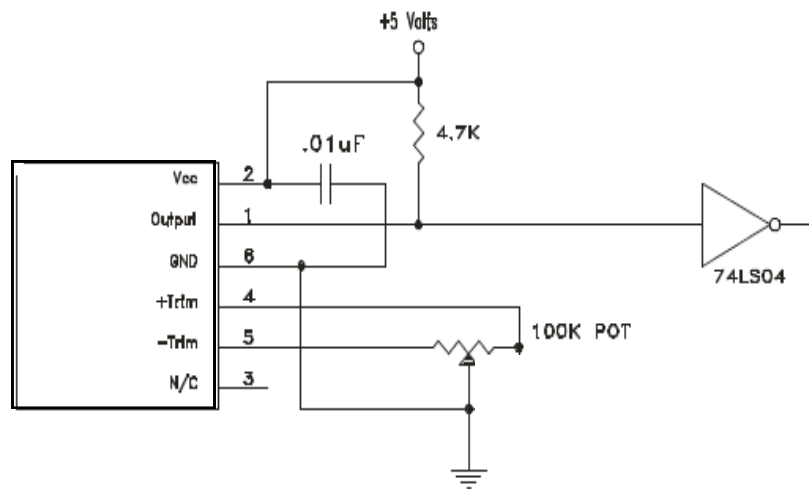


General Note
TT Electronics reserves the right to make changes in product specification without notice or liability. All information is subject to TT Electronics’ own data and is considered accurate at time of going to print.

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Ordering Information						
Part Number	Sensor	# of Elements	I _{cc} (mA) Typ / Max	Optical Hysteresis (%) Typical	Optical Offset (%) Min / Max	Packaging
OPR5011	Differential Optical Comparator	3	9 / 20	40.00	-40/+40	Chip Tray
OPR5011T	Differential Optical Comparator	3	9 / 20	40.00	-40/+40	Tape & Reel

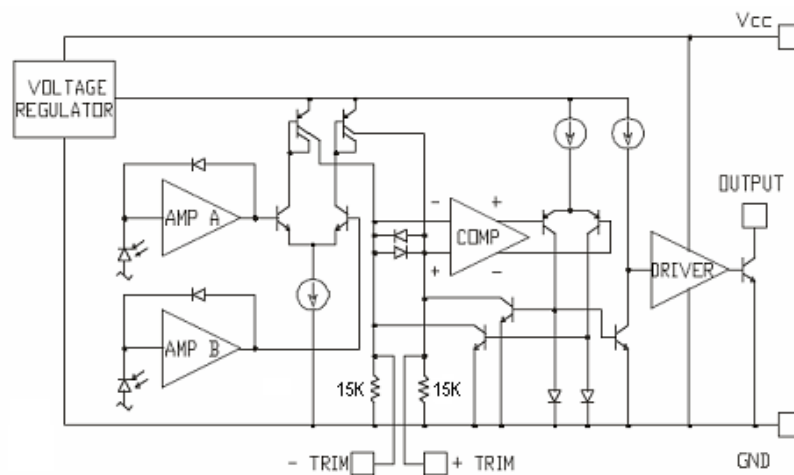
Application Circuit - OPR5011



Notes:

- (1) The 74LS04 is recommended as a means of isolating the “DOC” comparator circuitry from transients induced by inductive and capacitive loads.
- (2) It is recommended that a decoupling capacitor be placed as close as possible to the device.

Block Diagram - OPC8332



Electrical Specifications

Absolute Maximum Ratings (T_A = 25° C unless otherwise noted)

Storage and Operating Temperature	-40° C to +100° C
Supply Voltage	24 V
Output Voltage	24 V
Output Current	14 mA
Power Dissipation	500 mW
Solder reflow time within 5°C of peak temperature is 20 to 40 seconds ⁽¹⁾	250° C

Electrical Characteristics (T_A = 25° C unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I _{CC}	Supply Current	-	9	20	mA	V _{CC} = 24 V
V _{OL}	Low Level Output Voltage ⁽²⁾	-	0.3	0.4	V	I _{OL} = 14 mA, V _{CC} = 4.5 V
I _{OH}	High Level Output Current ⁽³⁾	-	0.1	1	µA	V _{CC} = V _O = 20 V
OPT-HYS	Optical Hysteresis ⁽⁴⁾⁽⁷⁾	-	40	-	%	V _{CC} = 5 V, I _{OL} = 1 mA
OPT-OFF	Optical Offset ⁽⁴⁾⁽⁷⁾	-40	10	+40	%	V _{CC} = 5 V, I _{OL} = 1 mA
f _{max}	Frequency Response ⁽⁵⁾	-	1	-	MHz	V _{CC} = 5 V
t _{lh}	Output Rise Time ⁽⁶⁾	-	1	-	µs	
t _{hl}	Output Fall Time ⁽⁶⁾	-	300	-	ns	

Notes:

- (1) Solder time less than 5 seconds at temperature extreme.
- (2) Pin (+) = 100.0 nW and Pin (-) = 1.0 µW .
- (3) Pin (+) = 1.0 µW and Pin (-) = 100.0 nW.
- (4) Pin (-) is held at 1.0 µW while Pin (+) is ramped from 0.5 µW to 1.5 µW and back to 0.5 µW.
- (5) Pin (+) is modulated from 1.0 µW to 2.0 µW. Pin (-) is modulated from 1.0 µW to 2.0 µW with phase shifted 180° with respect to Pin (+). Use 100 kΩ trimpot to set the output signal to 50% duty cycle for maximum operating frequency.
- (6) Measured between 10% and 90% points.
- (7) Optical Hysteresis and Optical Offset are found by placing 1.0 µW of light on the inverting photodiode and ramping the light intensity of the non-inverting input from 0.5 µW up to 1.5 µW and back down. This will produce two trigger points – an upper trigger point and lower trigger point. These points are used to calculate the optical hysteresis and offset.

These are defined as:

$$\% \text{ Optical Hysteresis} = 100 \times \frac{(P_{\text{rise}} - P_{\text{fall}})}{P_{\text{in}}(-)}$$

$$\% \text{ Optical Offset} = \frac{100 \times (P_{\text{average}} - P_{\text{in}}(-))}{P_{\text{in}}(-)}$$

Where:

P in (-) = Light level incident upon the “-” photodiode on the IC chip (Pin) (-) = 1.0 µW).

P rise = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is an increasing level (rising edge).

P fall = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is decreasing level (falling edge).

$$P_{\text{average}} = \frac{(P_{\text{rise}} + P_{\text{fall}})}{2}$$

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