

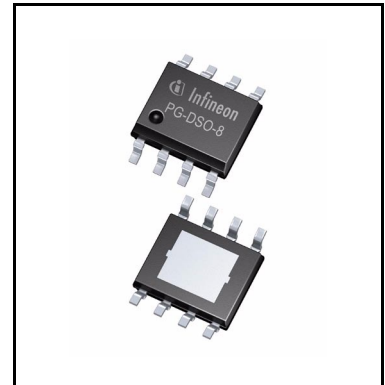
OPTIREG™ Linear TLE4263-2ES

5 V low drop voltage regulator



Features

- Output voltage tolerance $\leq \pm 2\%$
- 180 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog for monitoring microprocessor
- Power-on and undervoltage reset with programmable delay time
- Reset low down to $V_Q = 1V$
- Wide temperature range
- Exposed pad package with excellent thermal behavior
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ Linear TLE4263-2ES is a monolithic integrated very low dropout voltage regulator in a SMD package PG-DSO-8 exposed pad, especially designed for automotive applications. An input voltage up to 45 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 180 mA. The IC is short-circuit proof by the implemented current limitation and has an integrated overtemperature shutdown.

It additionally provides features like power-on and undervoltage reset with adjustable reset threshold, a watchdog circuit for monitoring a connected microcontroller and an inhibit input for enabling or disabling the component.

The reset output RO is set to “low” in case the output voltage falls below the reset switching threshold $V_{Q,rt}$. This threshold can be decreased down to 3.5 V by an external resistor divider. The power-on reset delay time can be programmed by the external delay capacitor CD.

The watchdog circuit provides a monitoring function for microcontrollers: At missing pulses on the watchdog’s input W the reset output RO is set to “low”. The trigger time for the watchdog pulses can be set by the external capacitor CD.

The IC can be switched off by the inhibit input, reducing the current consumption to typically 0 mA.

Type	Package	Marking
TLE4263-2ES	PG-DSO-8 exposed pad	4263-2

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Block diagram

1 Block diagram

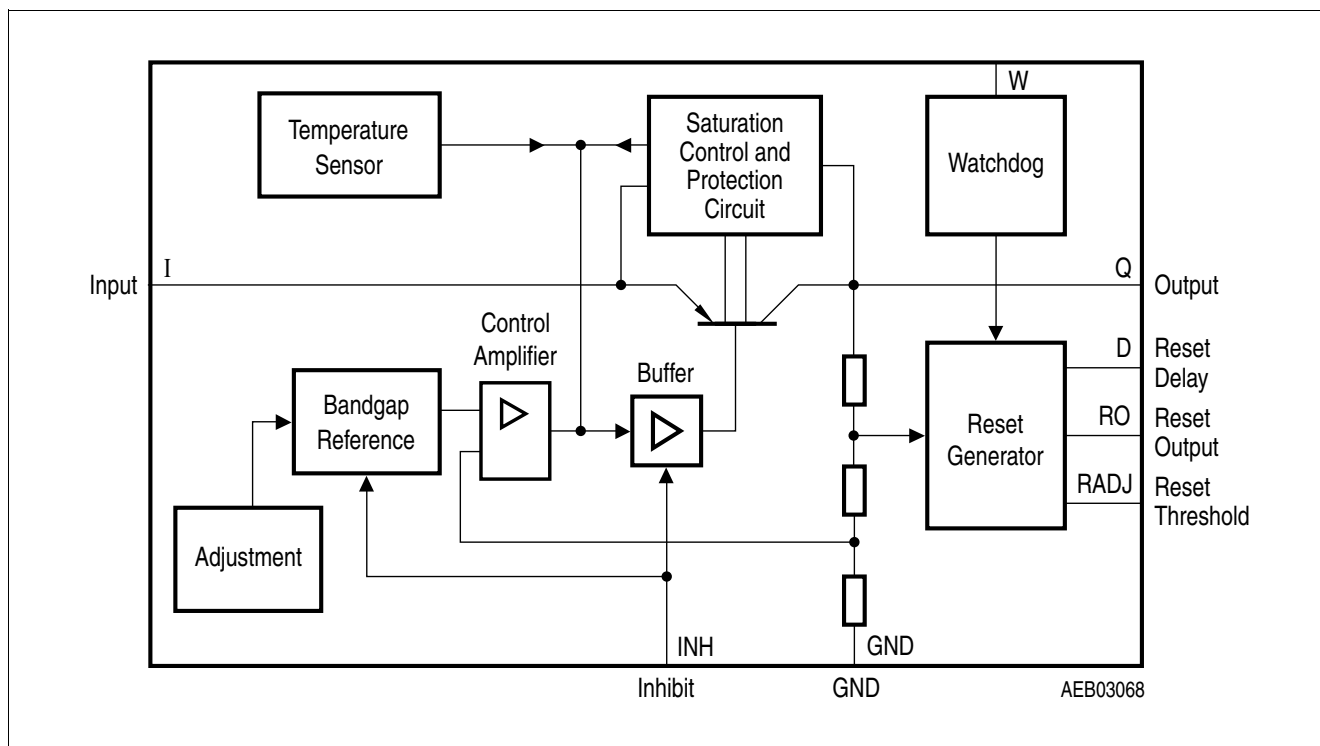


Figure 1 Block diagram

Pin configuration

2 Pin configuration

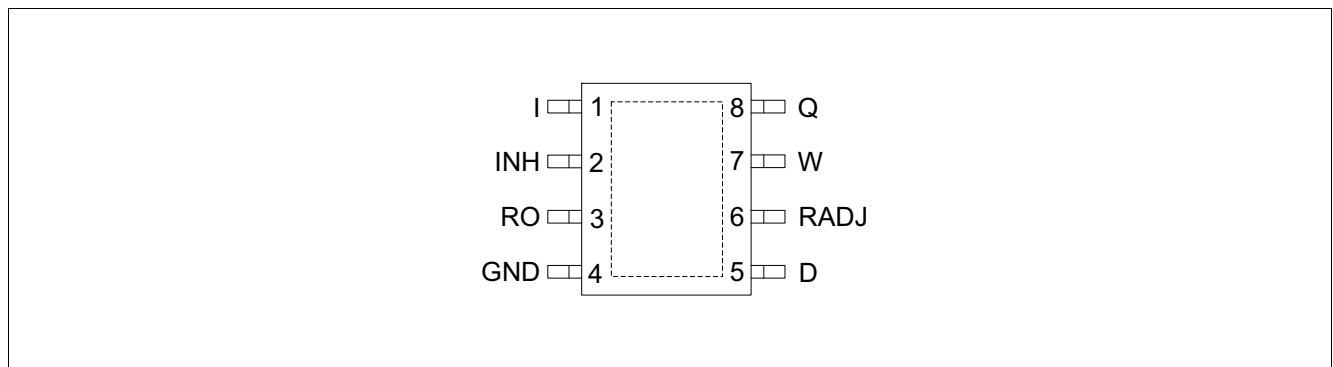


Figure 2 Pin configuration (top view)

Table 1 Pin definition and functions

Pin	Symbol	Function
1	I	Input for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	INH	Inhibit enables/disables the device; connect to I if the this function is not needed
3	RO	Reset Output open-collector output connected to the output via an internal 30kΩ pull-up resistor; leave open if the this function is not needed
4	GND	Ground
5	D	Reset Delay Timing connect a ceramic capacitor to GND for adjusting the reset delay time / watchdog trigger time; leave open if this function is not needed
6	RADJ	Reset Threshold Adjust connect an external voltage divider to adjust the reset switching threshold; connect to GND for using internal threshold
7	W	Watchdog rising edge triggered input for monitoring a microcontroller; connect to GND if this function is not needed
8	Q	Output block to ground with a capacitor close to the IC terminals with a capacitance value $C \geq 22 \mu\text{F}$, $\text{ESR} \leq 3 \Omega$
PAD	–	Exposed Pad attach the exposed pad on package bottom to the heatsink area on circuit board; connect to GND

General product characteristics

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings¹⁾

$T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Input voltage	V_I	- 42	-	45	V	-	P_3.1.1
Input current	I_I	-	-	-	-	Internally limited	
Reset output RO							
Input voltage	V_{RO}	- 0.3	-	42	V	-	P_3.1.2
Input current	I_{RO}	-	-	-	-	Internally limited	
Reset threshold RADJ							
Voltage	V_{RADJ}	- 0.3	-	6	V	-	P_3.1.3
Reset delay D							
Voltage	V_D	- 0.3	-	42	V	-	P_3.1.4
Current	I_D	-	-	-	-	Internally limited	
Output Q							
Voltage	V_Q	0.30	-	7.0	V	-	P_3.1.5
Current	I_Q	-	-	-	-	Internally limited	
Inhibit INH							
Input voltage	V_{INH}	-42	-	45	V	-	P_3.1.6
Input current	I_{INH}	-	-	-	-	Internally limited	
Watchdog W							
Voltage	V_W	-0.3	-	6	V	-	P_3.1.7
Ground GND							
Current	I_{GND}	-0.5	-	-	A	-	P_3.1.8
Temperature							
Junction temperature	T_j	-	-	150	$^\circ\text{C}$	-	P_3.1.9
Storage temperature	T_{stg}	-50	-	150	$^\circ\text{C}$	-	
ESD susceptibility							
Human body model (HBM)	Voltage	-	-	2	kV	²⁾	P_3.1.10
Charged device model (CBM)	Voltage	-	-	1	kV	³⁾	P_3.1.11

1) Not subject to production test, specified by design.

2) ESD HBM test according JEDEC JESD22-A114

3) ESD CDM test according AEC/ESDA ESD-STM5 3.1-1999

General product characteristics

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	5.5	–	45	V	1)	P_3.2.1
Junction temperature	T_j	-40	–	150	°C	–	P_3.2.2

1) Corresponds with characteristics of drop voltage, output current and power description (see diagrams).

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	1) measured to exposed pad	P_3.3.1
Junction to ambient	R_{thJA}	–	45	–	K/W	2)	P_3.3.2
Junction to ambient	R_{thJA}	–	153	–	K/W	footprint only ³⁾	P_3.3.3
Junction to ambient	R_{thJA}	–	64	–	K/W	300 mm ² heatsink area ²⁾	P_3.3.4
Junction to ambient	R_{thJA}	–	55	–	K/W	600 mm ² heatsink area ²⁾	P_3.3.5

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 μm Cu).

Functional description

4 Functional description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

In case the externally scaled down output voltage at the reset adjust input falls below 1.35 V, the external reset delay capacitor CD is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold VDRL, a reset signal occurs at the reset output and is held until the upper threshold VDU is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typically 4.65 V.

- Overload
- Overtemperature
- Reverse polarity

4.1 Choosing external components

The input capacitor C_1 is necessary for compensation of line influences. Using a resistor of approx. 1Ω in series with C_1 , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is ensured at values $C_O \geq 22 \mu\text{F}$ and an ESR of $\leq 3 \Omega$ within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

4.2 Electrical characteristics

Table 5 Electrical characteristics

$V_I = 13.5 \text{ V}$; $V_{\text{INH}} > 3.6 \text{ V}$ $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Normal Operation							
Output voltage	V_Q	4.90	5.00	5.10	V	$5 \text{ mA} \leq I_Q \leq 150 \text{ mA}$; $6 \text{ V} \leq V_I \leq 28 \text{ V}$	P_4.2.1
Output voltage	V_Q	4.90	5.00	5.10	V	$6 \text{ V} \leq V_I \leq 32 \text{ V}$; $I_Q = 100 \text{ mA}$; $T_j = 100^\circ\text{C}$	P_4.2.2
Output current limitation	$I_{Q,\text{max}}$	180	250	400	mA	$V_Q = 4.8 \text{ V}$	P_4.2.3
Current consumption; $I_q = I_I - I_Q$	I_q	–	0	10	μA	$V_{\text{INH}} = 0 \text{ V}$; $T_j \leq 115^\circ\text{C}$	P_4.2.4
Current consumption; $I_q = I_I - I_Q$	I_q	–	0.90	1.30	mA	$I_Q = 0 \text{ mA}$	P_4.2.5
Current consumption; $I_q = I_I - I_Q$	I_q	–	10	18	mA	$I_Q = 150 \text{ mA}$	P_4.2.6
Current consumption; $I_q = I_I - I_Q$	I_q	–	15	24	mA	$I_Q = 150 \text{ mA}$; $V_I = 4.5 \text{ V}$	P_4.2.7
Dropout voltage	V_{dr}	–	0.35	0.50	V	$I_Q = 150 \text{ mA}^{1)}$	P_4.2.8
Load regulation	$\Delta V_{Q,\text{lo}}$	–	–	25	mV	$I_Q = 5 \text{ mA}$ to 150 mA	P_4.2.9

Functional description

Table 5 Electrical characteristics (cont'd)

$V_I = 13.5\text{ V}$; $V_{\text{INH}} > 3.6\text{ V}$ $T_j = -40^\circ\text{C}$ to $+150^\circ\text{C}$; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Line regulation	$\Delta V_{Q,li}$	–	3	25	mV	$V_I = 6\text{ V}$ to 28 V ; $I_Q = 150\text{ mA}$	P_4.2.10
Power supply ripple rejection	$PSRR$	–	54	–	dB	$^2)f_r = 100\text{ Hz}$; $V_r = 0.5\text{ Vpp}$	P_4.2.11

Reset Generator

Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	$V_{\text{RADJ}} = 0\text{ V}$	P_4.2.12
Reset adjust threshold	$V_{\text{RADJ},th}$	1.26	1.36	1.44	V	$3.5\text{ V} \leq V_Q < 5\text{ V}$	P_4.2.13
Reset low voltage	$V_{\text{RO},l}$	–	0.10	0.40	V	$I_{\text{RO}} = 1\text{ mA}$	P_4.2.14
Saturation voltage	$V_{\text{D},sat}$	–	50	110	mV	$V_Q < V_{\text{R},th}$	P_4.2.15
Upper timing threshold	V_{DU}	1.40	1.70	2.20	V	–	P_4.2.16
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.59	V	–	P_4.2.17
Charge current	$I_{\text{D},ch}$	40	60	88	μA	–	P_4.2.18
Reset delay time	t_{rd}	1.3	2.8	4.1	ms	$C_D = 100\text{ nF}$	P_4.2.19
Reset reaction time	t_{rr}	0.5	1.2	4.0	μs	$C_D = 100\text{ nF}$	P_4.2.20

Watchdog

Discharge current	$I_{\text{D},wd}$	4.40	6.25	9.40	μA	$V_D = 1.0\text{ V}$	P_4.2.22
Upper timing threshold	V_{DU}	1.40	1.70	2.20	V	–	P_4.2.24
Lower timing threshold	V_{DWL}	0.20	0.35	0.55	V	–	P_4.2.25
Watchdog trigger time	$T_{\text{WI},tr}$	16	22.5	27	ms	$C_D = 100\text{ nF}$ $V_Q > V_{\text{Q},RT}$	P_4.2.26
Watchdog output low time	$T_{\text{WD},l}$	1.0	2.10	3.50	ms	$C_D = 100\text{ nF}$ $V_Q > V_{\text{Q},RT}$	P_4.2.27
Watchdog period $T_{\text{WI},P} = T_{\text{WD},L} + T_{\text{WI},tr}$	$T_{\text{WD},p}$	17	24.6	30.5	ms	$C_D = 100\text{ nF}$ $V_Q > V_{\text{Q},RT}$	P_4.2.28

Inhibit

Switching voltage	$V_{\text{INH},ON}$	3.6	–	–	V	IC turned on	P_4.2.29
Turn-OFF voltage	$V_{\text{INH},OFF}$	–	–	0.8	V	IC turned off	P_4.2.30
Input current	I_{INH}	5	10	27	μA	$V_{\text{INH}} = 5\text{ V}$	P_4.2.31

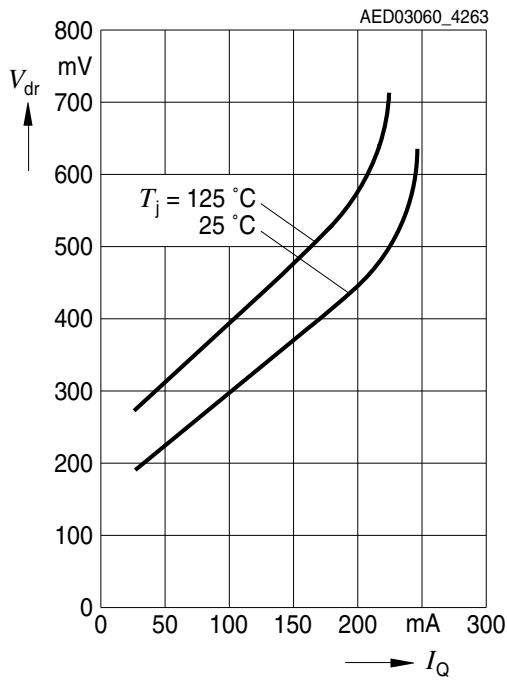
- 1) Drop voltage = $V_i - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input).
- 2) Not subject to production test, specified by design.

Note: The reset output is “low” within the range $V_Q = 1\text{ V}$ to $V_{\text{Q},rt}$

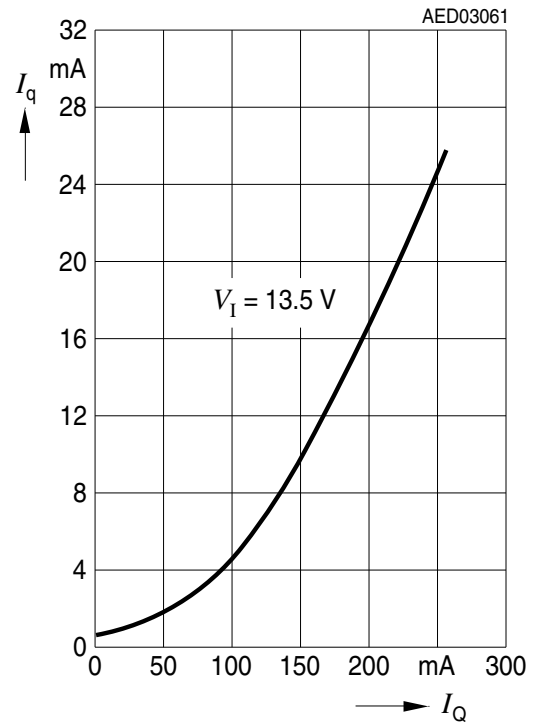
Functional description

4.3 Typical performance characteristics

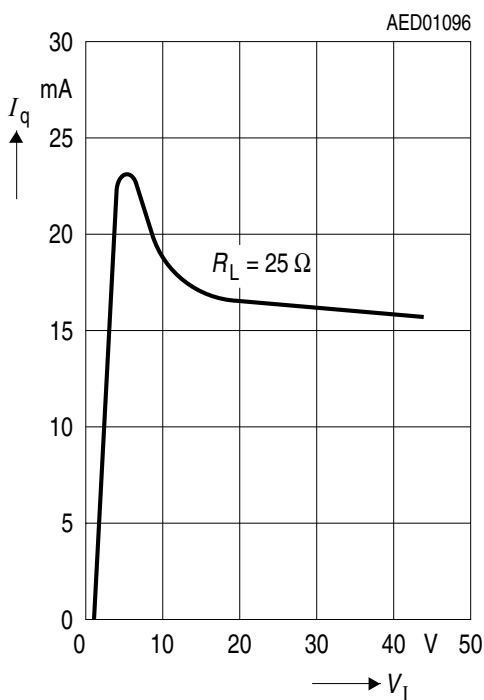
Drop voltage V_{DR} versus output current I_Q



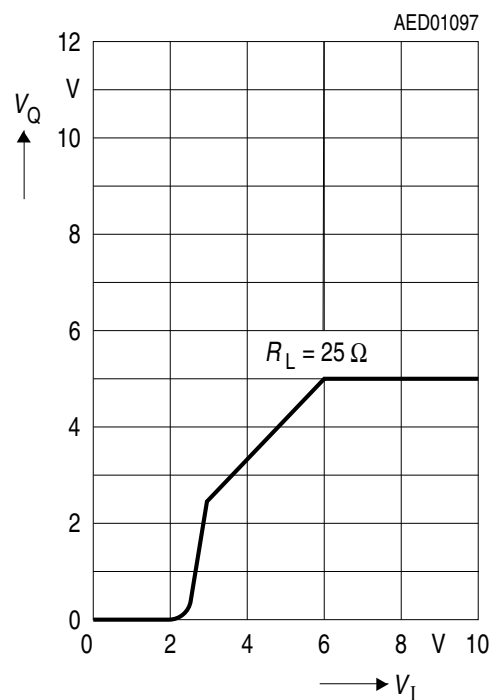
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I

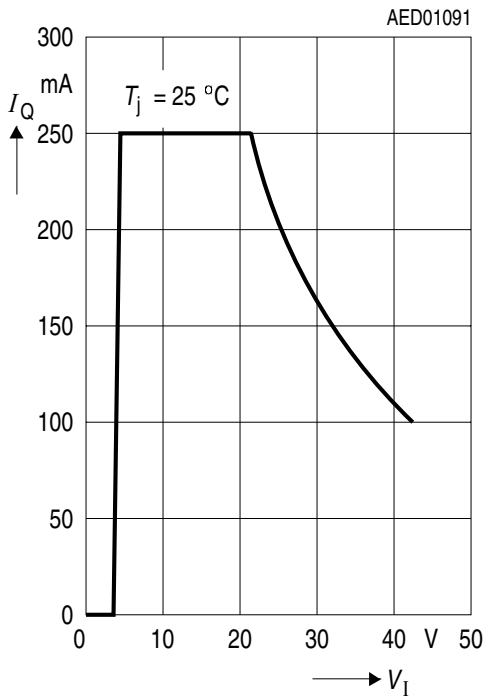


Output voltage V_Q versus input voltage V_I

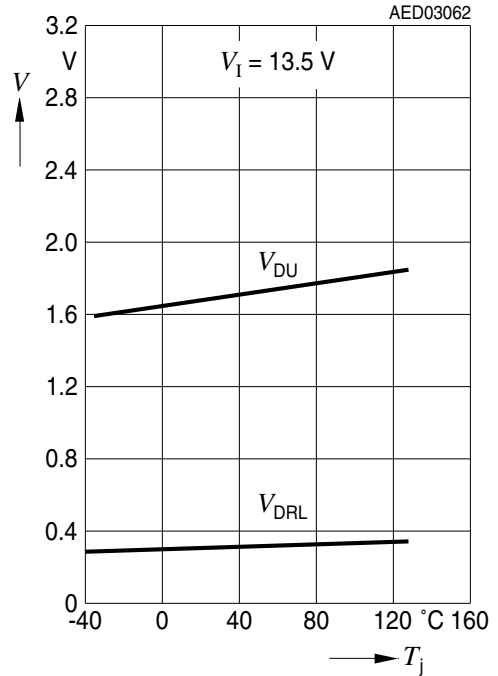


Functional description

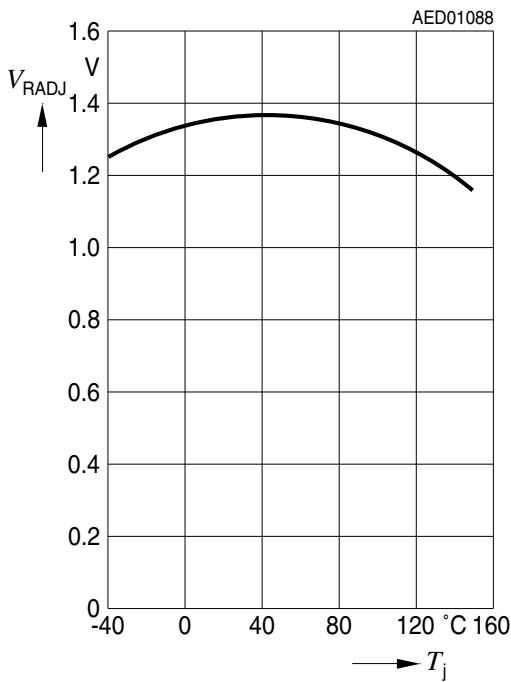
Output current I_Q versus input voltage V_I



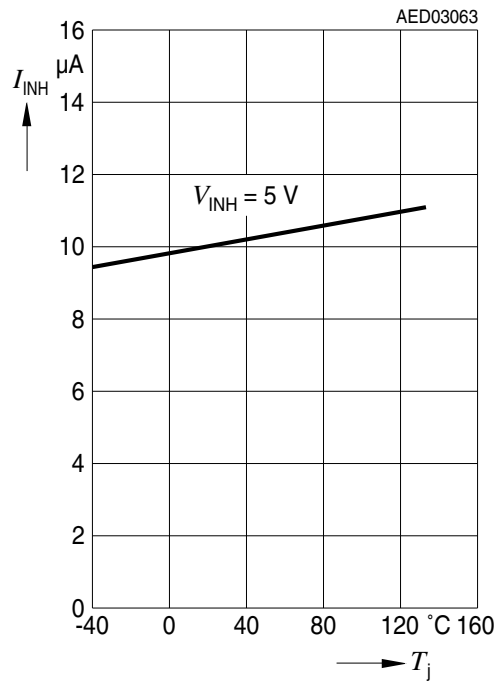
Timing threshold voltage V_{DU} and V_{DRL} versus junction temperature



Reset switching threshold V_{RADJ} versus junction temperature T_j

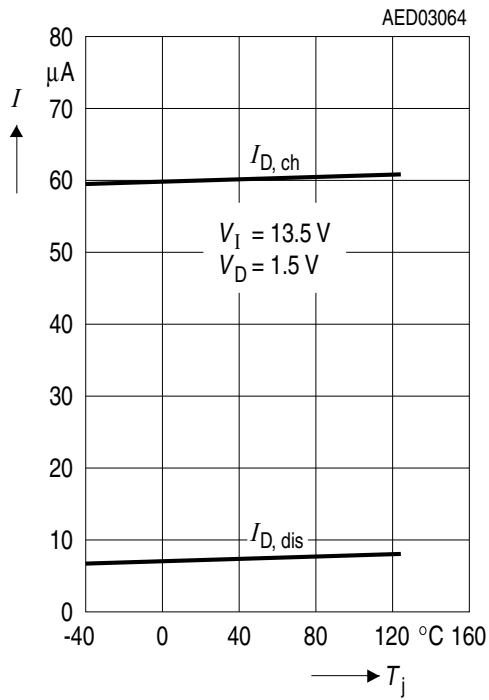


Current consumption of inhibit I_{INH} versus junction temperature T_j

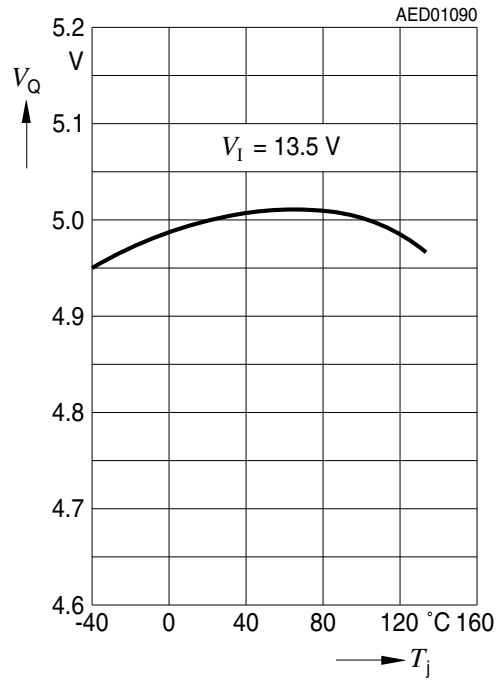


Functional description

Charge current and discharge current $I_{D,ch}$; $I_{D,dis}$ versus junction temperature T_j

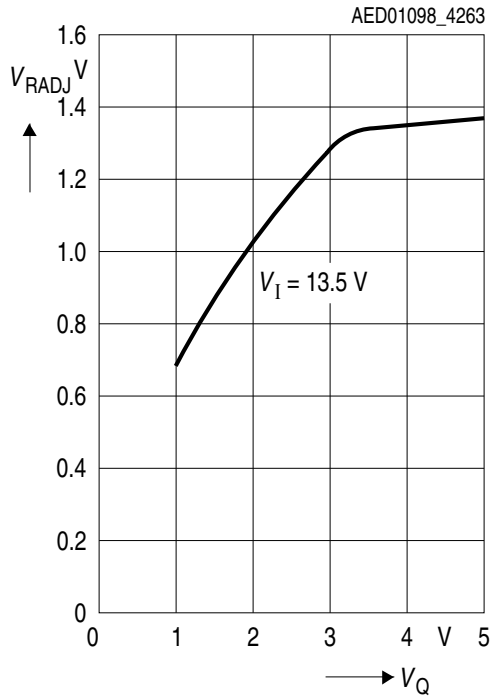


Output voltage V_Q versus junction temperature T_j

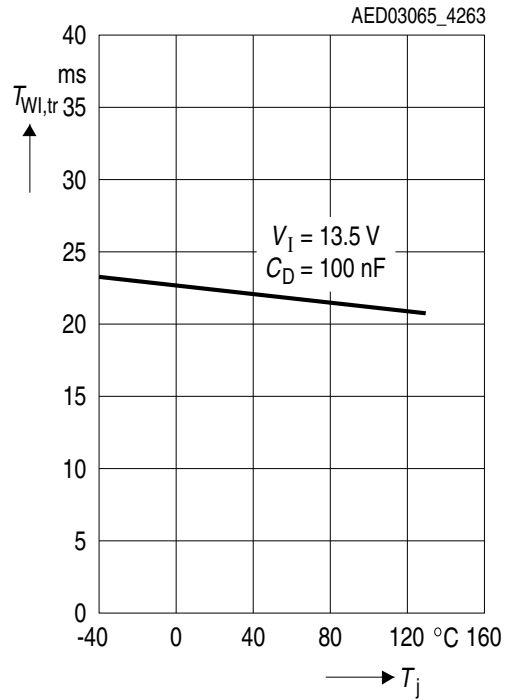


Functional description

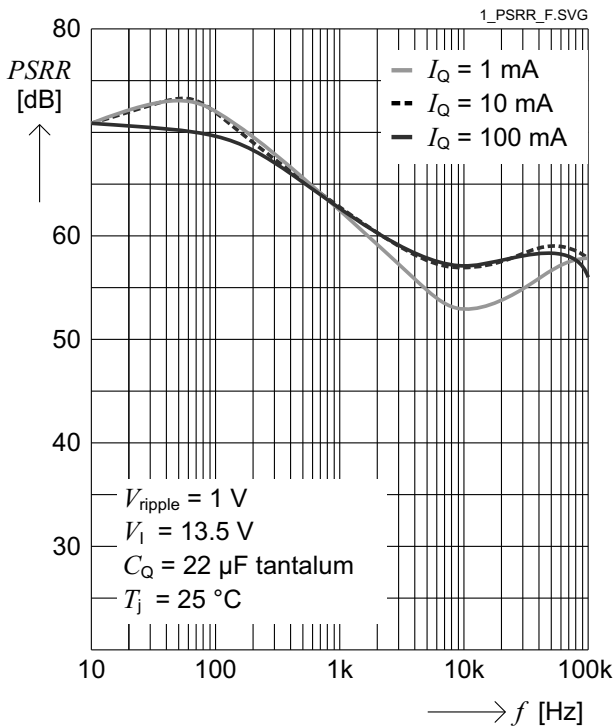
Undervoltage reset adjust threshold V_{RADJ} versus output voltage V_Q



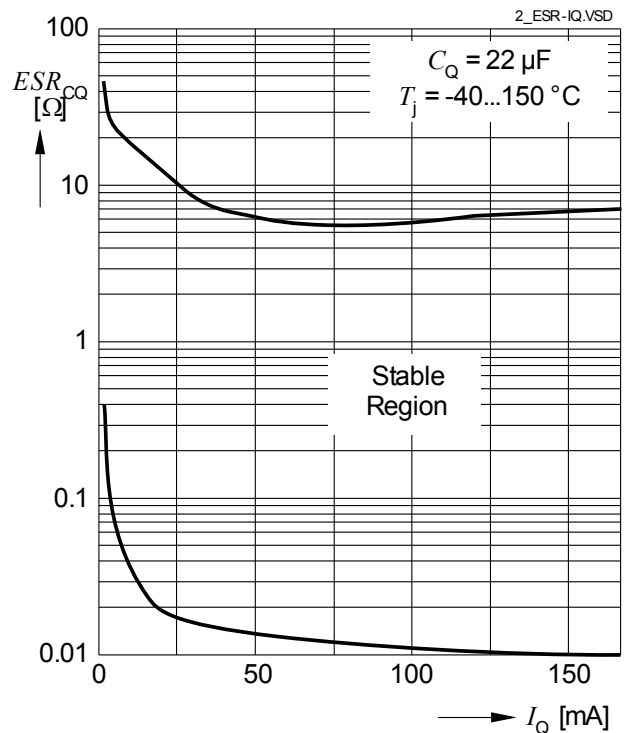
Pulse time $T_{WI,tr}$ versus junction temperature T_j



Power supply ripple rejection $PSRR$ versus ripple frequency f_r



Output capacitor series resistor ESR_{CQ} versus output current I_Q



Application information

5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality condition or quality of the device.

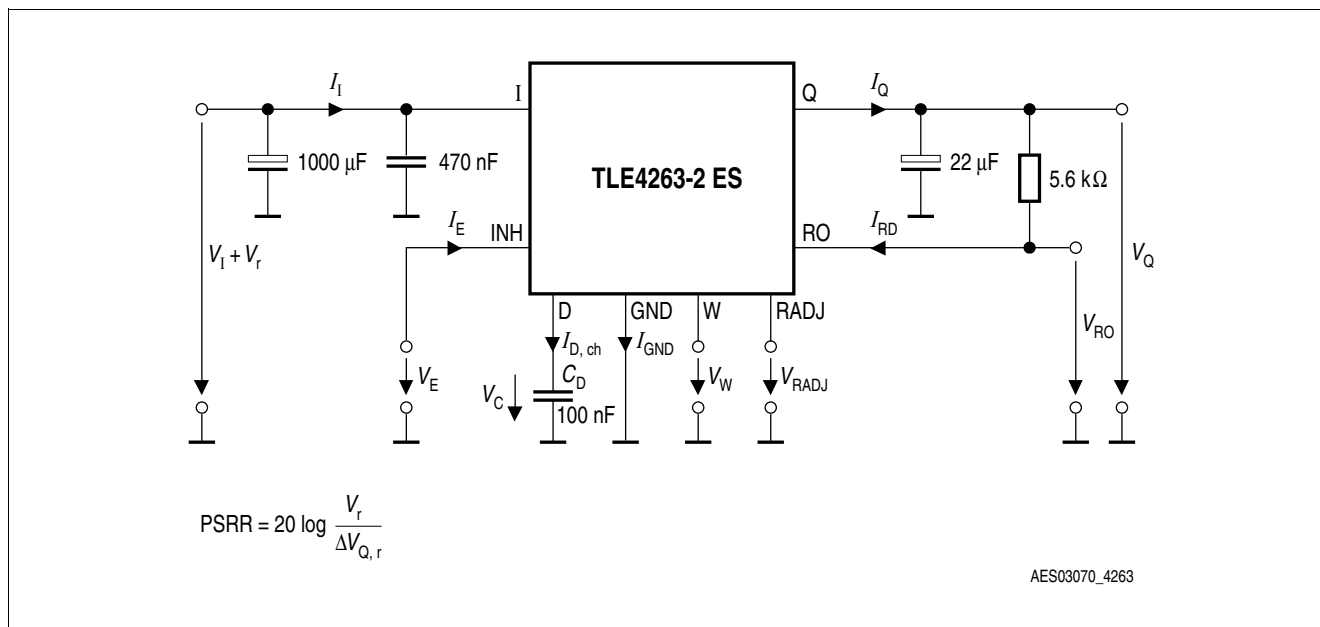


Figure 3 Application circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Application information

5.1 Reset

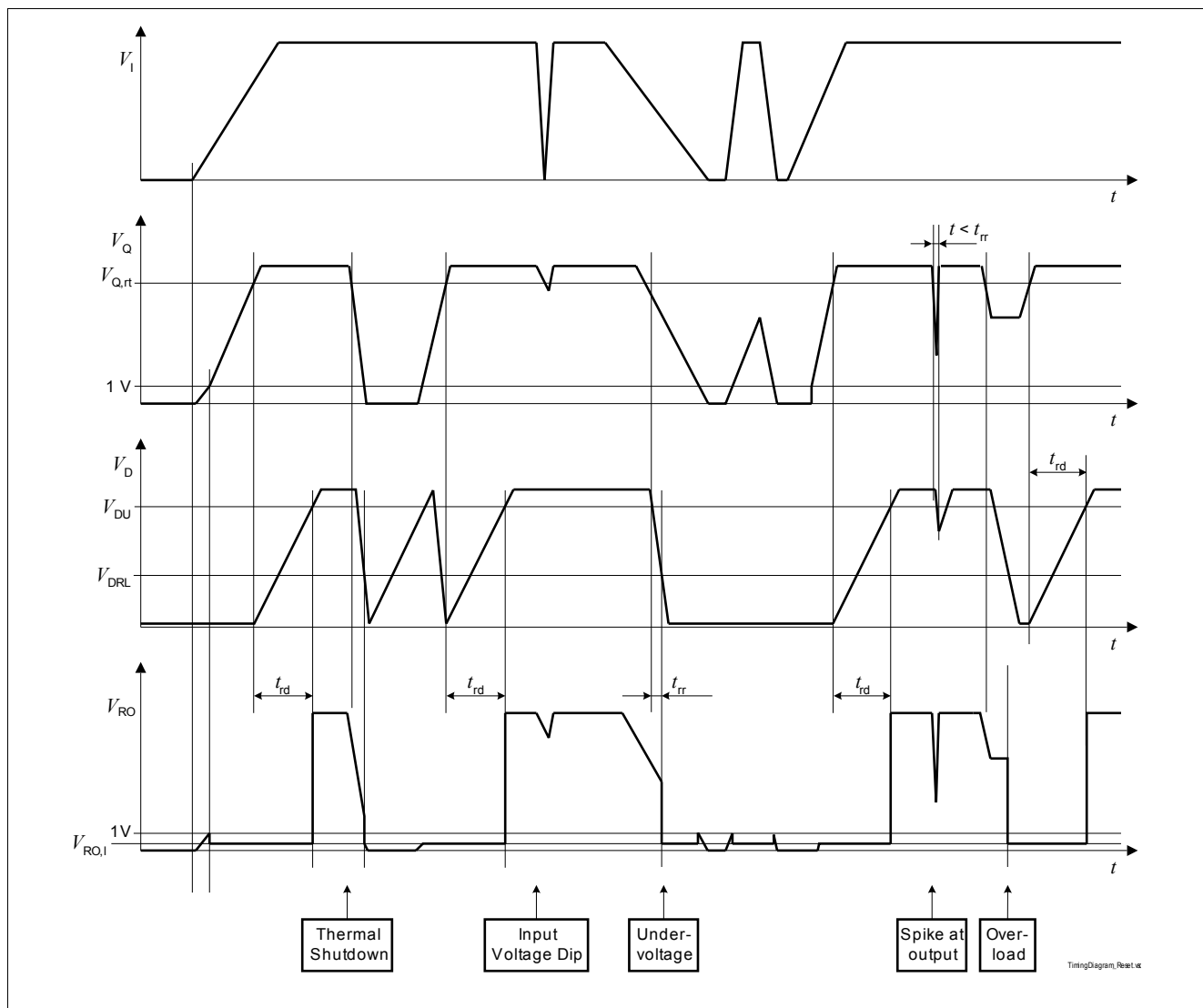


Figure 4 Reset timing diagram

5.2 Power-On Reset Delay Time

If the application needs a power-on reset delay time t_{rd} different from the value given in “Reset Generator” on Page 9, the delay capacitor’s value can be derived from these specified values and the desired power-on delay time:

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100nF \tag{5.1}$$

with:

- C_D : capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd} : power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

Application information

5.3 Reset adjust function

The undervoltage reset switching threshold can be adjusted according to the application’s needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

$$V_{RT,new} = \frac{R_{ADJ,1} + R_{ADJ,2}}{R_{ADJ,2}} \times V_{RADJ,th} \tag{5.2}$$

with

- $V_{RT,new}$: the desired new reset switching threshold
 - R_{ADJ1}, R_{ADJ2} : resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjust switching threshold given in *“Reset Generator” on Page 9*

5.4 Watchdog

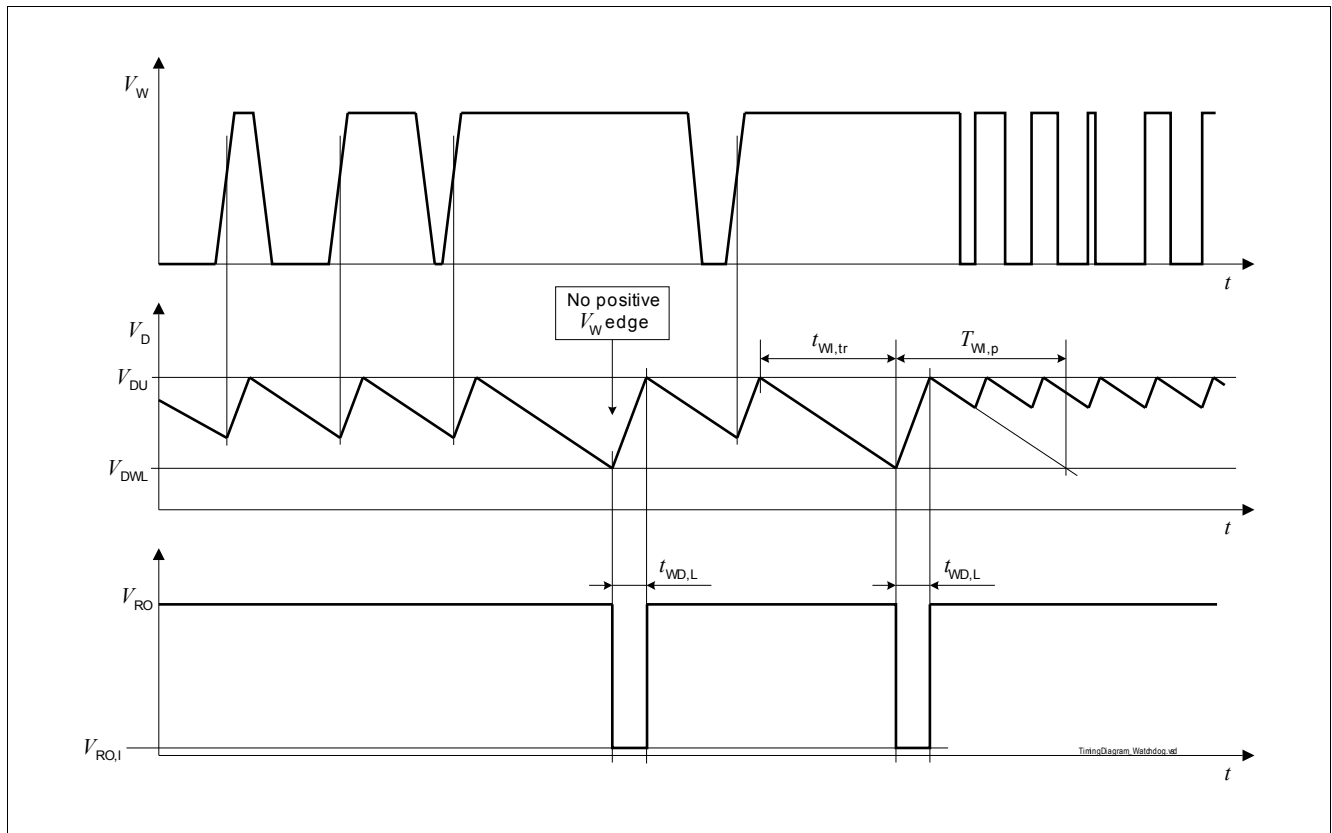


Figure 5 Timing of the Watchdog Function Reset

Application information

Watchdog Timing

The period of the watchdog pulses has to be smaller than the minimum watchdog trigger time which is set by the external reset delay capacitor C_D . Use the following formula for dimensioning C_D :

$$C_D = \frac{T_{Wl,tr,new}}{T_{Wl,tr}} \times 100 \text{ nF} \quad (5.3)$$

with

- C_D : capacitance of the delay capacitor to be chosen
- $T_{Wl,tr,new}$: desired watchdog trigger time
- $T_{Wl,tr}$: watchdog trigger time specified in this data sheet

Package information

6 Package information

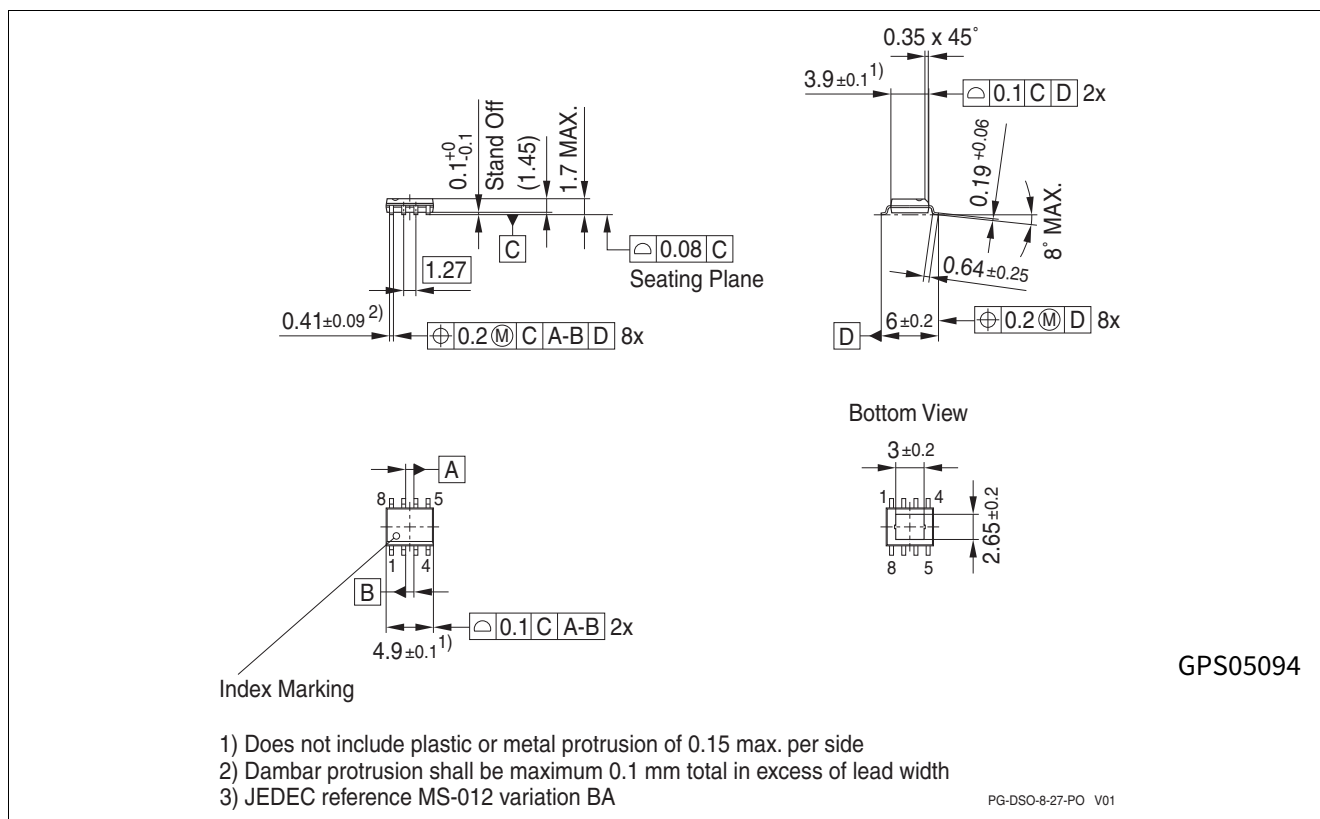


Figure 6 PG-DSO-8 exposed pad (Plastic Dual Small Outline)¹⁾

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

1) Dimension in mm

Revision history

7 Revision history

Revision	Date	Changes
1.1	2019-03-27	Updated layout and structure Editorial changes

Trademarks

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