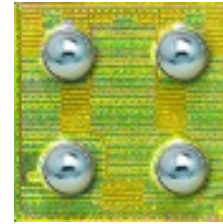
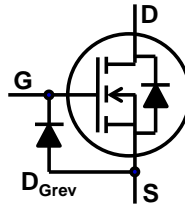


EPC2038 – Enhancement Mode Power Transistor with Integrated Reverse Gate Clamp Diode Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS} , 100V
- Internal Gate Diode
- Maximum $R_{DS(on)}$, 3.3 Ω
- I_D , 0.5 A
- Pb-Free (RoHS Compliant), Halogen Free



EPC2038 eGaN[®] FETs are supplied only in passivated die form with solder balls

Die Size: 0.9 mm x 0.9 mm

Applications:

Synchronous Bootstrap for:

- High Speed DC-DC Conversion
- Wireless Power Transfer
- High Frequency Hard-Switching and Soft-Switching Circuits
- LiDAR/Pulsed Power Applications
- Class-D Audio

MAXIMUM RATINGS

Parameter	Value
Maximum Drain – Source Voltage	100 V
Gate – Source Maximum Voltage Range	-4 V < V_{GS} < 6 V
Continuous Drain Current, ($T_A = 25\text{ }^\circ\text{C}$, $R_{\theta JA} = 120\text{ }^\circ\text{C/W}$)	0.5 A
Maximum Pulsed Drain Current, 25 $^\circ\text{C}$, $T_{pulse} = 300\text{ }\mu\text{s}$	0.5 A
Optimum Temperature Range	-40 $^\circ\text{C}$ < T_J < 150 $^\circ\text{C}$

STATIC CHARACTERISTICS

Parameter	Conditions	Value
Maximum Drain – Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$	0.1 mA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.05\text{ A}$	3.3 Ω
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 0.05\text{ A}$	2.1 Ω
Gate – Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 0.06\text{ mA}$	0.8 V < $V_{GS(TH)}$ < 2.5 V
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	1 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -1\text{ V}$	-0.1 mA
Gate-Source Maximum Forward Voltage	$I_{SG} = 0.2\text{ mA}$, $V_{DS} = 0\text{ V}$	-2.9 V

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated
Specifications are with Substrate shorted to Source

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DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value
C _{ISS} (Input Capacitance)	V _{DS} = 50 V, V _{GS} = 0 V	7 pF
C _{OSS} (Output Capacitance)		1.6 pF
C _{RSS} (Reverse Transfer Capacitance)		0.02 pF
Q _G (Total Gate Charge)	V _{DS} = 50 V, I _D = 0.05 A, V _{GS} = 5 V	44 pC
Q _{GS} (Gate to Source Charge)	V _{DS} = 50 V, I _D = 0.05 A	20 pC
Q _{GD} (Gate to Drain Charge)		4 pC
Q _{G(TH)} (Gate Charge at Threshold)		18 pC
Q _{OSS} (Output Charge)	V _{DS} = 50 V, V _{GS} = 0 V	134 pC
Q _{RR} (Source-Drain Recovery Charge)		0

T_J = 25 °C unless otherwise stated

Specifications are with Substrate shorted to Source

THERMAL CHARACTERISTICS

		TYP	
R _{θJC}	Thermal Resistance, Junction to Case	27	°C/W
R _{θJB}	Thermal Resistance, Junction to Board	91	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1)	100	°C/W

Note 1: R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

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Figure 1: Typical Output Characteristics at 25°C

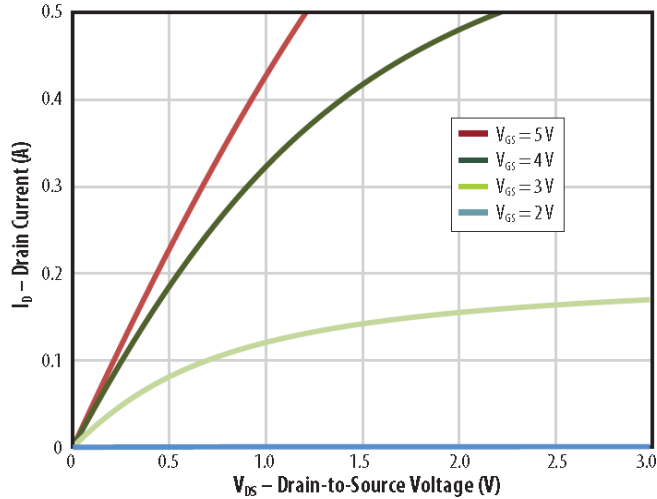


Figure 2: Transfer Characteristics

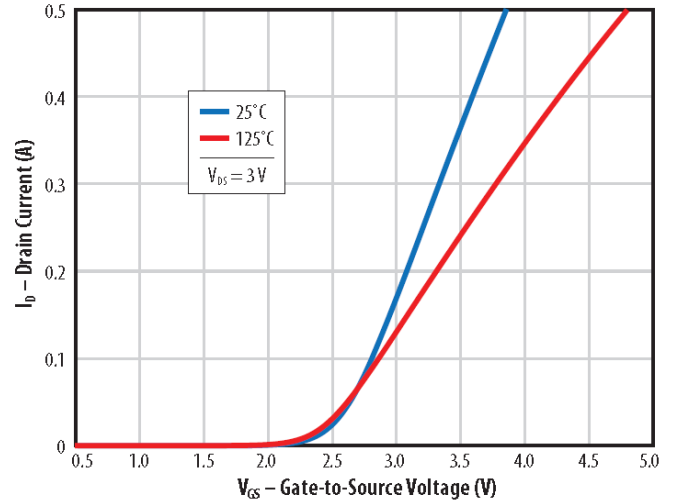


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

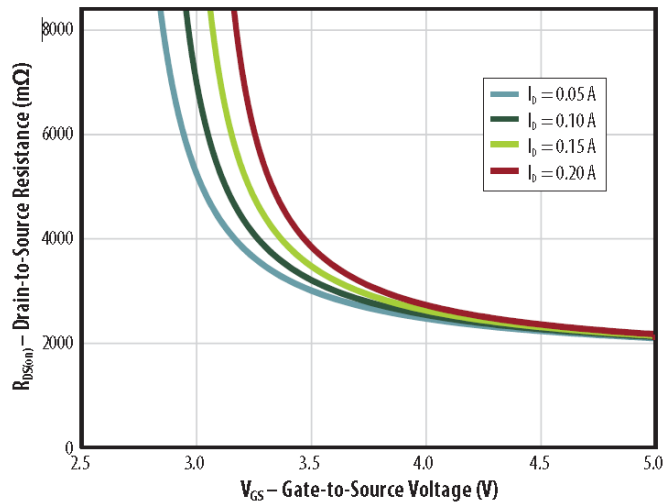


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Drain Temperatures

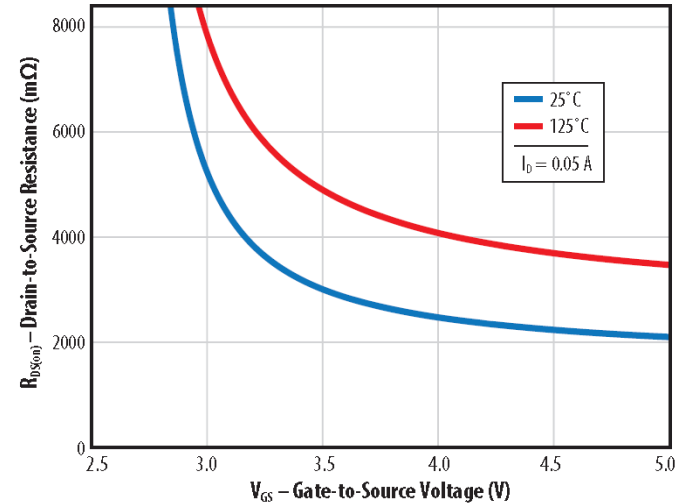


Figure 5a: Capacitance (Linear Scale)

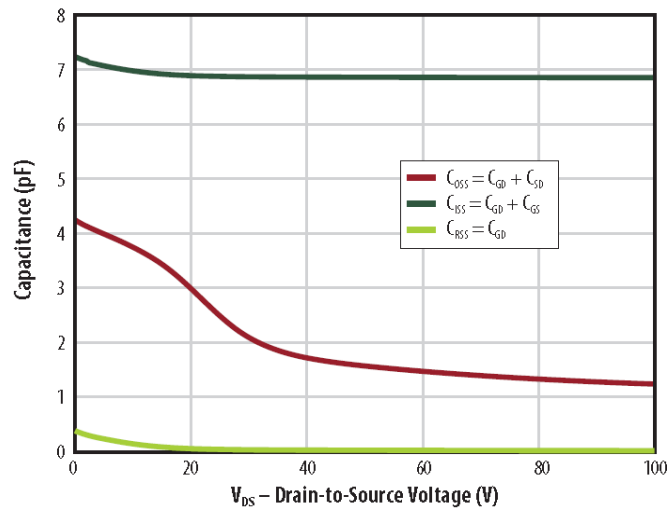
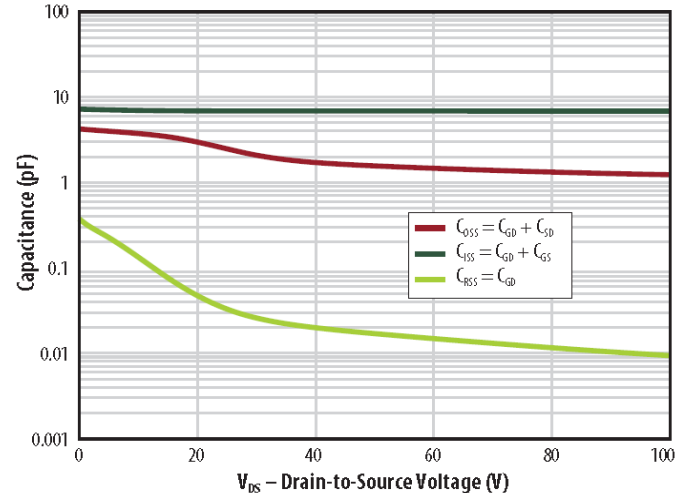


Figure 5b: Capacitance (Log Scale)



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Figure 6: Gate Charge

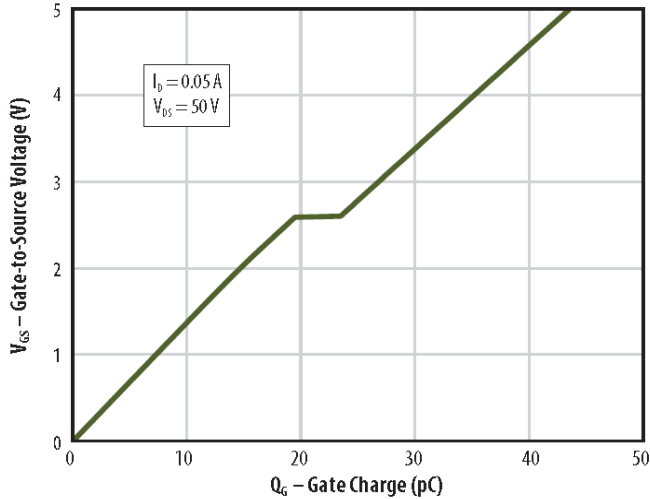


Figure 7: Reverse Drain-Source Characteristics

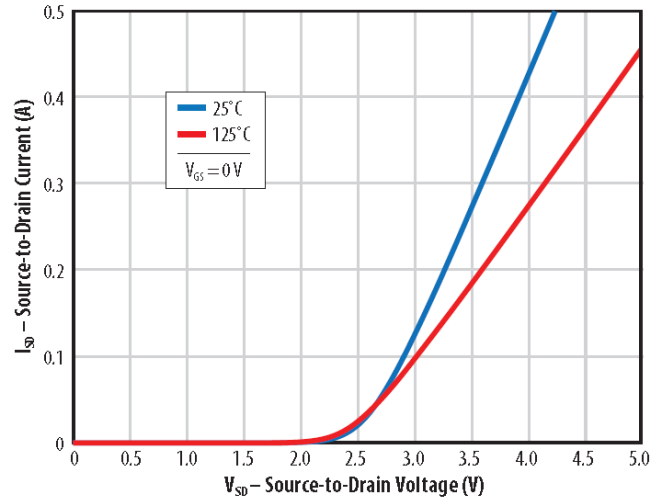


Figure 8: Normalized On Resistance vs. Temperature

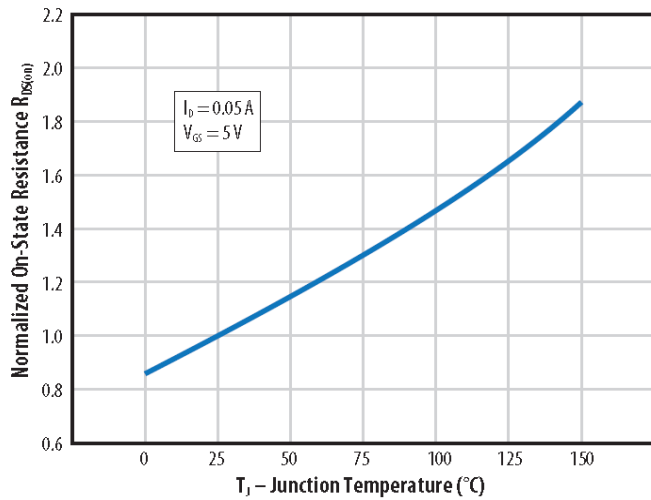


Figure 9: Normalized Threshold Voltage vs. Temperature

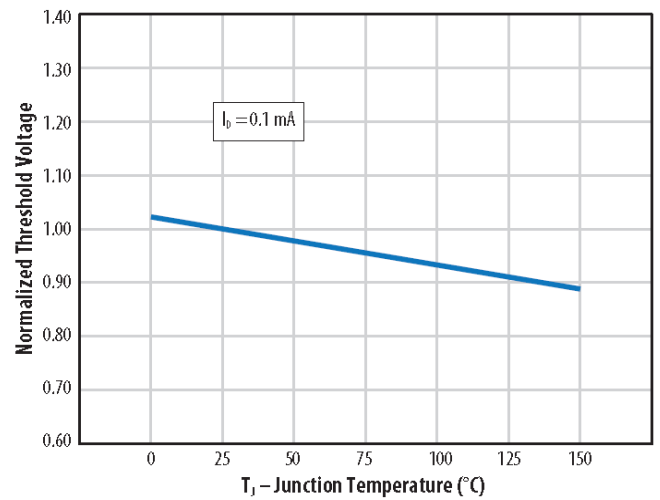
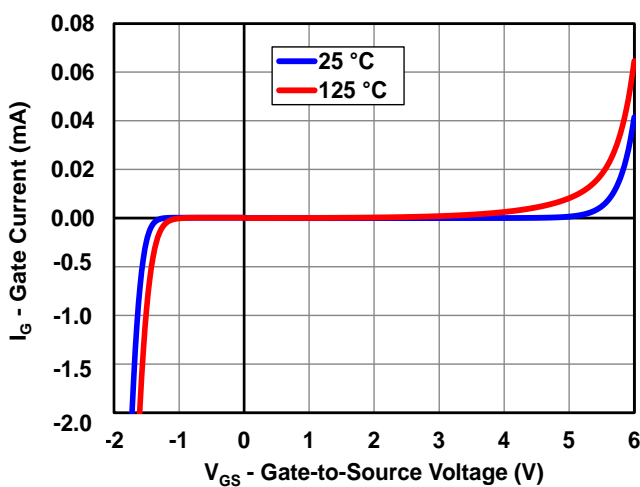


Figure 10: Gate-Source Characteristics



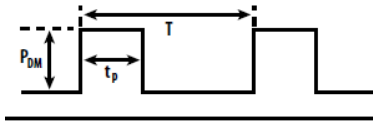
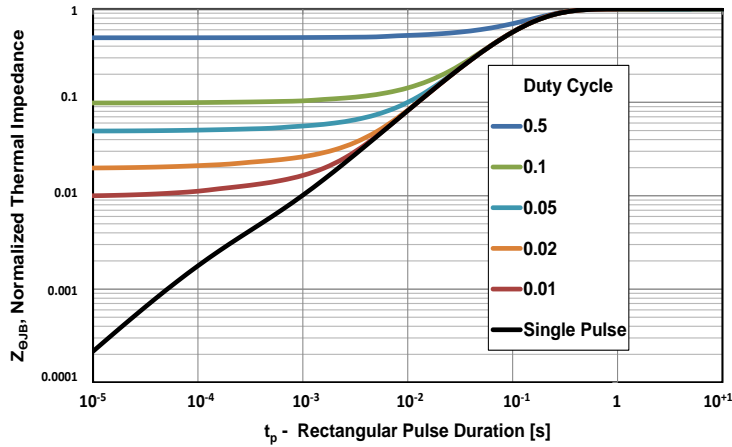
All measurements were done with substrate shorted to source

Figure 11: Transient Thermal Response Curves

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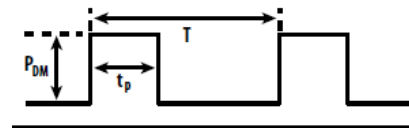
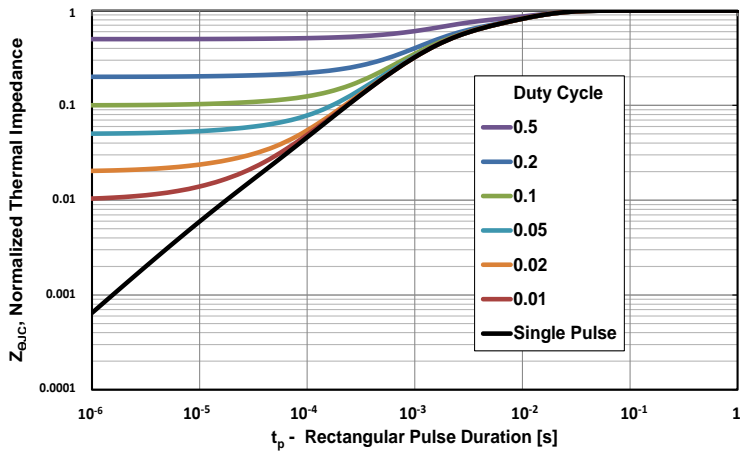
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Junction-to-Board



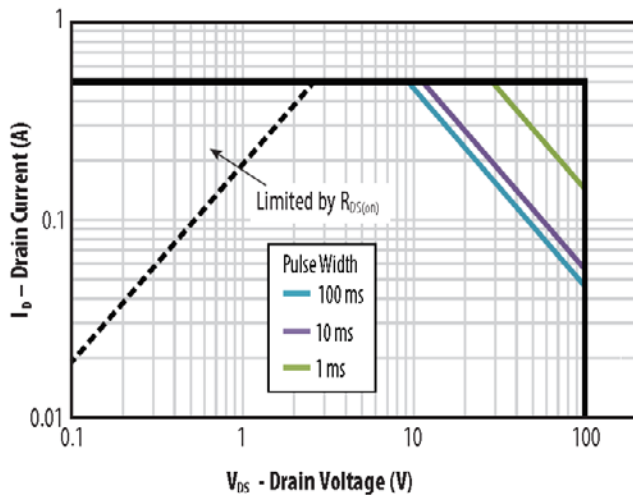
Notes:
 Duty Factor = t_p/T
 Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Junction-to-Case



Notes:
 Duty Factor = t_p/T
 Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 12: Safe Operating Area

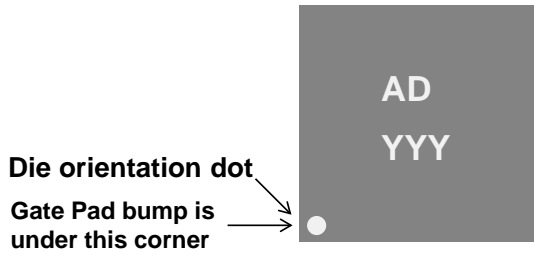


$T_J = \text{Max Rated}, T_C = +25^\circ\text{C}, \text{Single Pulse}$

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DIE MARKINGS

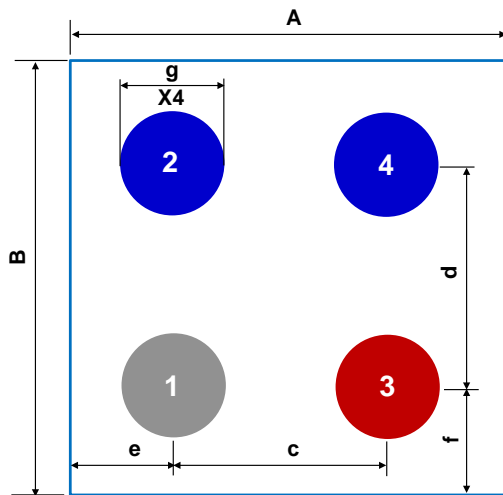


Part Number	Laser Marking	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2038ENGR	AD	YYY

DIE OUTLINE

Solder Bar View

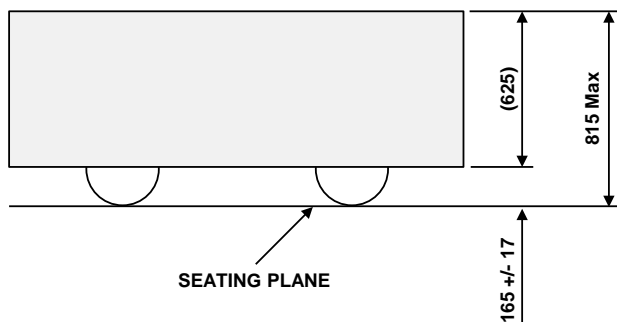
All measurements in micrometers (μm)



Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c	450	450	450
d	450	450	450
e	210	225	240
f	210	225	240
g	187	208	229

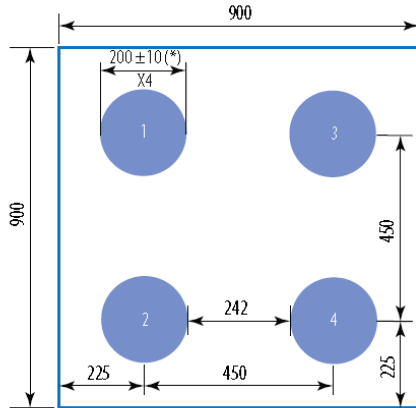
Side View



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RECOMMENDED LAND PATTERN

(Units in μm)



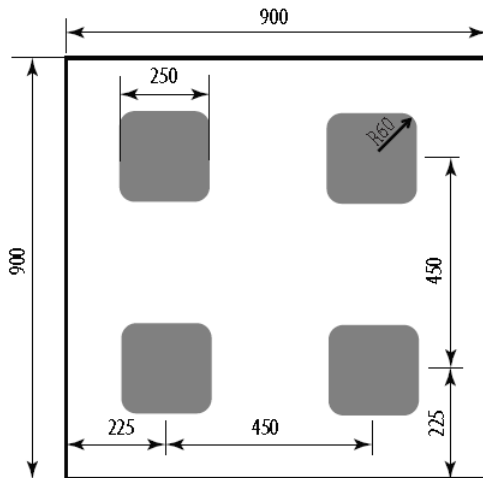
* minimum 190

The land pattern is solder mask defined
Solder mask is $10\ \mu\text{m}$ smaller per side than bump

Pads 1 is Gate;
Pad 3 is Drain;
Pads 2, 4 are Source

RECOMMENDED STENCIL

(Units in μm)



Recommended stencil should be 4mil ($100\ \mu\text{m}$) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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