SDR SDRAM

MT48LC128M4A2 – 32 Meg x 4 x 4 banks
MT48LC64M8A2 – 16 Meg x 8 x 4 banks
MT48LC32M16A2 – 8 Meg x 16 x 4 banks

Features

- PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode
- Auto refresh
  - 64ms, 8192-cycle refresh (commercial and industrial)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply

Options	Marking
• Configurations	
– 128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• Write recovery (^{t}WR)	
– ^{t}WR = 2 CLK[1]	A2
• Plastic package – OCPL[2]	
– 54-pin TSOP II (400 mil) (standard)	TG
– 54-pin TSOP II (400 mil) Pb-free	P
• Timing – cycle time	
– 7.5ns @ CL = 3 (PC133)	-75
– 7.5ns @ CL = 2 (PC133)	-7E[3]
• Self refresh	
– Standard	None
– Low power	L[4]
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Revision	:C

Notes:
1. See technical note TN-48-05 on Micron's Web site.
2. Off-center parting line.
3. Available on x4 and x8 only.
4. Contact Micron for availability.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-7E	143 MHz	–	5.4ns	1.5ns	0.8ns
-75	133 MHz	–	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	–	1.5ns	0.8ns
-75	100 MHz	6ns	–	1.5ns	0.8ns

Table 2: Address Table

Parameter	32 Meg x 4	32 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row addressing	8K A[12:0]	8K A[12:0]	8K A[12:0]
Bank addressing	4 BA[1:0]	4 BA[1:0]	4 BA[1:0]
Column addressing	4K A[9:0], A11, A12	2K A[9:0], A11	1K A[9:0]

Table 3: 512Mb SDR Part Numbering

Part Numbers	Architecture	Package
MT48LC128M4A2P	128 Meg x 4	54-pin TSOP II
MT48LC128M4A2TG	128 Meg x 4	54-pin TSOP II
MT48LC64M8A2P	64 Meg x 8	54-pin TSOP II
MT48LC64M8A2TG	64 Meg x 8	54-pin TSOP II
MT48LC32M16A2P	32 Meg x 16	54-pin TSOP II
MT48LC32M16A2TG	32 Meg x 16	54-pin TSOP II

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General Description

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA[1:0] select the bank; A[12:0] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 512Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagrams

Figure 1: 128 Meg x 4 Functional Block Diagram

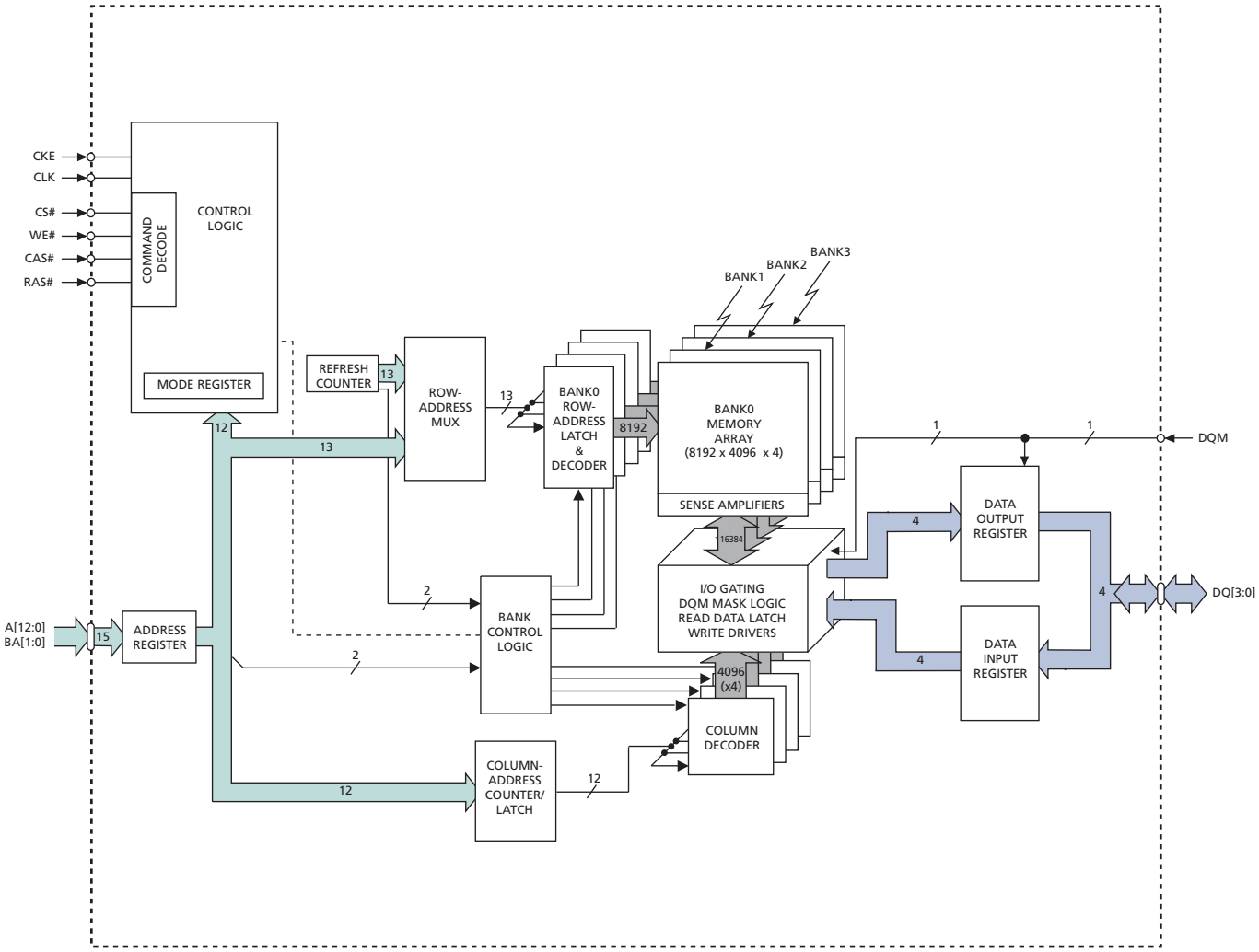


Figure 2: 64 Meg x 8 Functional Block Diagram

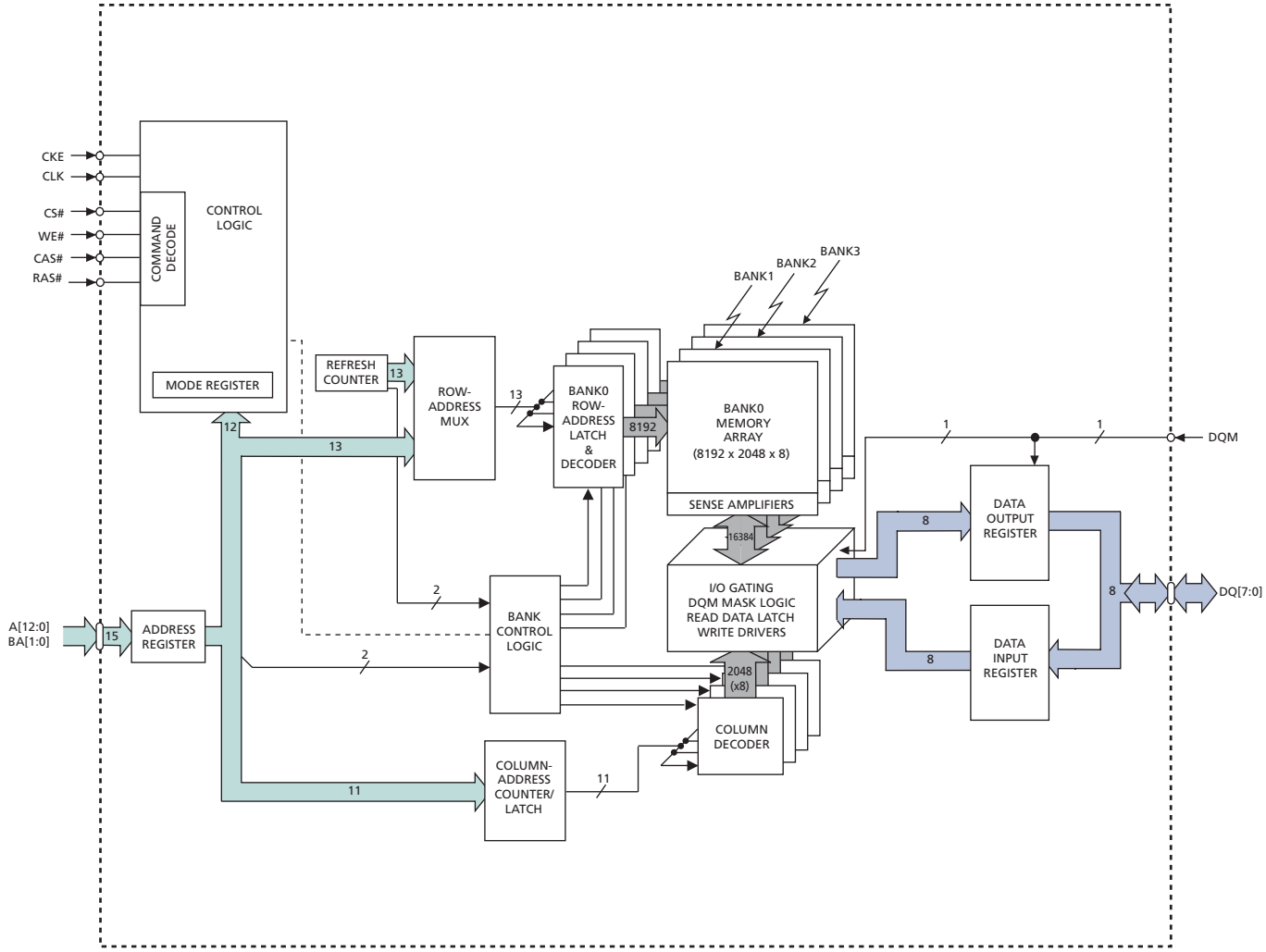
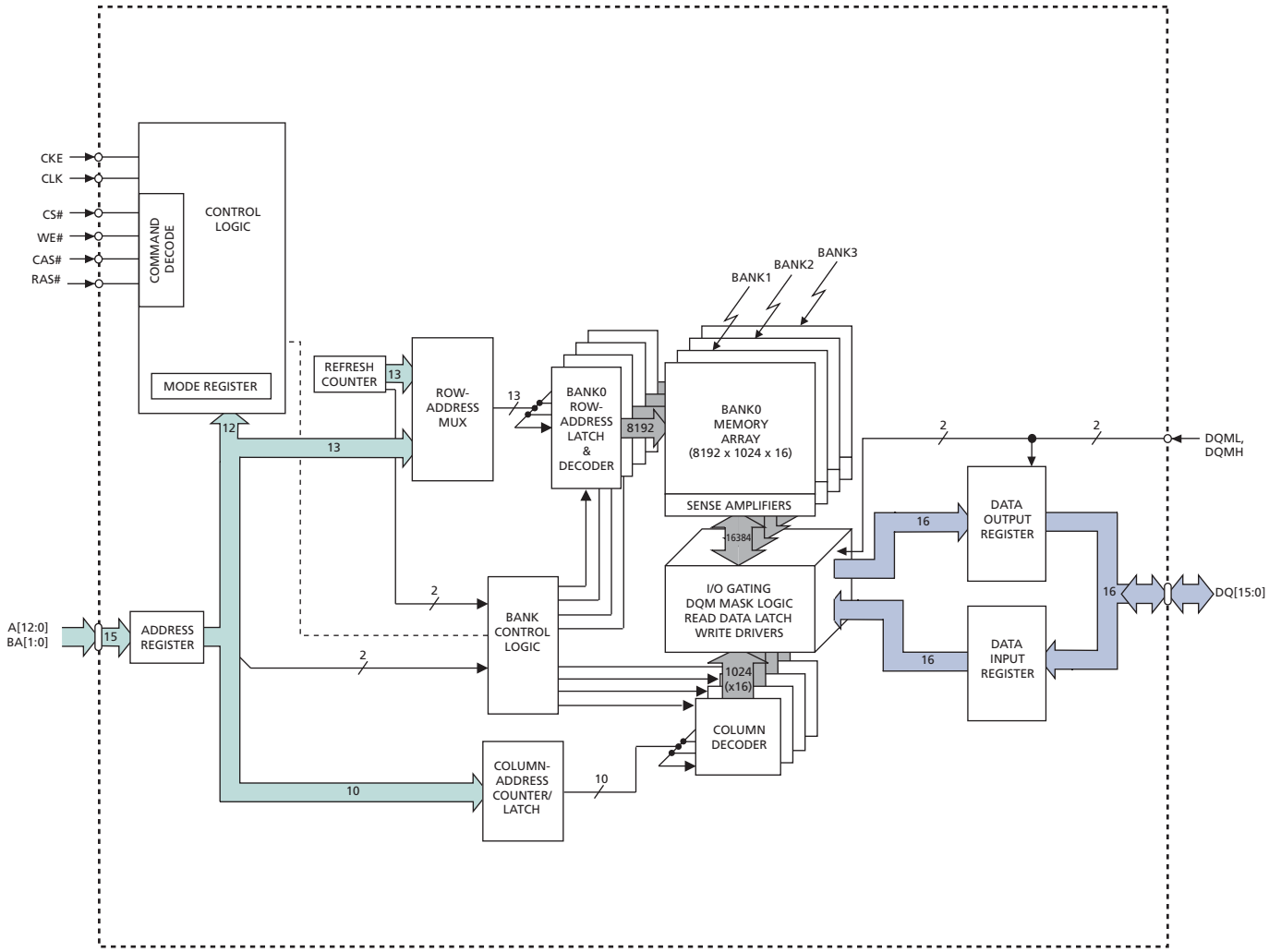
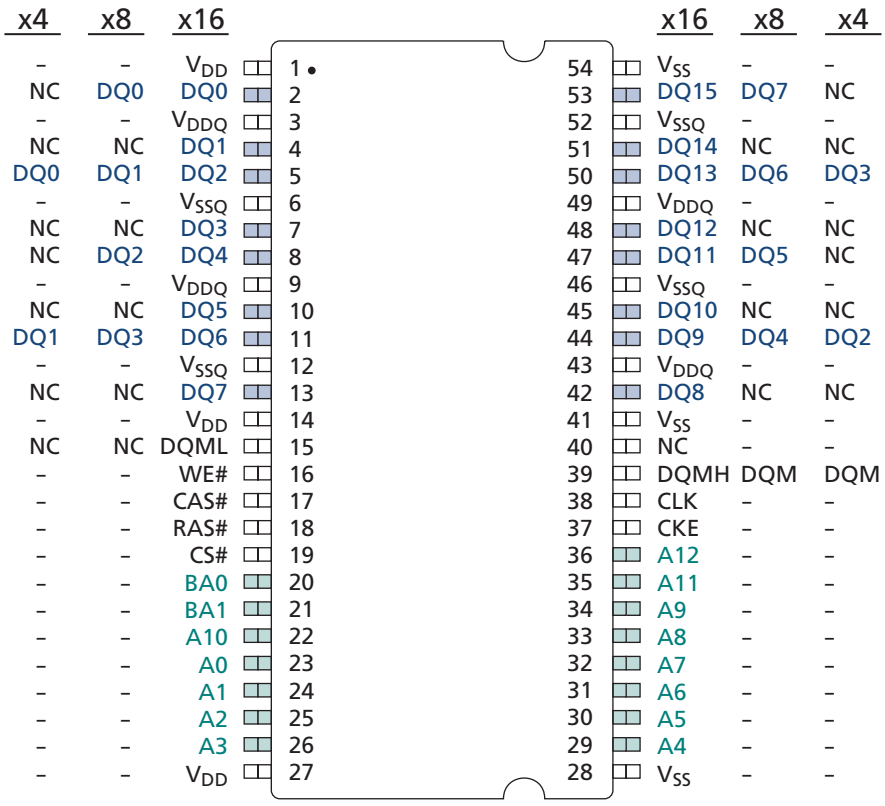


Figure 3: 32 Meg x 16 Functional Block Diagram



Pin and Ball Assignments and Descriptions

Figure 4: 54-Pin TSOP (Top View)



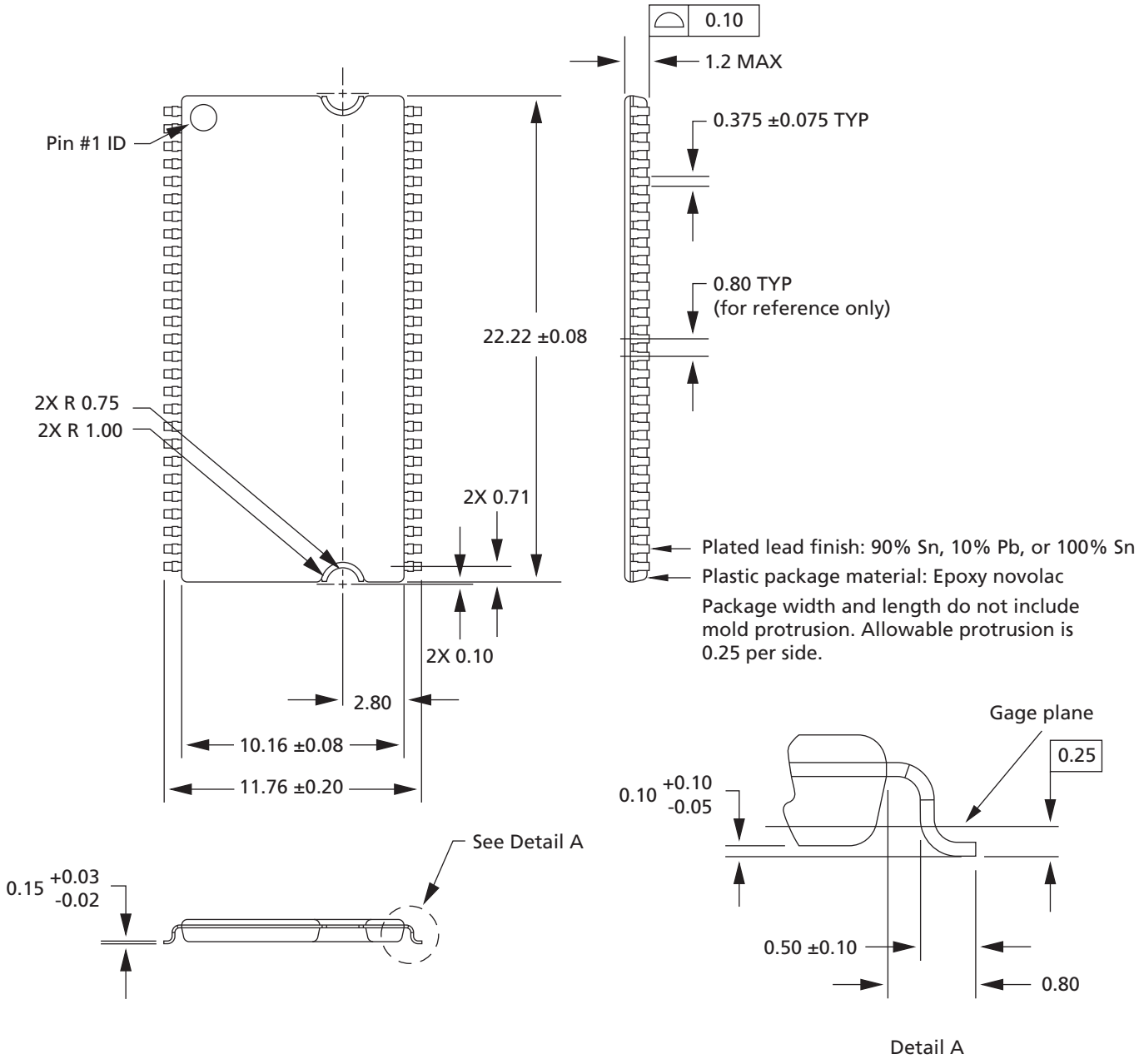
Notes:
1. The # symbol indicates that the signal is active LOW. A dash (-) indicates that the x8 and x4 pin function is the same as the x16 pin function.
2. Package may or may not be assembled with a location notch.

Table 4: Pin and Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while CS# is HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
x4, x8: DQM x16: DQML, DQMH LDQM, UDQM (54-ball)	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ[7:0], and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same state when referenced as DQM.
BA[1:0]	Input	Bank address input(s): BA[1:0] define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0], A11, and A12 for x4; A[9:0] and A11 for x8; A[9:0] for x16; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
x16: DQ[15:0]	I/O	Data input/output: Data bus for x16 (pins 4, 7, 10, 13, 15, 42, 45, 48, and 51 are NC for x8; and pins 2, 4, 7, 8, 10, 13, 15, 42, 45, 47, 48, 51, and 53 are NC for x4).
x8: DQ[7:0]	I/O	Data input/output: Data bus for x8 (pins 2, 8, 47, 53 are NC for x4).
x4: DQ[3:0]	I/O	Data input/output: Data bus for x4.
V_{DDQ}	Supply	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	DQ ground: DQ ground to the die for improved noise immunity.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground.
NC	–	These should be left unconnected.

Package Dimensions

Figure 5: 54-Pin Plastic TSOP (400 mil) – Package Codes TG/P



Notes:
1. All dimensions are in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. 2X means the notch is present in two locations (both ends of the device).
4. Package may or may not be assembled with a location notch.

Temperature and Thermal Impedance

It is imperative that the SDRAM device's temperature specifications, shown in Table 6 (page 14), be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in Table 6 (page 14) for the applicable die revision and packages being made available. These thermal impedance values vary according to the density, package, and particular design used for each device.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed in Table 6 (page 14). To ensure the compatibility of current and future designs, contact Micron Applications Engineering to confirm thermal impedance values.

The SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Temperature Limits

Parameter		Symbol	Min	Max	Unit	Notes
Operating case temperature	Commercial	T_C	0	80	°C	1, 2, 3, 4
	Industrial		–40	90		
Junction temperature	Commercial	T_J	0	85	°C	3
	Industrial		–40	95		
Ambient temperature	Commercial	T_A	0	70	°C	3, 5
	Industrial		–40	85		
Peak reflow temperature		T_{PEAK}	–	260	°C	

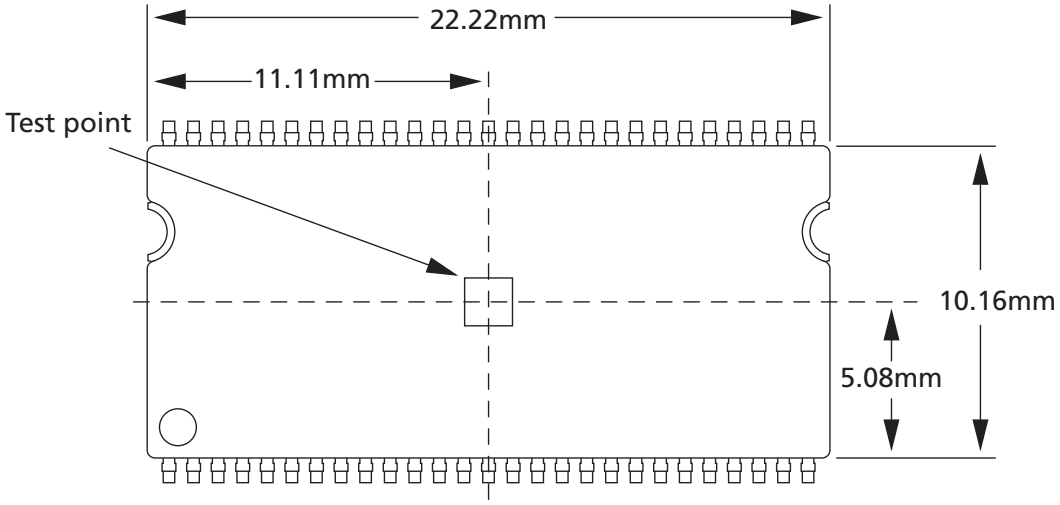
Notes:
1. MAX operating case temperature, TC, is measured in the center of the package on the top side of the device, as shown in Figure 6 (page 14).
2. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
3. All temperature specifications must be satisfied.
4. The case temperature should be measured by gluing a thermocouple to the top-center of the component. This should be done with a 1mm bead of conductive epoxy, as defined by the JEDEC EIA/JESD51 standards. Take care to ensure that the thermocouple bead is touching the case.
5. Operating ambient temperature surrounding the package.

Table 6: Thermal Impedance Simulated Values

Die Revision	Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)
D	54-pin TSOP	2-layer	62.6	48.4	44.2	19.2	6.7
		4-layer	39.2	32.3	30.6	19.3	

Notes:
1. For designs expected to last beyond the die revision listed, contact Micron Applications Engineering to confirm thermal impedance values.
2. Thermal resistance data is sampled from multiple lots, and the values should be viewed as typical.
3. These are estimates; actual results may vary.

Figure 6: Example: Temperature Test Point Location, 54-Pin TSOP (Top View)



Note:
1. Package may or may not be assembled with a location notch.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Unit	Notes
Voltage on V_{DD}/V_{DDQ} supply relative to V_{SS}	V_{DD}/V_{DDQ}	–1	+4.6	V	1
Voltage on inputs, NC, or I/O balls relative to V_{SS}	V_{IN}	–1	+4.6		
Storage temperature (plastic)	T_{STG}	–55	+155	°C	
Power dissipation	–	–	1	W	

Note: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 8: DC Electrical Characteristics and Operating Conditions

Notes 1–3 apply to all parameters and conditions; V_{DD}/V_{DDQ} = +3.3V ±0.3V

Parameter/Condition		Symbol	Min	Max	Unit	Notes
Supply voltage		V_{DD}, V_{DDQ}	3	3.6	V	
Input high voltage: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	4
Input low voltage: Logic 0; All inputs		V_{IL}	–0.3	+0.8	V	4
Output high voltage: I_{OUT} = –4mA		V_{OH}	2.4	–	V	
Output low voltage: I_{OUT} = 4mA		V_{OL}	–	0.4	V	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)		I_L	–5	5	µA	
Output leakage current: DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ}		I_{OZ}	–5	5	µA	
Operating temperature:	Commercial	T_A	0	+70	˚C	
	Industrial	T_A	–40	+85	˚C	

Notes:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), and –40°C ≤ TA ≤ +105°C (automotive)).
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. V_{IH} overshoot: $V_{IH,max}$ = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: $V_{IL,min}$ = –2V for a pulse width ≤3ns.

Table 9: Capacitance

Note 1 applies to all parameters and conditions

Package	Parameter	Symbol	Min	Max	Unit	Notes
TSOP "TG" package	Input capacitance: CLK	C_{L1}	2.5	3.5	pF	2
	Input capacitance: All other input-only balls	C_{L2}	2.5	3.8	pF	3
	Input/output capacitance: DQ	C_{L0}	4	6	pF	4

Notes:
1. This parameter is sampled. V_{DD}, V_{DDQ} = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
2. PC100 specifies a maximum of 4pF.
3. PC100 specifies a maximum of 5pF.
4. PC100 specifies a maximum of 6.5pF.
5. PC133 specifies a minimum of 2.5pF.
6. PC133 specifies a minimum of 2.5pF.
7. PC133 specifies a minimum of 3.0pF.

Electrical Specifications – I_{DD} Parameters

Table 10: I_{DD} Specifications and Conditions (-7E, -75)

Notes 1–5 apply to all parameters and conditions; V_{DD}/V_{DDQ} = +3.3V ±0.3V

Parameter/Condition		Symbol	Max		Unit	Notes
			-7E	-75		
Operating current: Active mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}	120	110	mA	6, 9, 10, 13
Standby current: Power-down mode; All banks idle; CKE = LOW		I_{DD2}	3.5	3.5	mA	13
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}	45	45	mA	6, 8, 10, 13
Operating current: Burst mode; Page burst; READ or WRITE; All banks active		I_{DD4}	125	115	mA	6, 9, 10, 13
Auto refresh current: CKE = HIGH; CS# = HIGH	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	255	255	mA	6, 8, 9, 10, 13, 14
	^{t}RFC = 7.813µs	I_{DD6}	6	6	mA	
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD7}	6	6	mA	
	Low power (L)	I_{DD7}	3	3	mA	7

Notes:
1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured; (0°C ≤ TA ≤ +70°C (commercial), –40°C ≤ TA ≤ +85°C (industrial), and –40°C ≤ TA ≤ +105°C (automotive)).
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC operating and I_{DD} test conditions have V_{IL} = 0V and V_{IH} = 3.0V using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from $V_{IL,\ max}$ and $V_{IH,min}$ and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
5. I_{DD} specifications are tested after the device is properly initialized.
6. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
7. Enables on-chip refresh and address counters.
8. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
9. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
10. Address transitions average one transition every two clocks.
11. PC100 specifies a maximum of 4pF.
12. PC100 specifies a maximum of 5pF.
13. For -75, CL = 3 and tCK = 7.5ns; for -7E, CL = 2 and tCK = 7.5ns.
14. CKE is HIGH during REFRESH command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

Electrical Specifications – AC Operating Conditions

Table 11: Electrical Characteristics and Recommended AC Operating Conditions (-7E, -75)

Notes 1, 2, 4, 5, 7, and 20 apply to all parameters and conditions

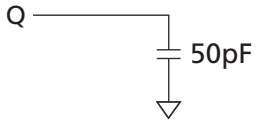
Parameter		Symbol	-7E		-75		Unit	Notes
			Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	tAC(3)	–	5.4	–	5.4	ns	18
	CL = 2	tAC(2)	–	5.4	–	6		
Address hold time		tAH	0.8	–	0.8	–	ns	
Address setup time		tAS	1.5	–	1.5	–	ns	
CLK high-level width		tCH	2.5	–	2.5	–	ns	
CLK low-level width		tCL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	tCK(3)	7	–	7.5	–	ns	14
	CL = 2	tCK(2)	7.5	–	10	–		
CKE hold time		tCKH	0.8	–	0.8	–	ns	
CKE setup time		tCKS	1.5	–	1.5	–	ns	21
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	0.8	–	0.8	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	1.5	–	1.5	–	ns	
Data-in hold time		tDH	0.8	–	0.8	–	ns	
Data-in setup time		tDS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	tHZ(3)	–	5.4	–	5.4	ns	6
	CL = 2	tHZ(2)	–	5.4	–	6	ns	
Data-out Low-Z time		tLZ	1	–	1	–	ns	
Data-out hold time (load)		tOH	2.7	–	2.7	–	ns	
Data-out hold time (no load)		tOH*n*	1.8	–	1.8	–	ns	19
ACTIVE-to-PRECHARGE command		tRAS	37	120,000	44	120,000	ns	
ACTIVE-to-ACTIVE command period		tRC	60	–	66	–	ns	23
ACTIVE-to-READ or WRITE delay		tRCD	15	–	20	–	ns	
Refresh period (8192 rows)		tREF	–	64	–	64	ms	
AUTO REFRESH period		tRFC	66	–	66	–	ns	
PRECHARGE command period		tRP	15	–	20	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		tRRD	14	–	15	–	tCK	
Transition time		tT	0.3	1.2	0.3	1.2	ns	3
WRITE recovery time		tWR	1 CLK + 7ns	–	1 CLK + 7.5ns	–	ns	15
			14	–	15	–		16
Exit SELF REFRESH-to-ACTIVE command		tXSR	67	–	75	–	ns	12

Table 12: AC Functional Characteristics (-7E, -75)

Notes 1–5 and note 7 apply to all parameters and conditions

Parameter		Symbol	-7E	-75	Unit	Notes
Last data-in to burst STOP command		tBDL	1	1	tCK	11
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	11
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	11
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	8
Data-in to ACTIVE command		tDAL	4	5	tCK	9, 13
Data-in to PRECHARGE command		tDPL	2	2	tCK	10, 13
DQM to input data delay		tDQD	0	0	tCK	11
DQM to data mask during WRITEs		tDQM	0	0	tCK	11
DQM to data High-Z during READs		tDQZ	2	2	tCK	11
WRITE command to input data delay		tDWD	0	0	tCK	11
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	17
CKE to clock enable or power-down exit setup mode		tPED	1	1	tCK	8
Last data-in to PRECHARGE command		tRDL	2	2	tCK	10, 13
Data-out High-Z from PRECHARGE command	CL = 3	tROH(3)	3	3	tCK	11
	CL = 2	tROH(2)	2	2	tCK	11

Notes:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C commercial temperature, -40°C ≤ T_A ≤ +85°C industrial temperature, and -40°C ≤ T_A ≤ +105°C automotive temperature) is ensured.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
3. AC characteristics assume tT = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



6. tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet tOH before going High-Z.
7. AC operating and I_{DD} test conditions have V_{IL} = 0V and V_{IH} = 3.0V using a measurement reference level of 1.5V. If the input transition time is longer than 1ns, then the timing is measured from $V_{IL,max}$ and $V_{IH,min}$ and no longer from the 1.5V midpoint. CLK should always be 1.5V referenced to crossover. Refer to Micron technical note TN-48-09.
8. Timing is specified by tCKS. Clock(s) specified as a reference only at minimum cycle rate.
9. Timing is specified by tWR plus tRP. Clock(s) specified as a reference only at minimum cycle rate.
10. Timing is specified by tWR.

11. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
12. CLK must be toggled a minimum of two times during this period.
13. Based on ^{t}CK = 7.5ns for -75 and -7E, 6ns for -6A.
14. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
15. Auto precharge mode only. The precharge timing budget (^{t}RP) begins at 7ns for -7E and 7.5ns for -75 after the first clock delay and after the last WRITE is executed.
16. Precharge mode only.
17. JEDEC and PC100 specify three clocks.
18. ^{t}AC for -75/-7E at CL = 3 with no load is 4.6ns and is guaranteed by design.
19. Parameter guaranteed by design.
20. PC100 specifies a maximum of 6.5pF.
21. For operating frequencies ≤ 45 MHz, ^{t}CKS = 3.0ns.
22. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 6ns for -6A after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
23. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

Functional Description

In general, 512Mb SDRAM devices (32 Meg x 4 x 4 banks, 16 Meg x 8 x 4 banks, and 16 Meg x 16 x 4 banks) are quad-bank DRAM that operate at 3.3V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 4096 columns by 4 bits. Each of the x8's 134,217,728-bit banks is organized as 8192 rows by 2048 columns by 8 bits. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits.

Read and write accesses to the SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A[12:0] select the row). The address bits (x4: A[9:0], A11, ***A12***; x8: A[9:0], ***A11***; x16: ***A[9:0]***) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Commands

The following table provides a quick reference of available commands, followed by a written description of each command. Additional Truth Tables (Table 14 (page 28), Table 15 (page 30), and Table 16 (page 32)) provide current state/next state information.

Table 13: Truth Table – Commands and DQM Operation

Note 1 applies to all parameters and conditions

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE	L	H	H	L	X	X	Active	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	8
Write enable/output enable	X	X	X	X	L	X	Active	9
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	9

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. A[11:0] define the op-code written to the mode register.
9. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the device, regardless of whether the CLK signal is enabled. The device is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to the selected device (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

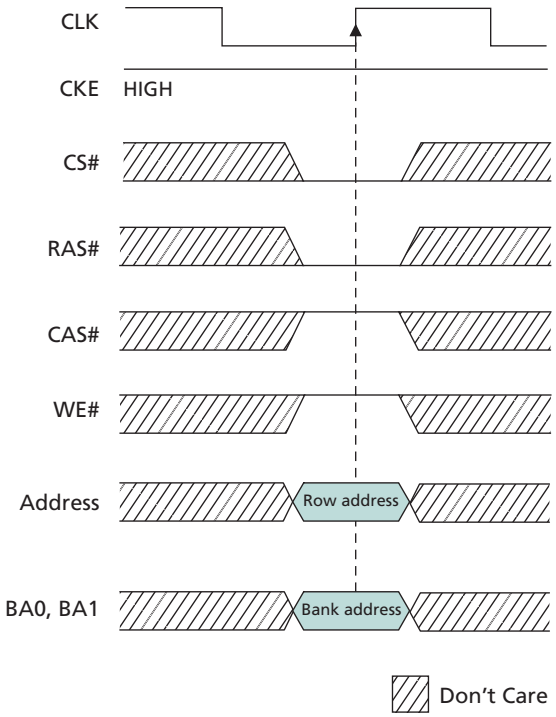
LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A[*n:0]* (where A*n* is the most significant address term), BA0, and BA1 (see Mode Register (page 35)). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to activate a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

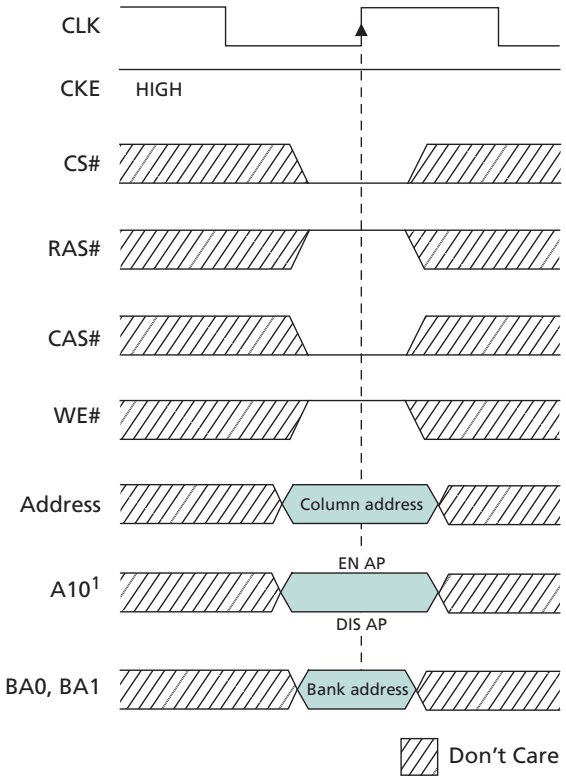
Figure 7: ACTIVE Command



READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

Figure 8: READ Command

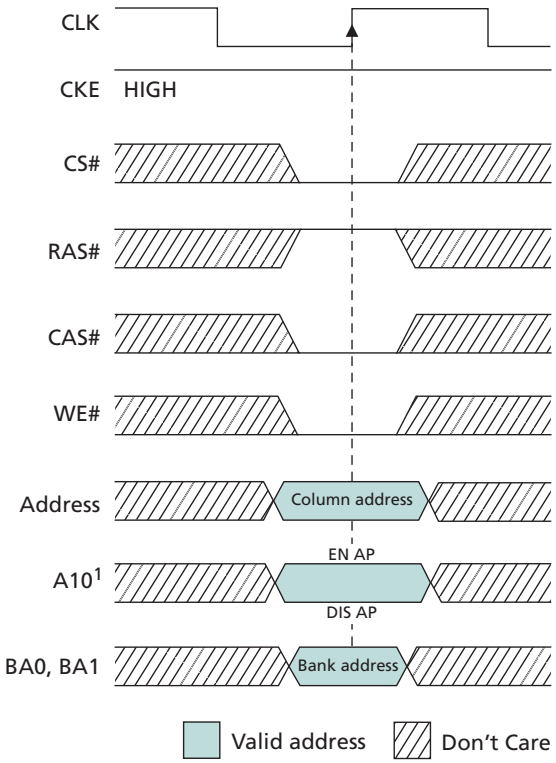


Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array, subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location.

Figure 9: WRITE Command

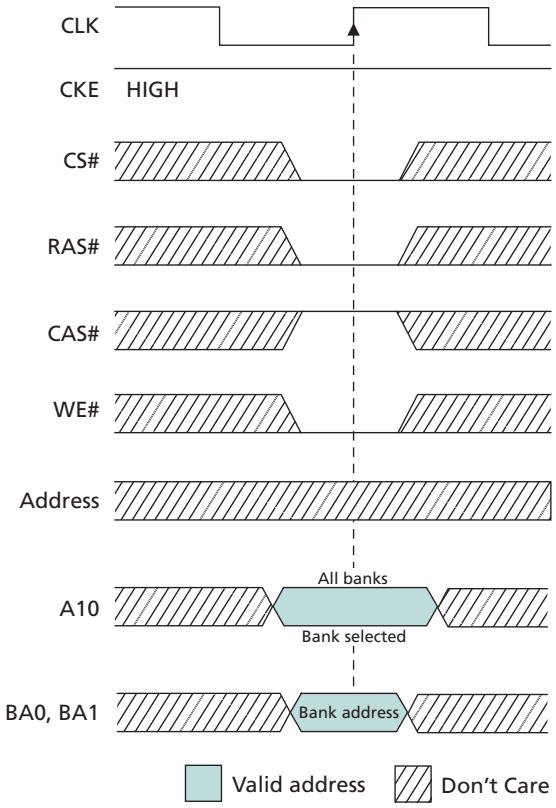


Note: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands are issued to that bank.

Figure 10: PRECHARGE Command



BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command is truncated.

REFRESH

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command, as shown in Bank/Row Activation (page 40).

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. Regardless of device width, the 512Mb SDRAM requires 8192 AUTO REFRESH cycles every 64ms (commercial and industrial). Providing a distributed AUTO REFRESH command every 7.813µs (commercial and industrial) will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms (commercial and industrial).

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered-down. When in the self refresh mode, the SDRAM retains data without external clocking.

The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become a "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. After CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued at the specified intervals, as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Truth Tables

Table 14: Truth Table – Current State Bank *n*, Command to Bank *n*

Notes 1–6 apply to all parameters and conditions

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	8
Row active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	10
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 16 (page 32)) and after ^{t}XSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown can be issued to that bank when in that state). Exceptions are covered below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to any other bank are determined by the bank's current state and the conditions described in this and the following table.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. After ^{t}RP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. After ^{t}RCD is met, the bank will be in the row active state.

Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the device will be in the all banks idle state.

   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the device will be in the all banks idle state.

   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank specific; requires that all banks are idle.
8. Does not affect the state of the bank and acts as a NOP to that bank.
9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. May or may not be bank specific; if all banks need to be precharged, each must be in a valid state for precharging.
11. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.

Table 15: Truth Table – Current State Bank n, Command to Bank *m*

Notes 1–6 apply to all parameters and conditions

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise supported for bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 12
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (Table 16 (page 32)), and after ^{t}XSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; for example, the current state is for bank *n* and the commands shown can be issued to bank *m*, assuming that bank *m* is in such a state that the given command is supported. Exceptions are covered below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^{t}RP has been met.

   Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands can only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
9. The burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency (CL) later.
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Table 16: Truth Table – CKE

Notes 1–4 apply to all parameters and conditions

Current State	CKE_{n-1}	CKE_n	$Command_n$	$Action_n$	Notes
Power-down	L	L	X	Maintain power-down	
Self refresh			X	Maintain self refresh	
Clock suspend			X	Maintain clock suspend	
Power-down	L	H	COMMAND INHIBIT or NOP	Exit power-down	5
Self refresh			COMMAND INHIBIT or NOP	Exit self refresh	6
Clock suspend			X	Exit clock suspend	7
All banks idle	H	L	COMMAND INHIBIT or NOP	Power-down entry	
All banks idle			AUTO REFRESH	Self refresh entry	
Reading or writing			VALID	Clock suspend entry	
	H	H	See Table 15 (page 30).		

Notes:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^{t}CKS is met).
6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state after ^{t}XSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^{t}XSR period. A minimum of two NOP commands must be provided during the ^{t}XSR period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.

Initialization

SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. After power is applied to V_{DD} and V_{DDQ} (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands must be applied.

After the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, at least two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it must be loaded prior to applying any operational command. If desired, the two AUTO REFRESH commands can be issued after the LMR command.

The recommended power-up sequence for SDRAM:

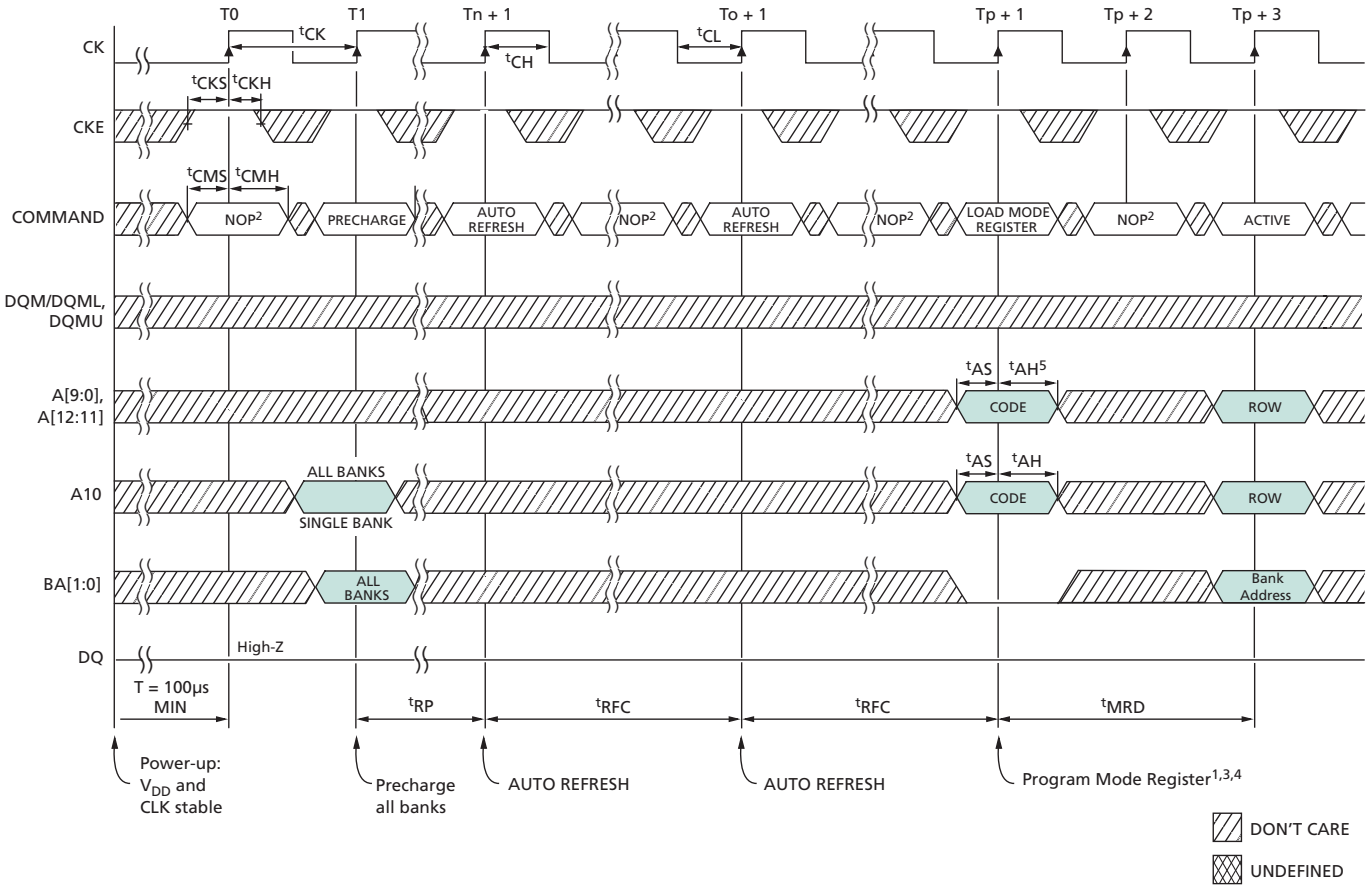
1. Simultaneously apply power to V_{DD} and V_{DDQ}.
2. Assert and hold CKE at a LVTTL logic LOW since all inputs and outputs are LVTTL-compatible.
3. Provide stable CLOCK signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
4. Wait at least 100µs prior to issuing any command other than a COMMAND INHIBIT or NOP.
5. Starting at some point during this 100µs period, bring CKE HIGH. Continuing at least through the end of this period, 1 or more COMMAND INHIBIT or NOP commands must be applied.
6. Perform a PRECHARGE ALL command.
7. Wait at least ^{t}RP time; during this time NOPs or DESELECT commands must be given. All banks will complete their precharge, thereby placing the device in the all banks idle state.
8. Issue an AUTO REFRESH command.
9. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
10. Issue an AUTO REFRESH command.
11. Wait at least ^{t}RFC time, during which only NOPs or COMMAND INHIBIT commands are allowed.
12. The SDRAM is now ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded with desired bit values prior to applying any operational command. Using the LMR command, program the mode register. The mode register is programmed via the MODE REGISTER SET command with BA1 = 0, BA0 = 0 and retains the stored information until it is programmed again or the device loses power. Not programming the mode register upon initialization will result in default settings which may not be desired. Outputs are guaranteed High-Z after the LMR command is issued. Outputs should be High-Z already before the LMR command is issued.
13. Wait at least ^{t}MRD time, during which only NOP or DESELECT commands are allowed.

At this point the DRAM is ready for any valid command.

Note:

More than two AUTO REFRESH commands can be issued in the sequence. After steps 9 and 10 are complete, repeat them until the desired number of AUTO REFRESH + ^{t}RFC loops is achieved.

Figure 11: Initialize and Load Mode Register



Notes:
1. The mode register may be loaded prior to the AUTO REFRESH cycles if desired.
2. If CS is HIGH at clock HIGH time, all commands applied are NOP.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after command is issued.
5. A12 should be a LOW at ^{t}P + 1.

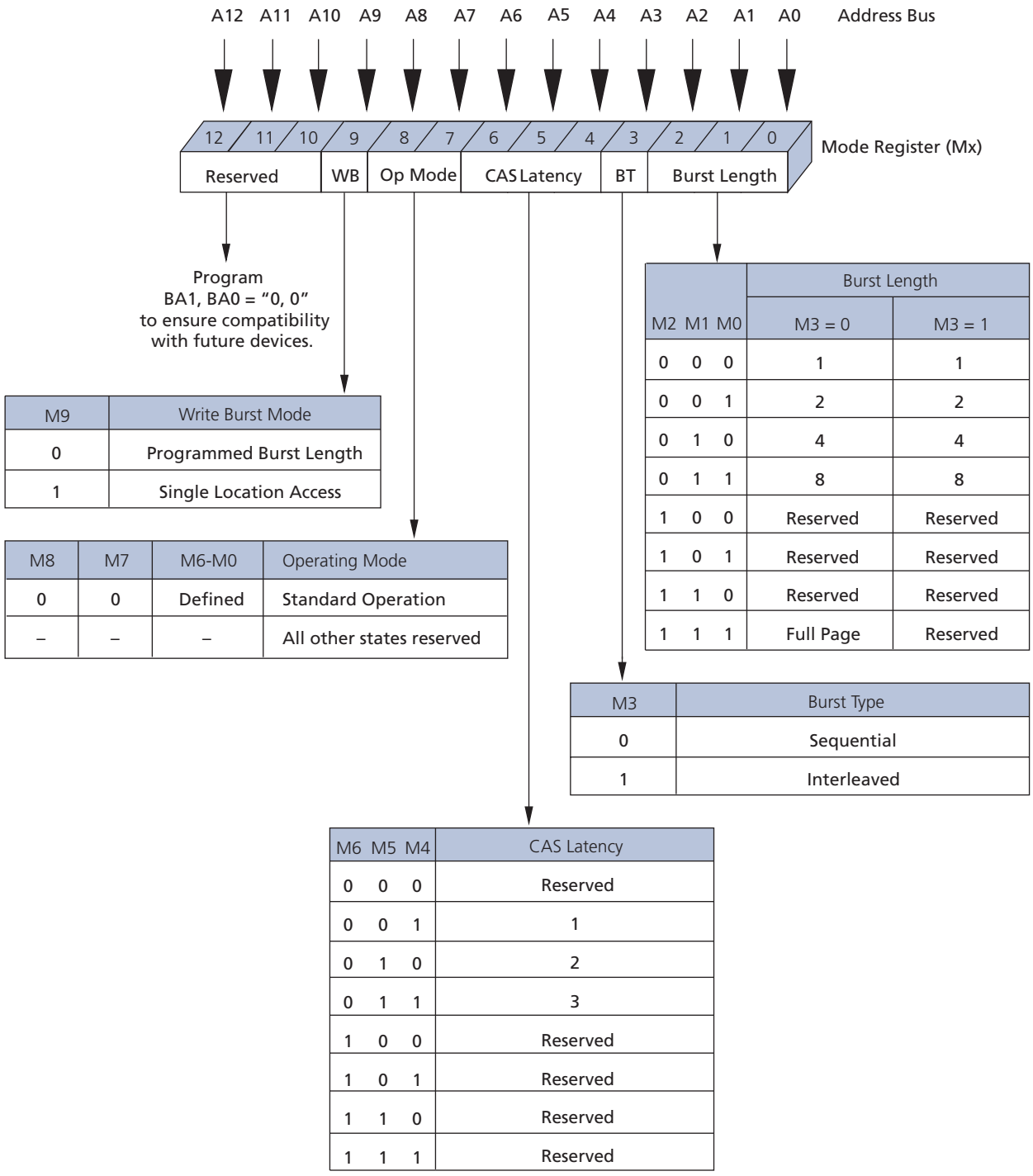
Mode Register

The mode register defines the specific mode of operation, including burst length (BL), burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and retains the stored information until it is programmed again or the device loses power.

Mode register bits M[2:0] specify the BL; M3 specifies the type of burst; M[6:4] specify the CL; M7 and M8 specify the operating mode; M9 specifies the write burst mode; and M10–M*n* should be set to zero to ensure compatibility with future revisions. M*n* + 1 and M*n* + 2 should be set to zero to select the mode register.

The mode registers must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 12: Mode Register Definition



M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
–	–	–	All other states reserved

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

Burst Length

Read and write accesses to the device are burst oriented, and the burst length (BL) is programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, 8, or continuous locations are available for both the sequential and the interleaved burst types, and a continuous page burst is available for the sequential type. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block when a boundary is reached. The block is uniquely selected by A[8:1] when BL = 2, A[8:2] when BL = 4, and A[8:3] when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Continuous page bursts wrap within the page when the boundary is reached.

Burst Type

Accesses within a given burst can be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address.

Table 17: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Continuous					
	n = A0–An/9/8 (location 0–y)			Cn, Cn + 1, Cn + 2, Cn + 3...Cn - 1, Cn...	Not supported

Notes:
1. For full-page accesses: y = 2048 (x4); y = 1024 (x8); y = 512 (x16).
2. For BL = 2, A1–A9, A11 (x4); A1–A9 (x8); or A1–A8 (x16) select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A9, A11 (x4); A2–A9 (x8); or A2–A8 (x16) select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A9, A11 (x4); A3–A9 (x8); or A3–A8 (x16) select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A9, A11 (x4); A0–A9 (x8); or A0–A8 (x16) select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For BL = 1, A0–A9, A11 (x4); A0–A9 (x8); or A0–A8 (x16) select the unique column to be accessed, and mode register bit M3 is ignored.

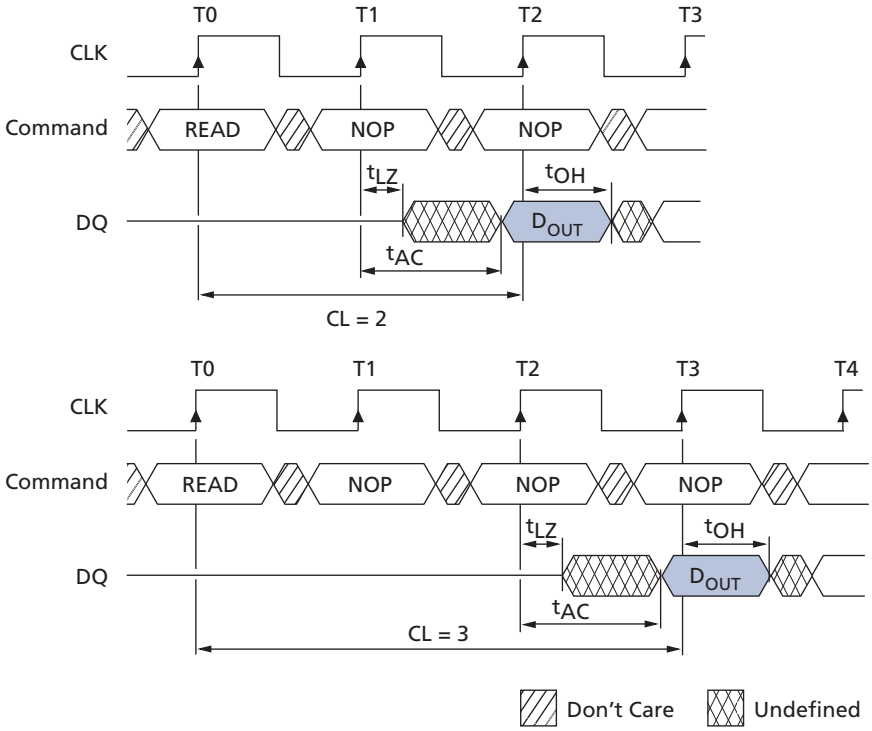
CAS Latency

The CAS latency (CL) is the delay, in clock cycles, between the registration of a READ command and the availability of the output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQ start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data is valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQ start driving after T1 and the data is valid by T2.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 13: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M[2:0] applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Bank/Row Activation

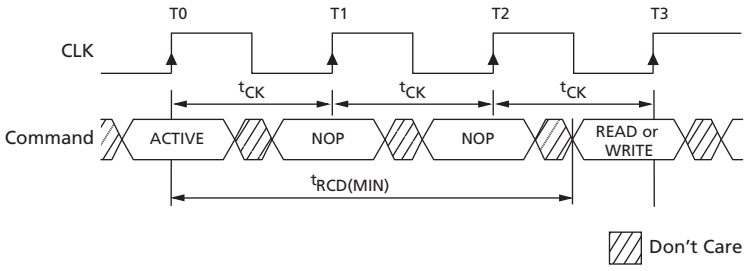
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with the ACTIVE command, a READ or WRITE command can be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 14 (page 40), which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been precharged. The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 14: Example: Meeting ^{t}RCD (MIN) When $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$



READ Operation

READ bursts are initiated with a READ command, as shown in Figure 8 (page 24). The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. In the following figures, auto precharge is disabled.

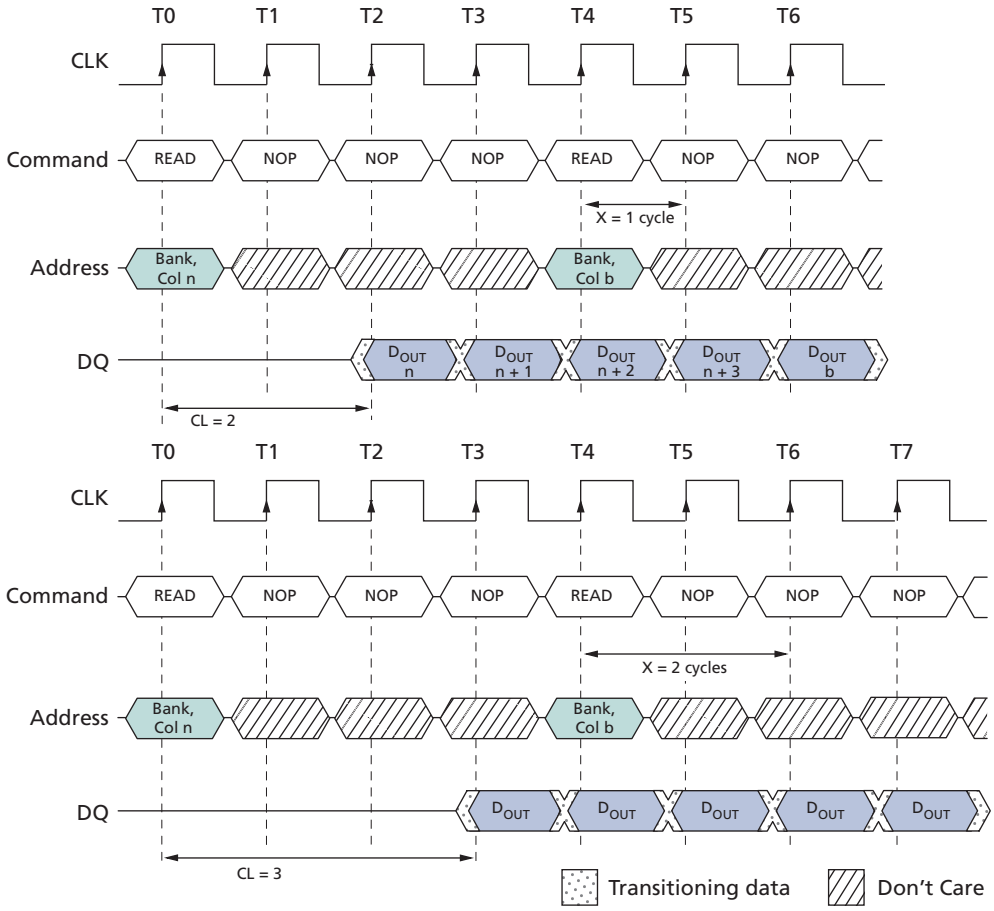
During READ bursts, the valid data-out element from the starting column address is available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 16 (page 43) shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ signals will go to High-Z. A continuous page burst continues until terminated. At the end of the page, it wraps to column 0 and continues.

Data from any READ burst can be truncated with a subsequent READ command, and data from a fixed-length READ burst can be followed immediately by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 16 (page 43) for CL2 and CL3.

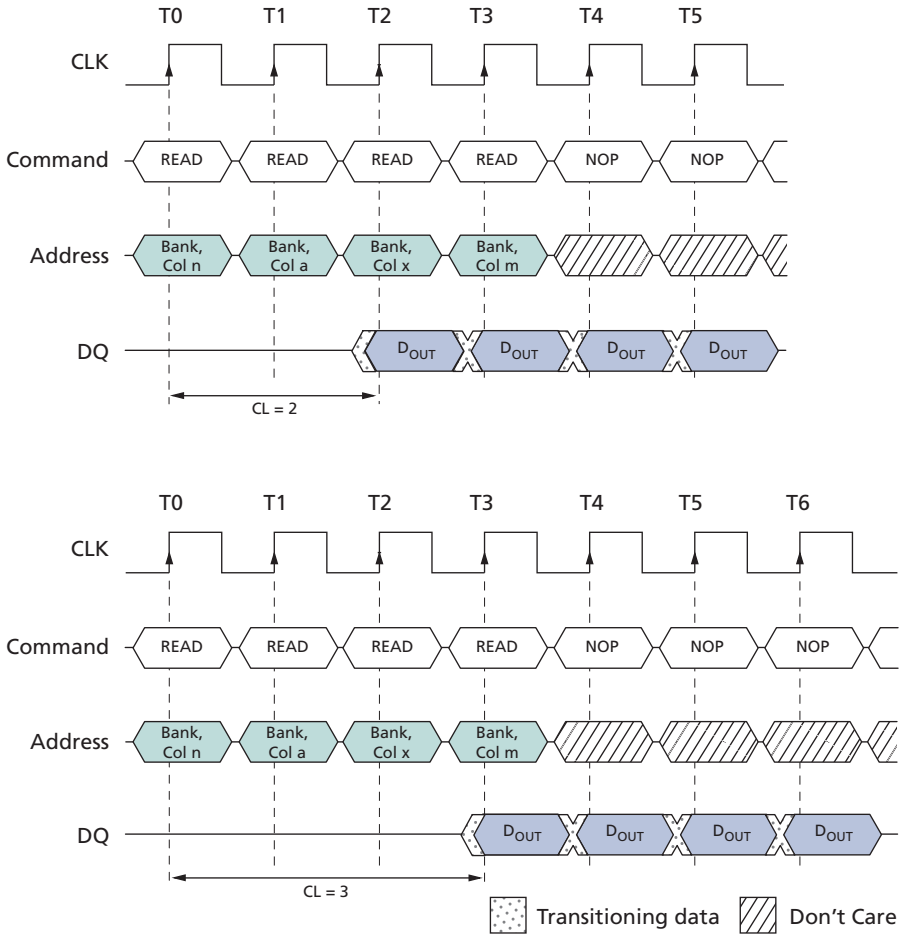
SDRAM devices use a pipelined architecture and therefore do not require the 2n rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a READ command. Full-speed random read accesses can be performed to the same bank, or each subsequent READ can be performed to a different bank.

Figure 15: Consecutive READ Bursts



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

Figure 16: Random READ Accesses



Note: 1. Each READ command can be issued to any bank. DQM is LOW.

Data from any READ burst can be truncated with a subsequent WRITE command, and data from a fixed-length READ burst can be followed immediately by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst can be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there is a possibility that the device driving the input data will go Low-Z before the DQ go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

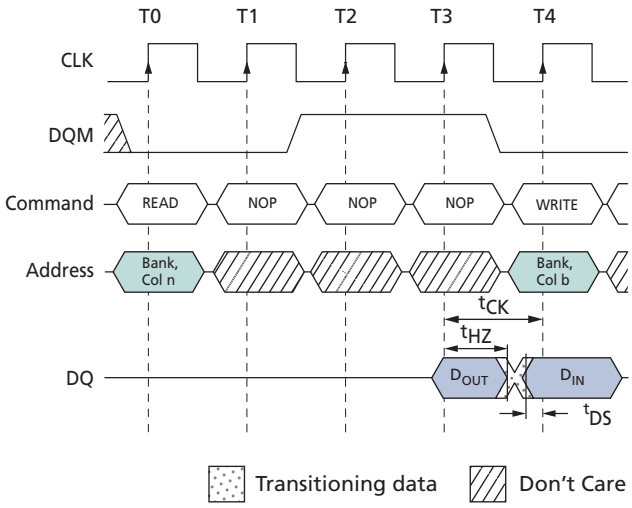
The DQM input is used to avoid I/O contention, as shown in Figure 17 (page 44) and Figure 18 (page 45). The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. After the WRITE command is registered, the DQ will go to High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4, then the WRITEs at T5 and T7 would be valid, and the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 17 (page 44) shows where, due to the clock cycle frequency, bus contention is avoided without having to add a NOP cycle, while Figure 18 (page 45) shows the case where an additional NOP cycle is required.

A fixed-length READ burst may be followed by or truncated with a PRECHARGE command to the same bank, provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 19 (page 45) for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

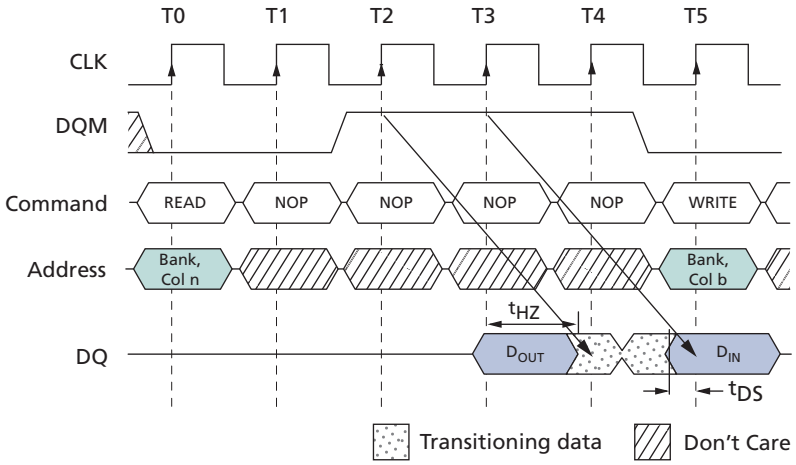
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate fixed-length or continuous page bursts.

Figure 17: READ-to-WRITE



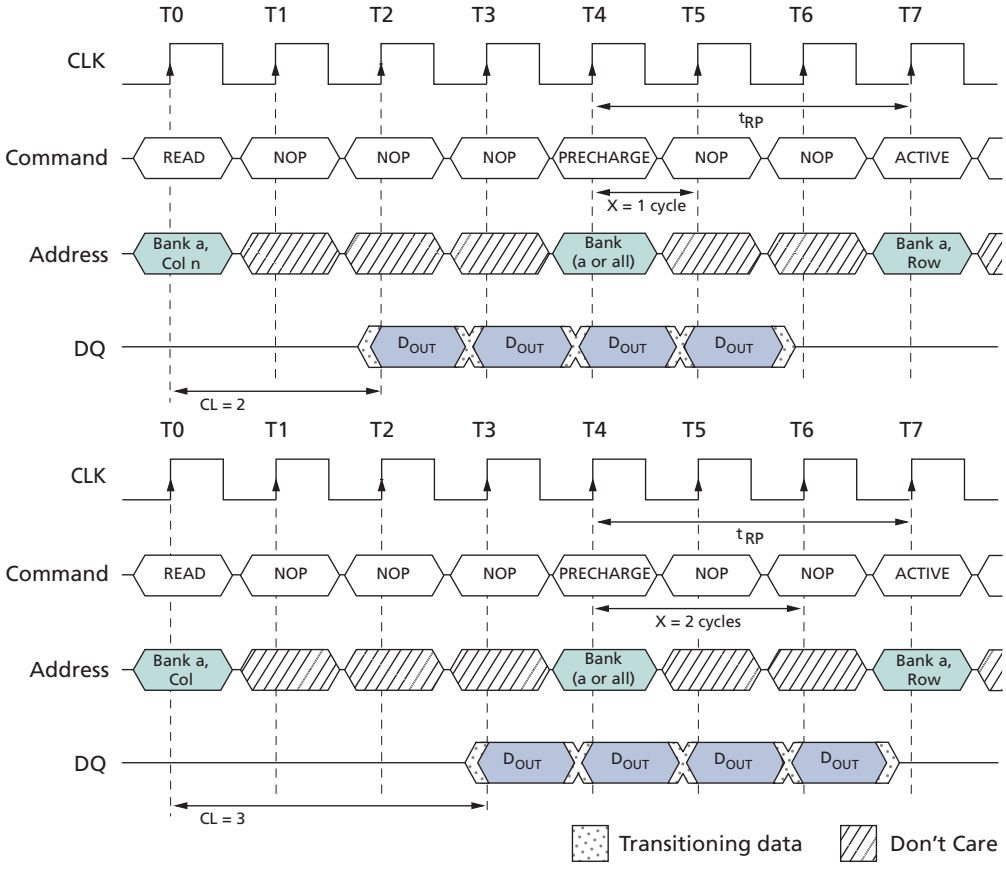
Note: 1. CL = 3. The READ command can be issued to any bank, and the WRITE command can be to any bank. If a burst of one is used, DQM is not required.

Figure 18: READ-to-WRITE With Extra Clock Cycle



Note: 1. CL = 3. The READ command can be issued to any bank, and the WRITE command can be to any bank.

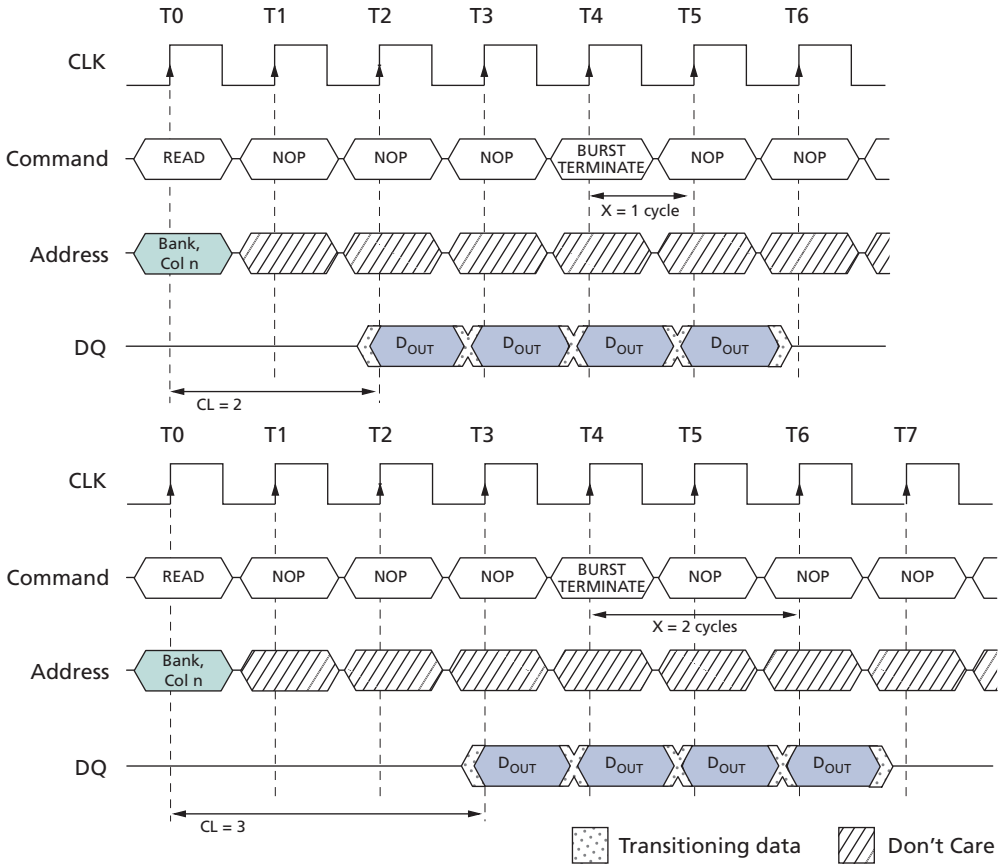
Figure 19: READ-to-PRECHARGE



Note: 1. DQM is LOW.

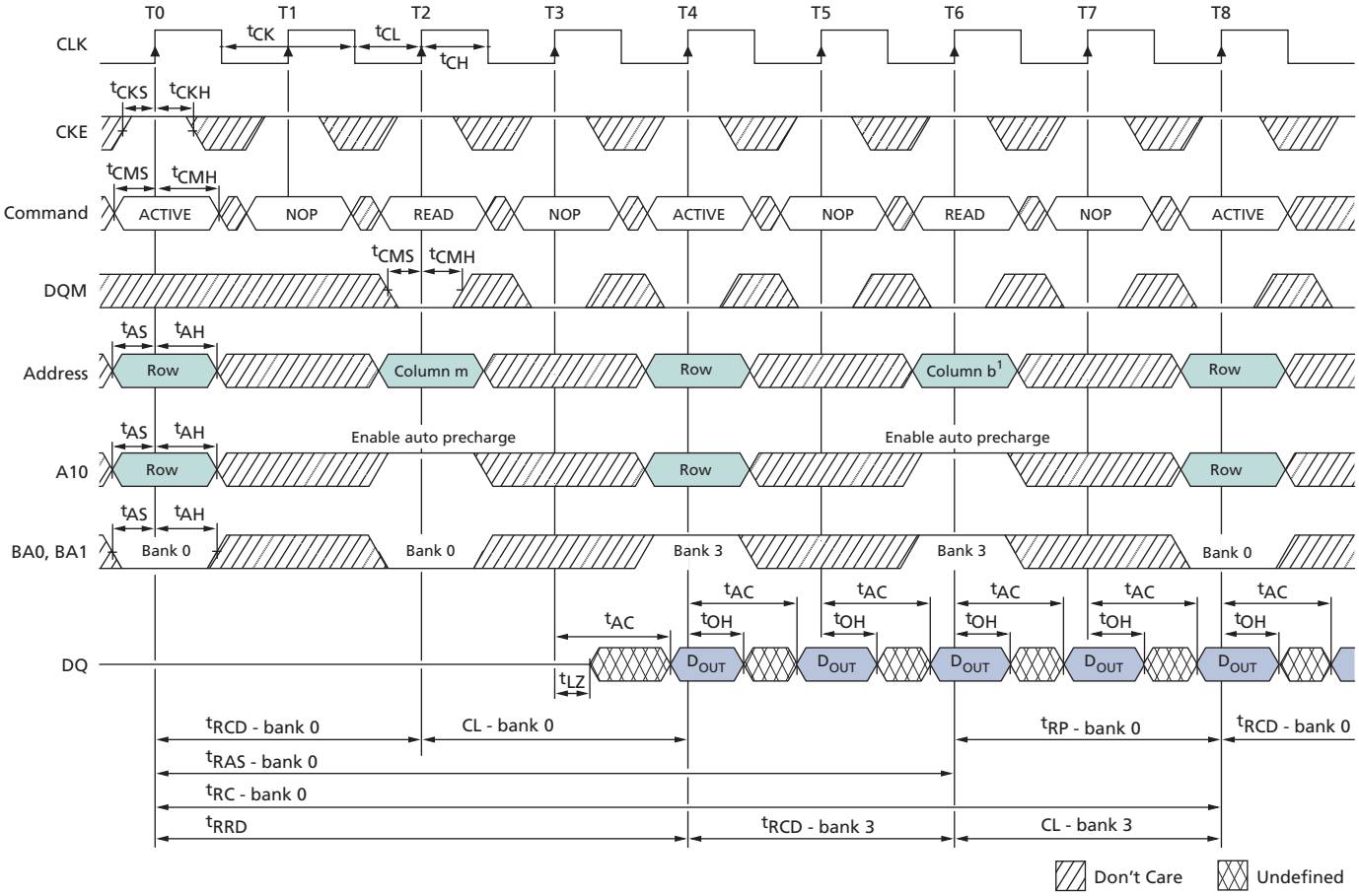
Continuous-page READ bursts can be truncated with a BURST TERMINATE command and fixed-length READ bursts can be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 20 (page 46) for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

Figure 20: Terminating a READ Burst



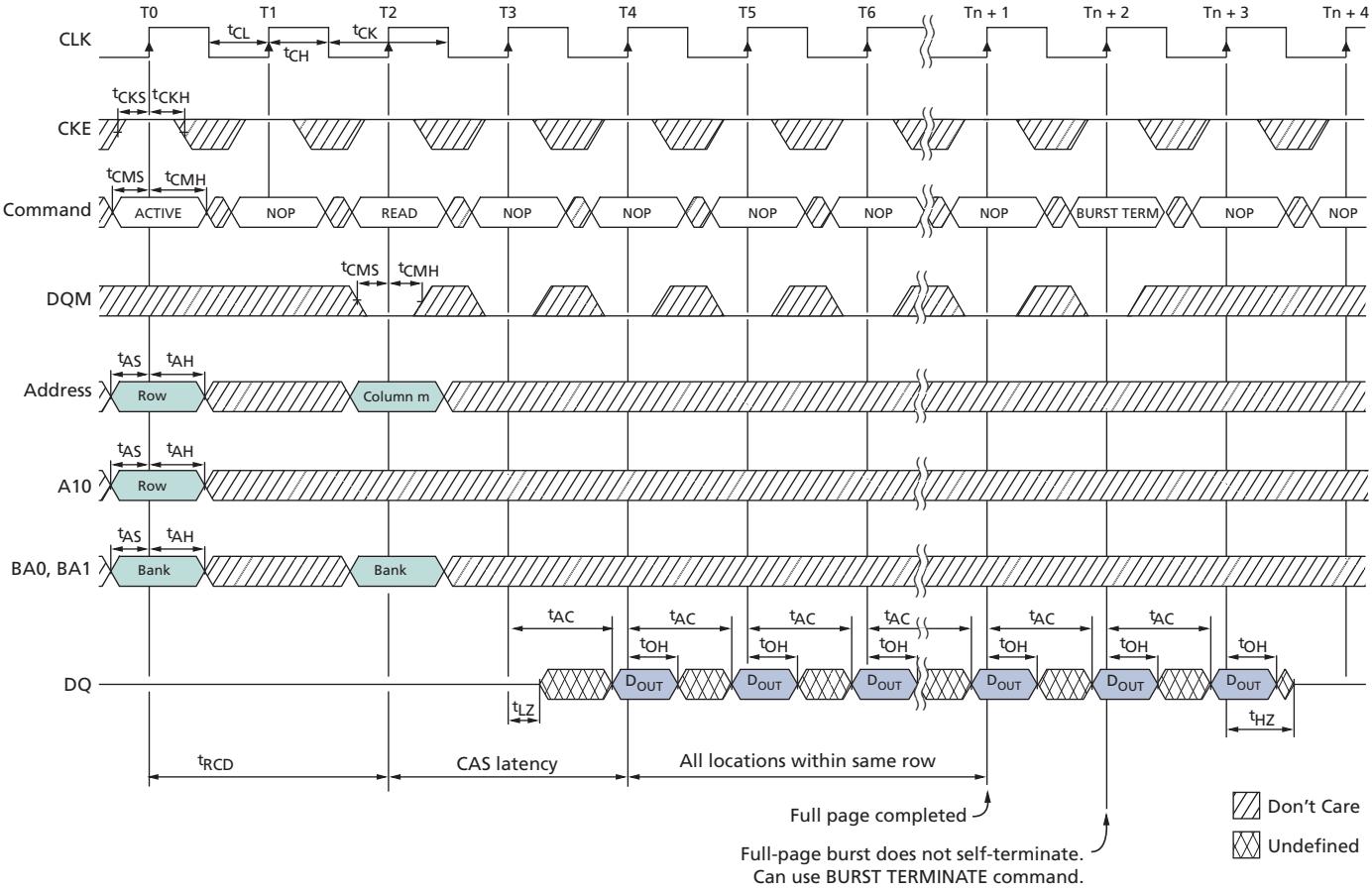
Note: 1. DQM is LOW.

Figure 21: Alternating Bank Read Accesses



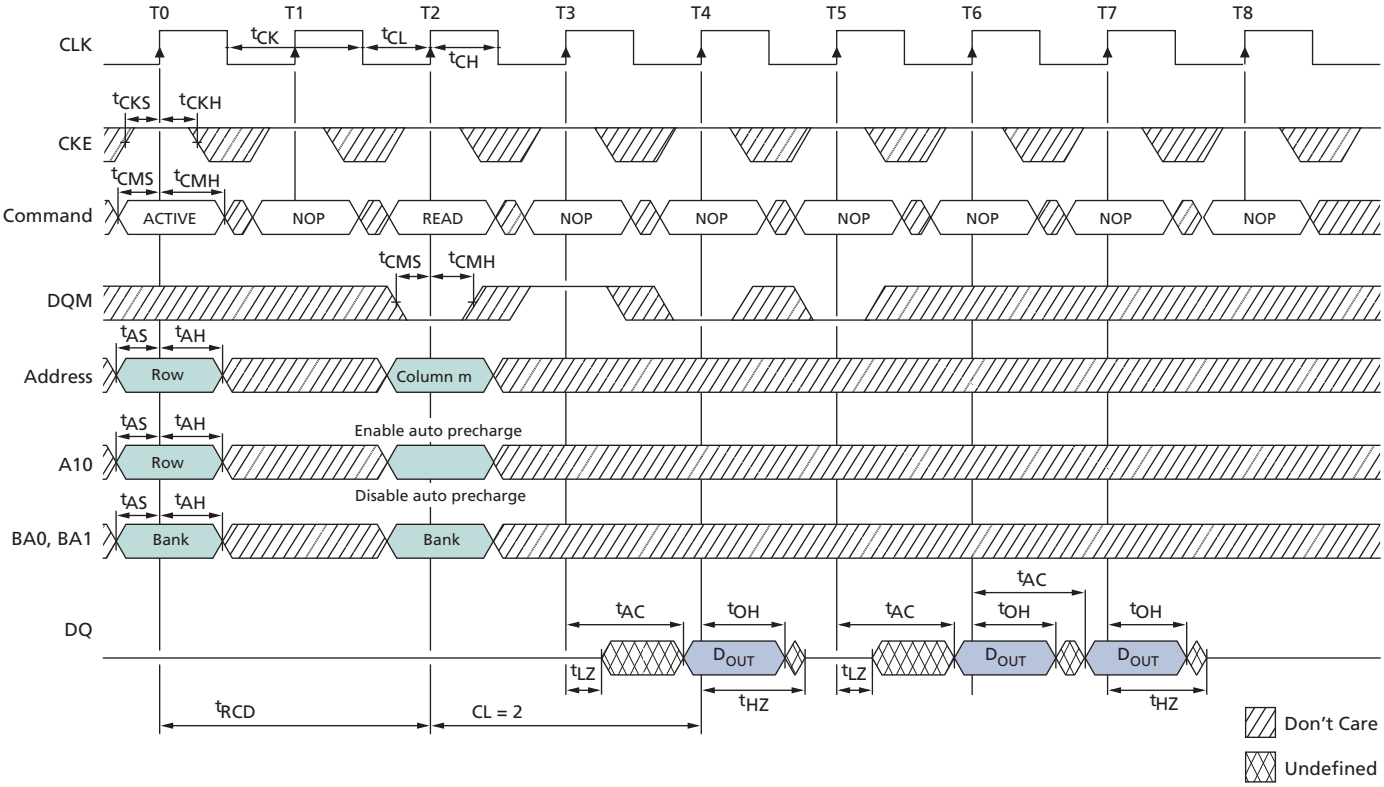
Note: 1. For this example, BL = 4 and CL = 2.

Figure 22: READ Continuous Page Burst



Note: 1. For this example, CL = 2.

Figure 23: READ – DQM Operation



Note: 1. For this example, BL = 4 and CL = 2.

WRITE Operation

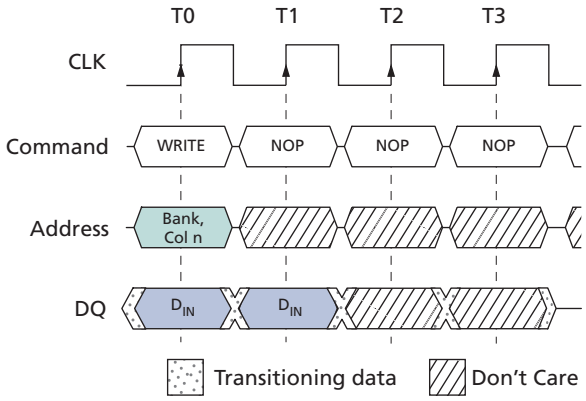
WRITE bursts are initiated with a WRITE command, as shown in Figure 9 (page 25). The starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following figures, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command. Subsequent data elements are registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain at High-Z and any additional input data will be ignored (see Figure 24 (page 50)). A continuous page burst continues until terminated; at the end of the page, it wraps to column 0 and continues.

Data for any WRITE burst can be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst can be followed immediately by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command (see Figure 25 (page 51)). Data $n + 1$ is either the last of a burst of two or the last desired data element of a longer burst.

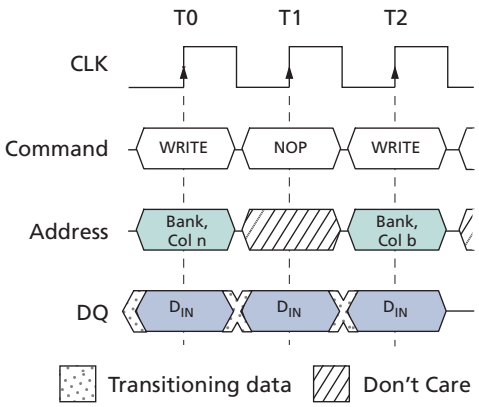
SDRAM devices use a pipelined architecture and therefore do not require the $2n$ rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 26 (page 52), or each subsequent WRITE can be performed to a different bank.

Figure 24: WRITE Burst



Note: 1. BL = 2. DQM is LOW.

Figure 25: WRITE-to-WRITE



Note: 1. DQM is LOW. Each WRITE command may be issued to any bank.

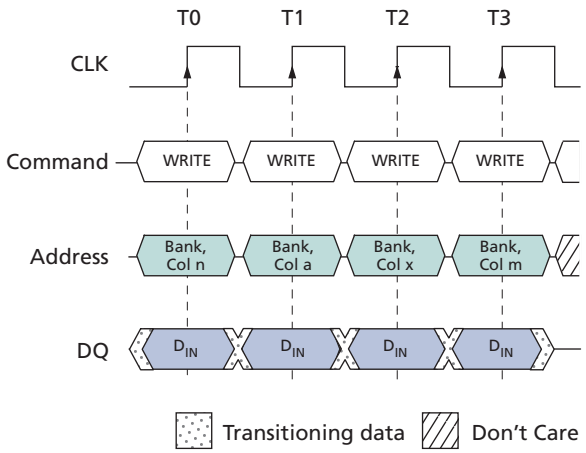
Data for any WRITE burst can be truncated with a subsequent READ command, and data for a fixed-length WRITE burst can be followed immediately by a READ command. After the READ command is registered, data input is ignored and WRITEs will not be executed (see Figure 27 (page 52)). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst.

Data for a fixed-length WRITE burst can be followed by or truncated with a PRECHARGE command to the same bank, provided that auto precharge was not activated. A continuous-page WRITE burst can be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock with time to complete, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to and the clock edge coincident with the PRECHARGE command (see Figure 28 (page 53)). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

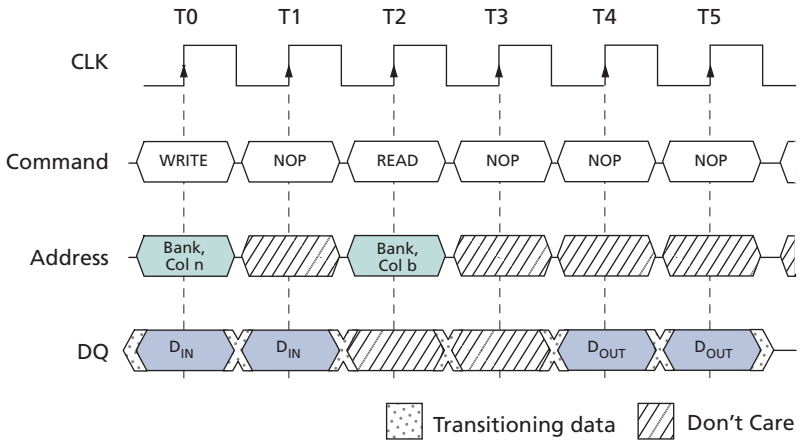
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts or continuous page bursts.

Figure 26: Random WRITE Cycles



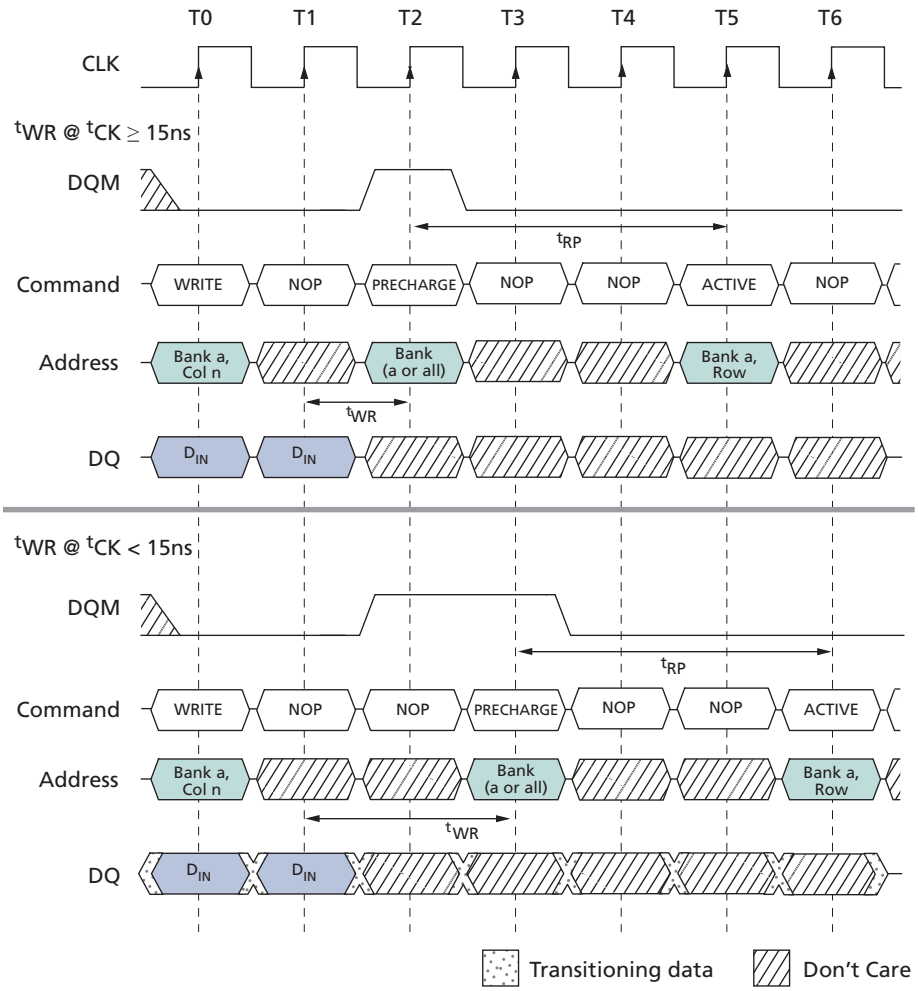
Note: 1. Each WRITE command can be issued to any bank. DQM is LOW.

Figure 27: WRITE-to-READ



Note: 1. The WRITE command can be issued to any bank, and the READ command can be to any bank. DQM is LOW. CL = 2 for illustration.

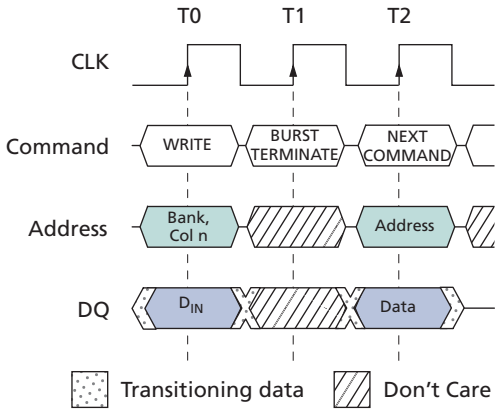
Figure 28: WRITE-to-PRECHARGE



Note: 1. In this example DQM could remain LOW if the WRITE burst is a fixed length of two.

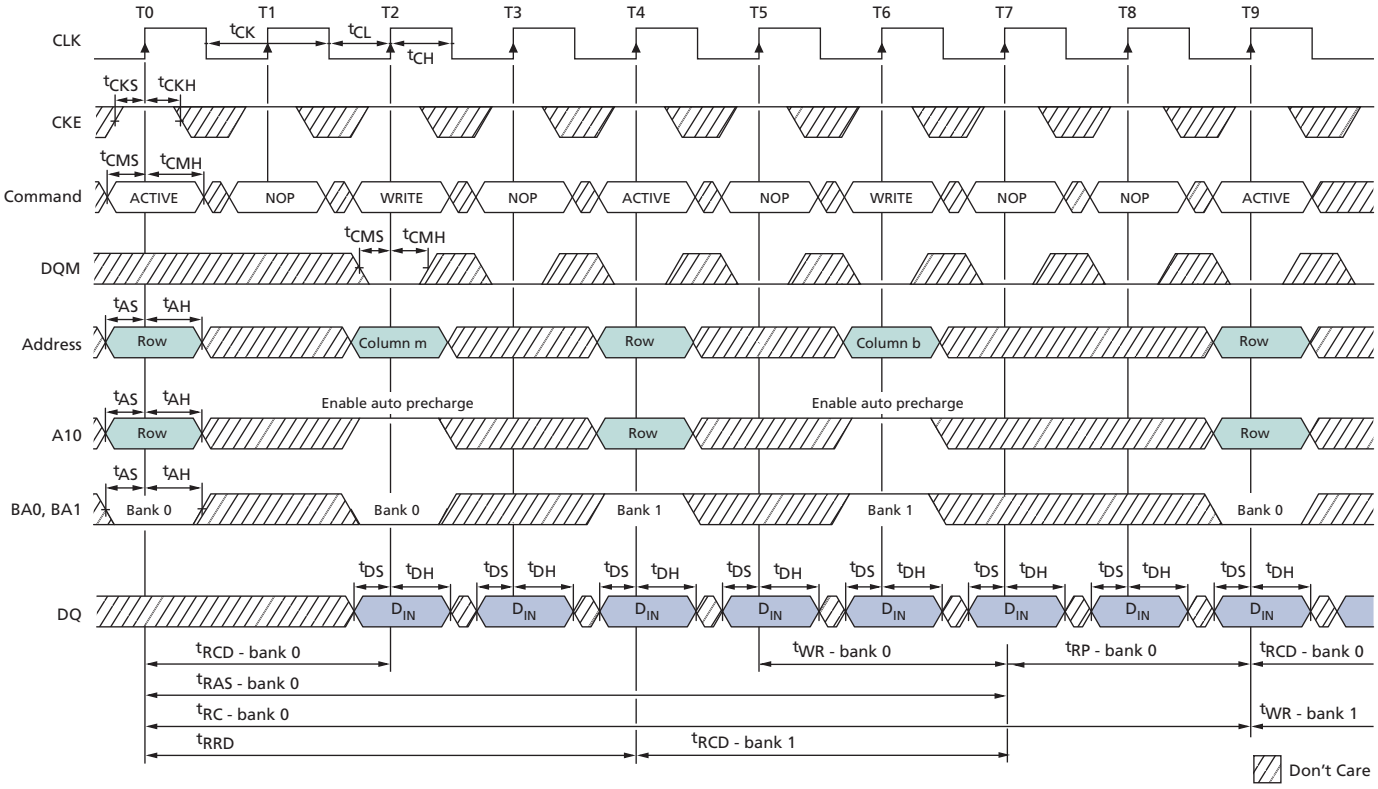
Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command is ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 29 (page 54), where data *n* is the last desired data element of a longer burst.

Figure 29: Terminating a WRITE Burst



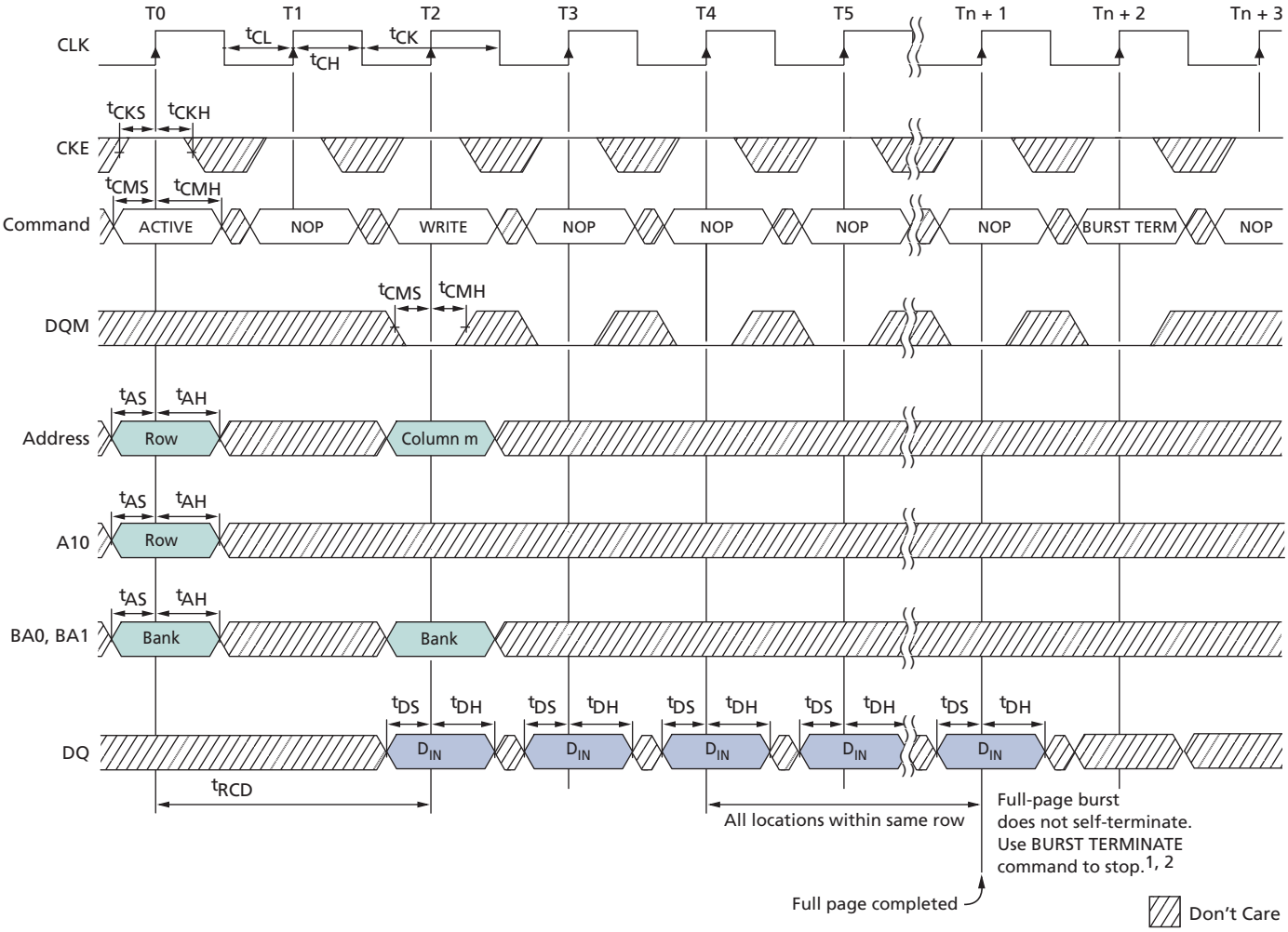
Note: 1. DQM is LOW.

Figure 30: Alternating Bank Write Accesses



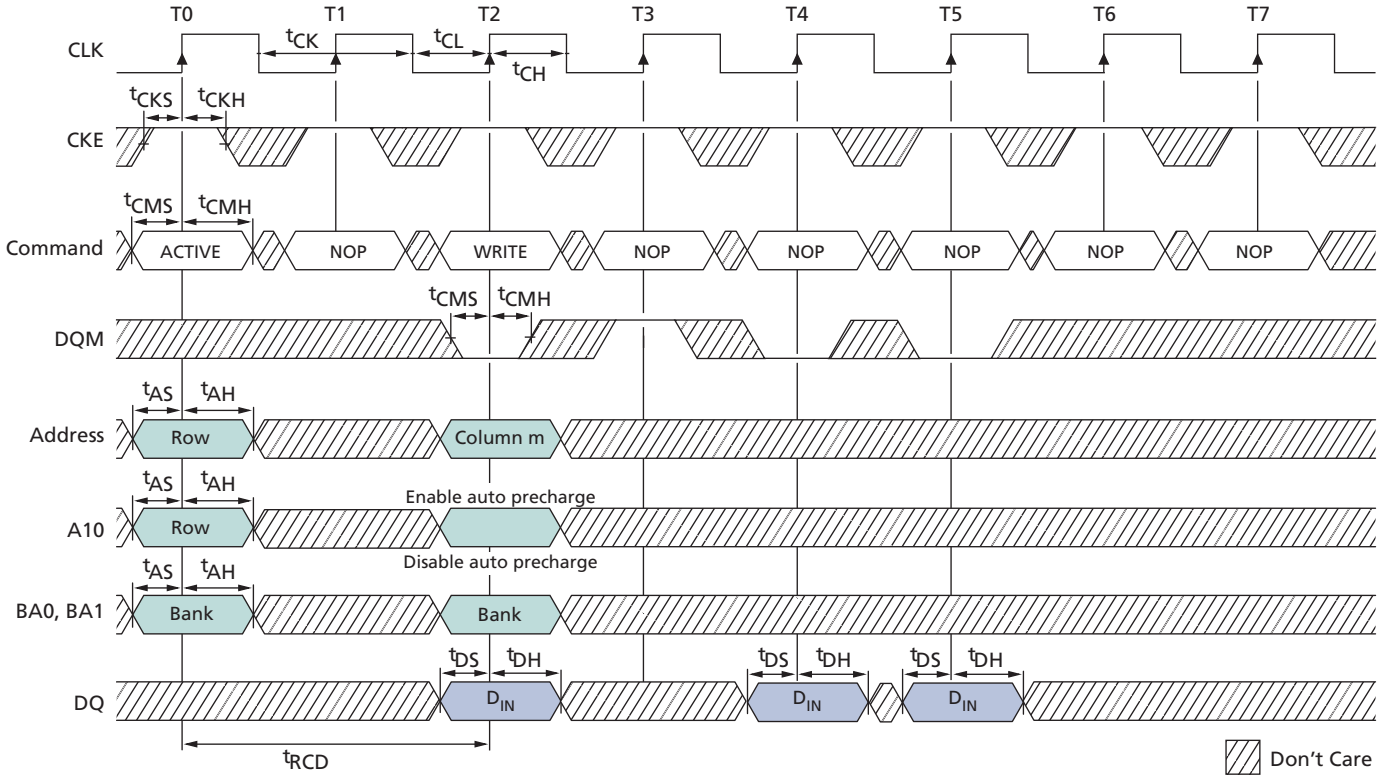
Note: 1. For this example, BL = 4.

Figure 31: WRITE – Continuous Page Burst



Notes:
1. tWR must be satisfied prior to issuing a PRECHARGE command.
2. Page left open; no tRP.

Figure 32: WRITE – DQM Operation



Note: 1. For this example, BL = 4.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

PRECHARGE Operation

The PRECHARGE command (see Figure 10 (page 26)) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged (A10 = LOW), inputs BA0 and BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described previously, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the continuous page burst mode where auto precharge does not apply. In the specific case of write burst mode set to single location access with burst length set to continuous, the burst length setting is the overriding setting and auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. Another command cannot be issued to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Burst Type (page 37) section.

Micron SDRAM supports concurrent auto precharge; cases of concurrent auto precharge for READs and WRITEs are defined below.

READ with auto precharge interrupted by a READ (with or without auto precharge)

A READ to bank *m* will interrupt a READ on bank *n* following the programmed CAS latency. The precharge to bank *n* begins when the READ to bank *m* is registered (see Figure 33 (page 59)).

READ with auto precharge interrupted by a WRITE (with or without auto precharge)

A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* begins when the WRITE to bank *m* is registered (see Figure 34 (page 60)).

WRITE with auto precharge interrupted by a READ (with or without auto precharge)

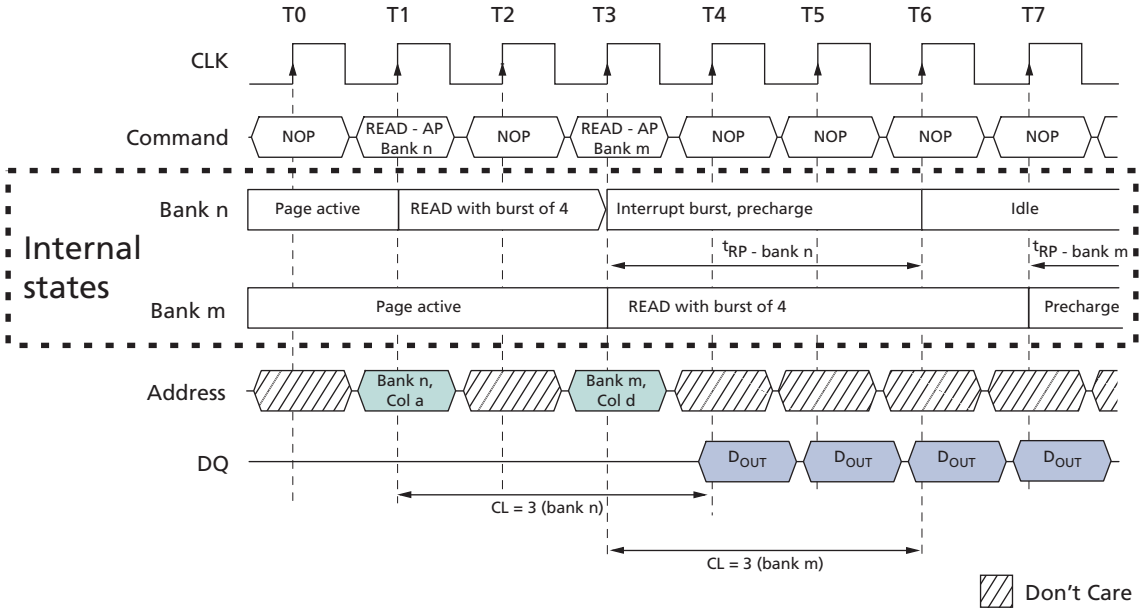
A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 39 (page 65)).

WRITE with auto precharge interrupted by a WRITE (with or without auto precharge)

A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is reg-

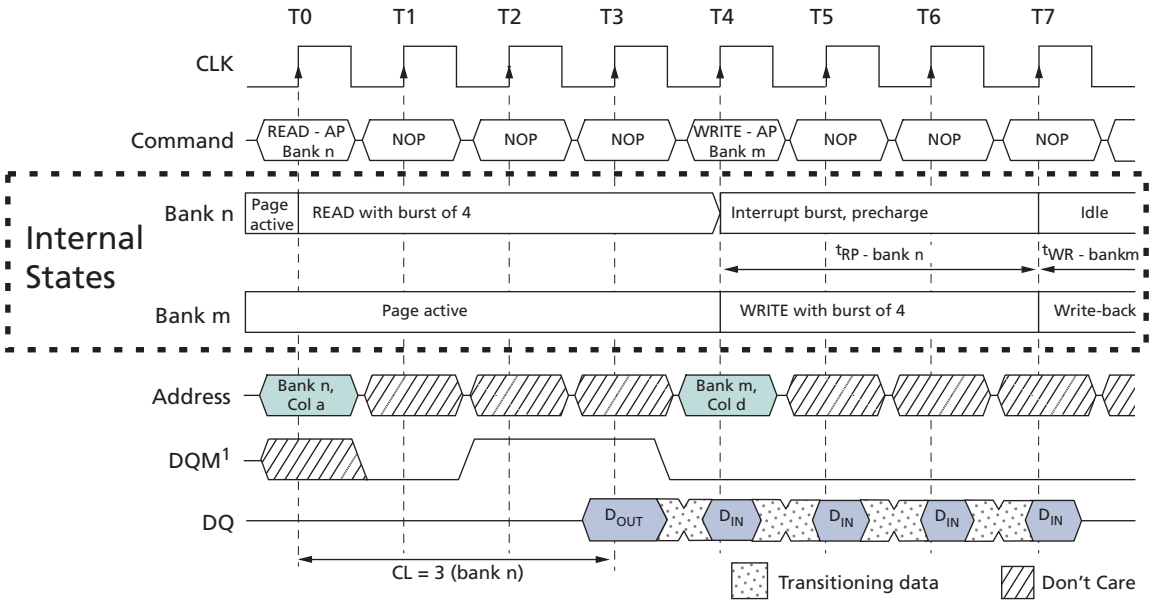
istered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 40 (page 65)).

Figure 33: READ With Auto Precharge Interrupted by a READ



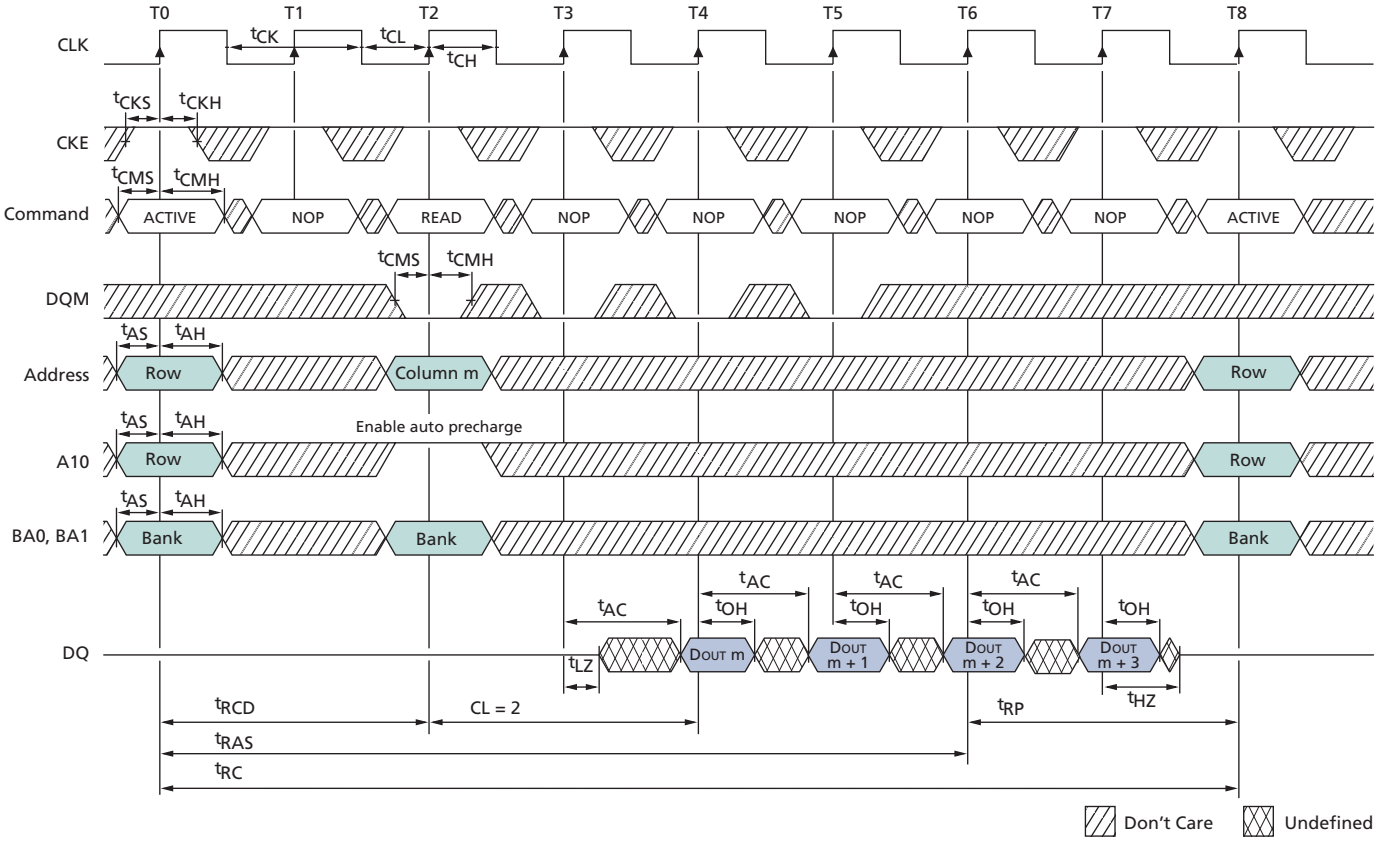
Note: 1. DQM is LOW.

Figure 34: READ With Auto Precharge Interrupted by a WRITE



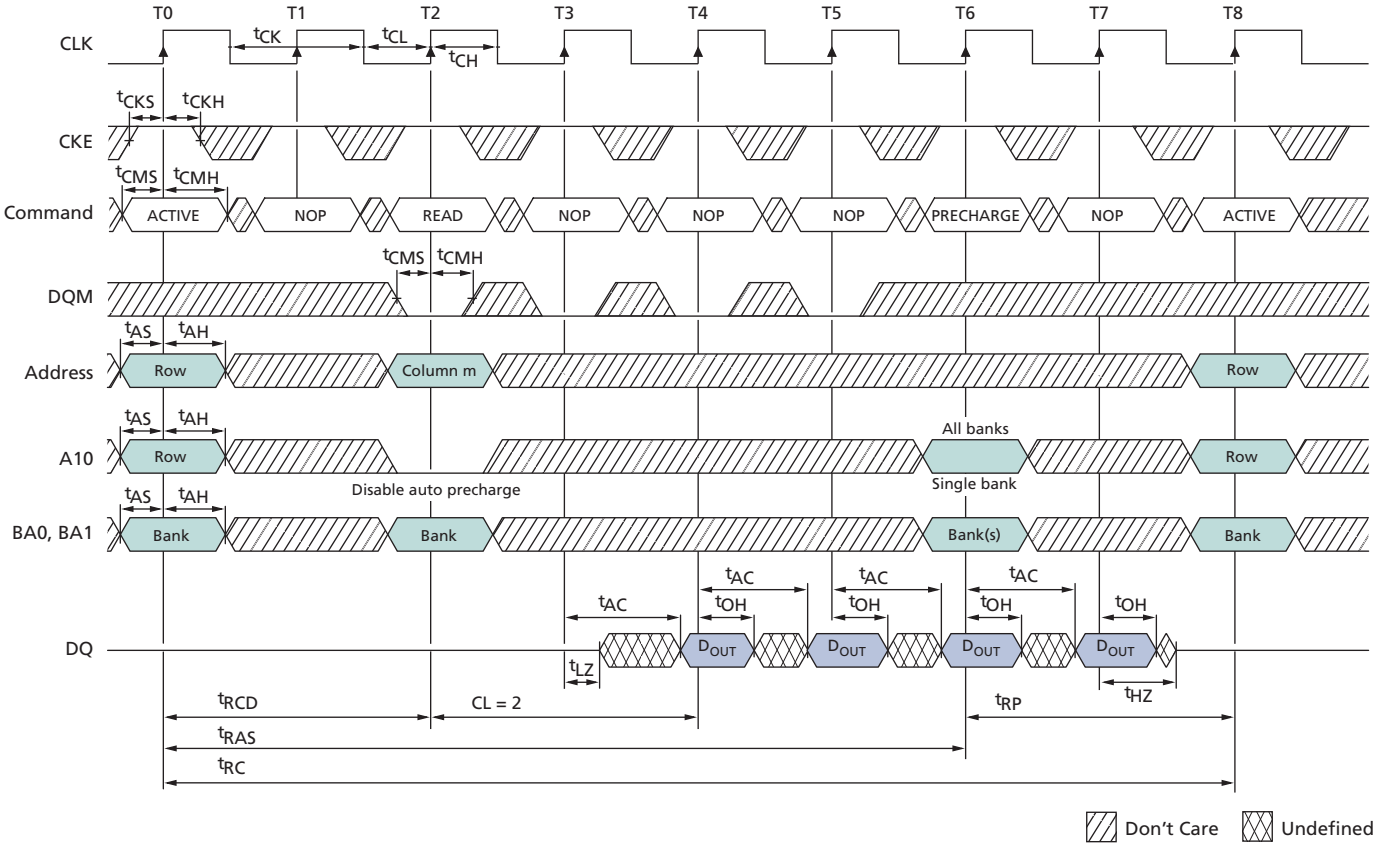
Note: 1. DQM is HIGH at T2 to prevent $D_{OUT}a$ + 1 from contending with $D_{IN}d$ at T4.

Figure 35: READ With Auto Precharge



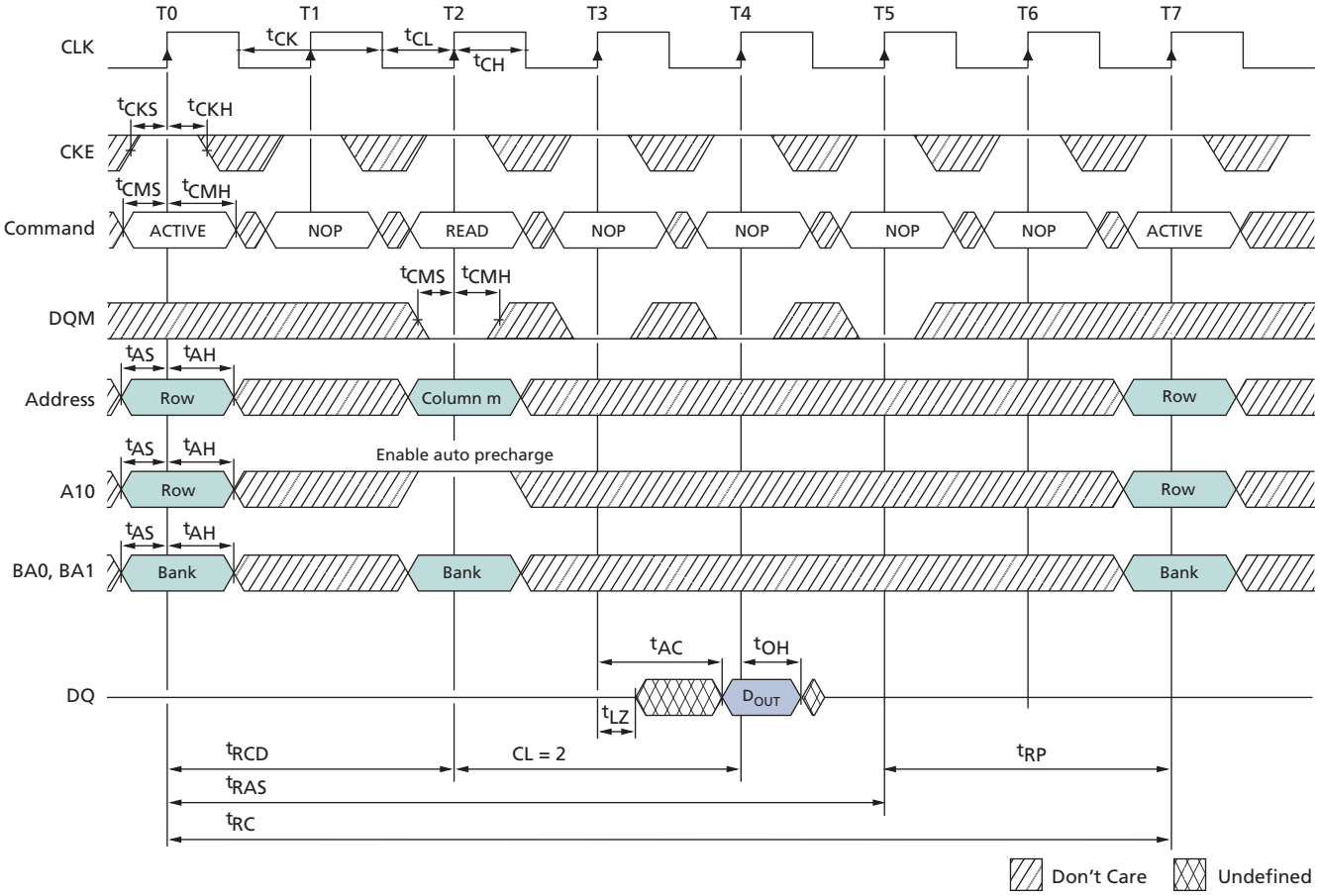
Note: 1. For this example, BL = 4 and CL = 2.

Figure 36: READ Without Auto Precharge



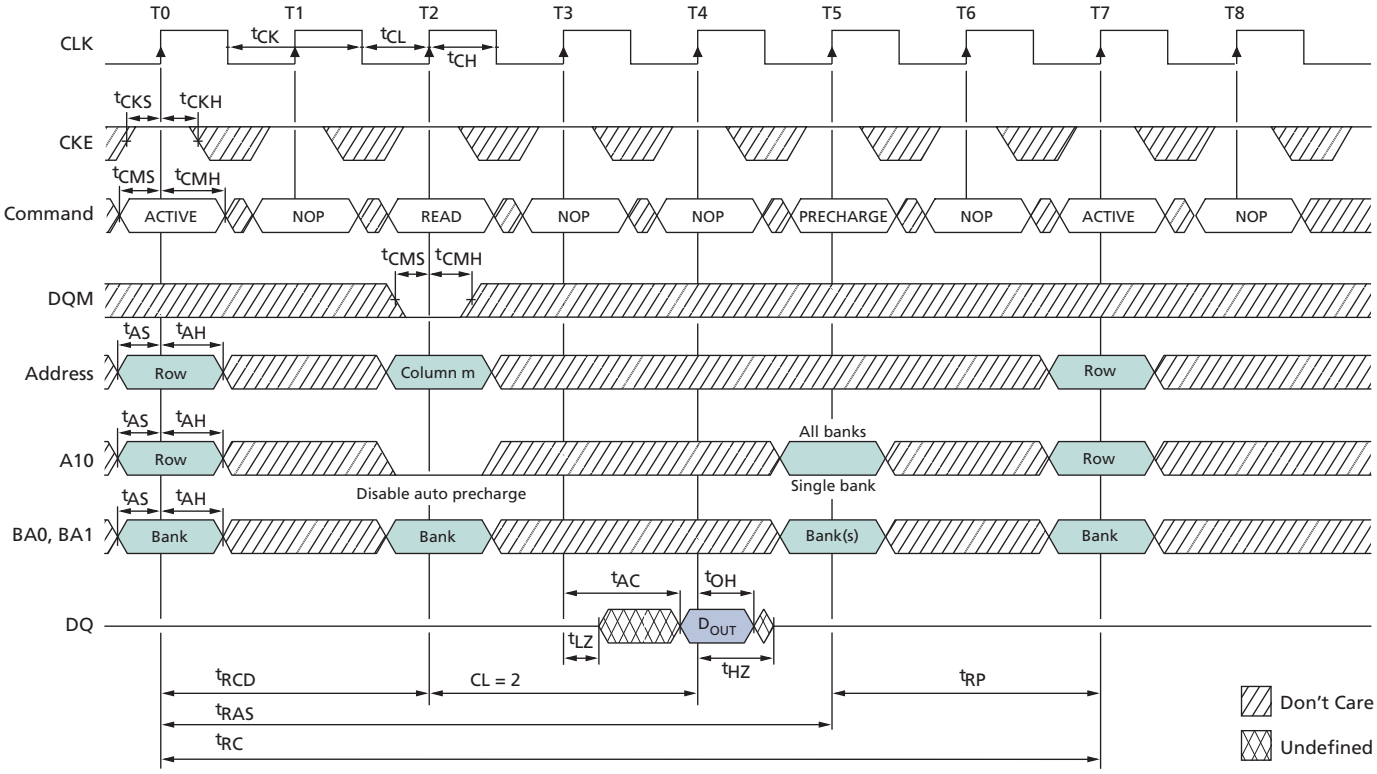
Note: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 37: Single READ With Auto Precharge



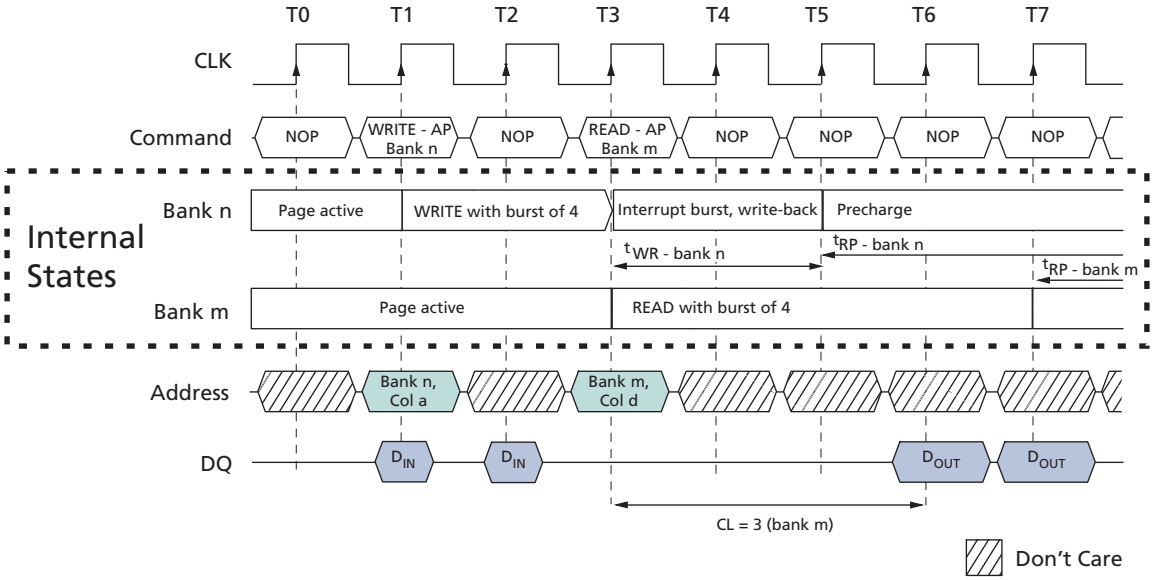
Note: 1. For this example, BL = 1 and CL = 2.

Figure 38: Single READ Without Auto Precharge



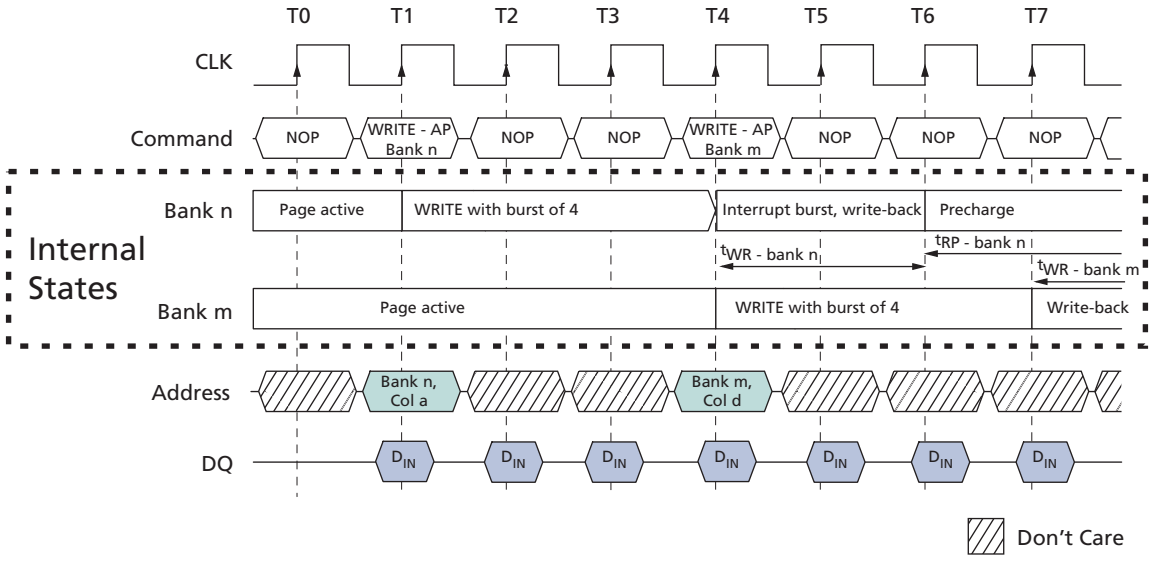
Note: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 39: WRITE With Auto Precharge Interrupted by a READ



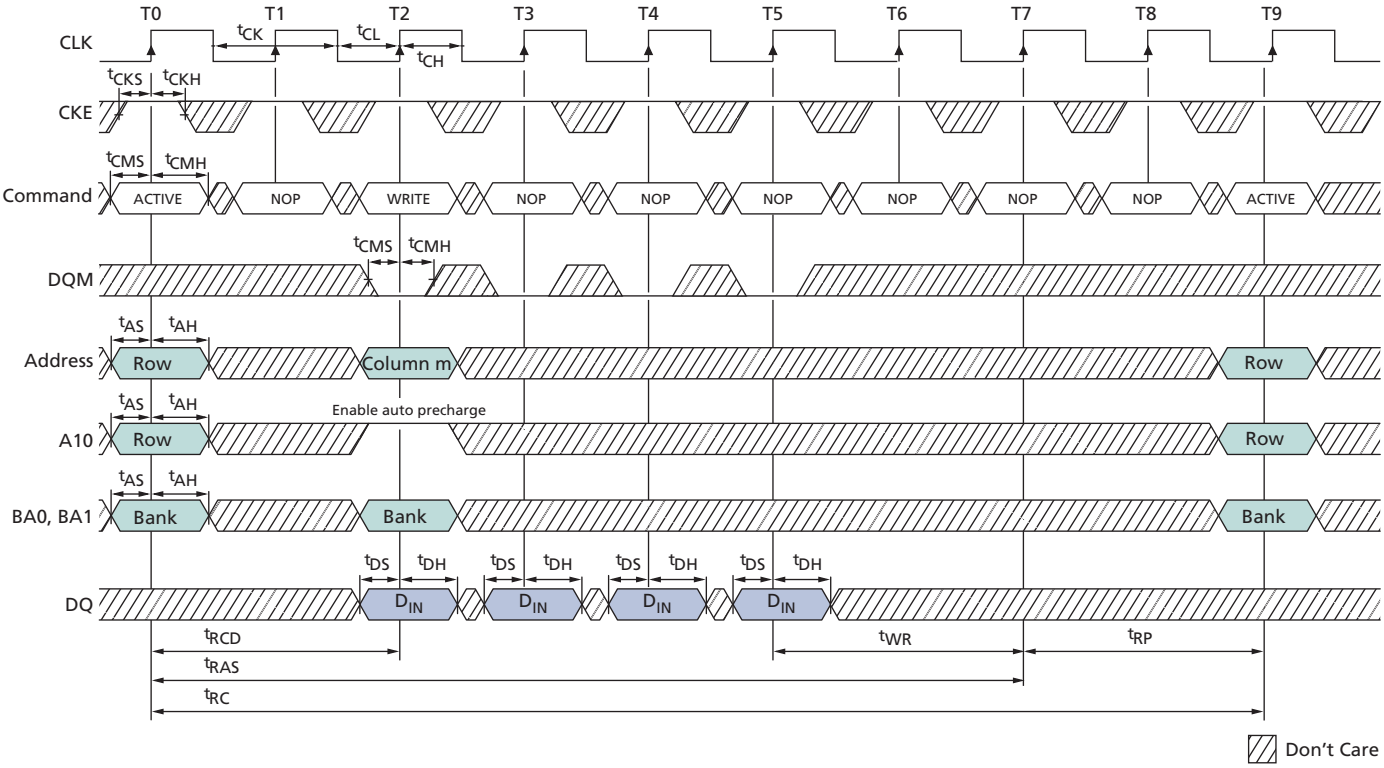
Note: 1. DQM is LOW.

Figure 40: WRITE With Auto Precharge Interrupted by a WRITE



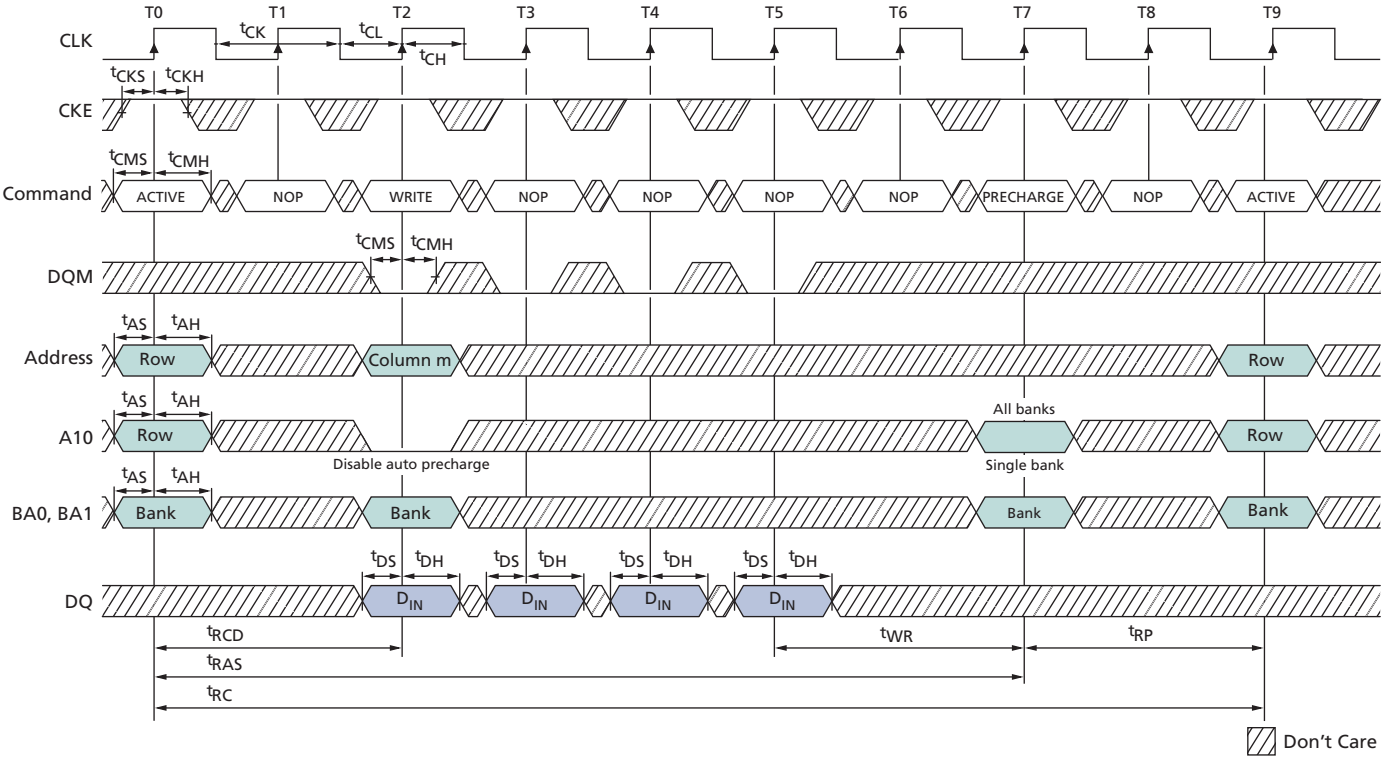
Note: 1. DQM is LOW.

Figure 41: WRITE With Auto Precharge



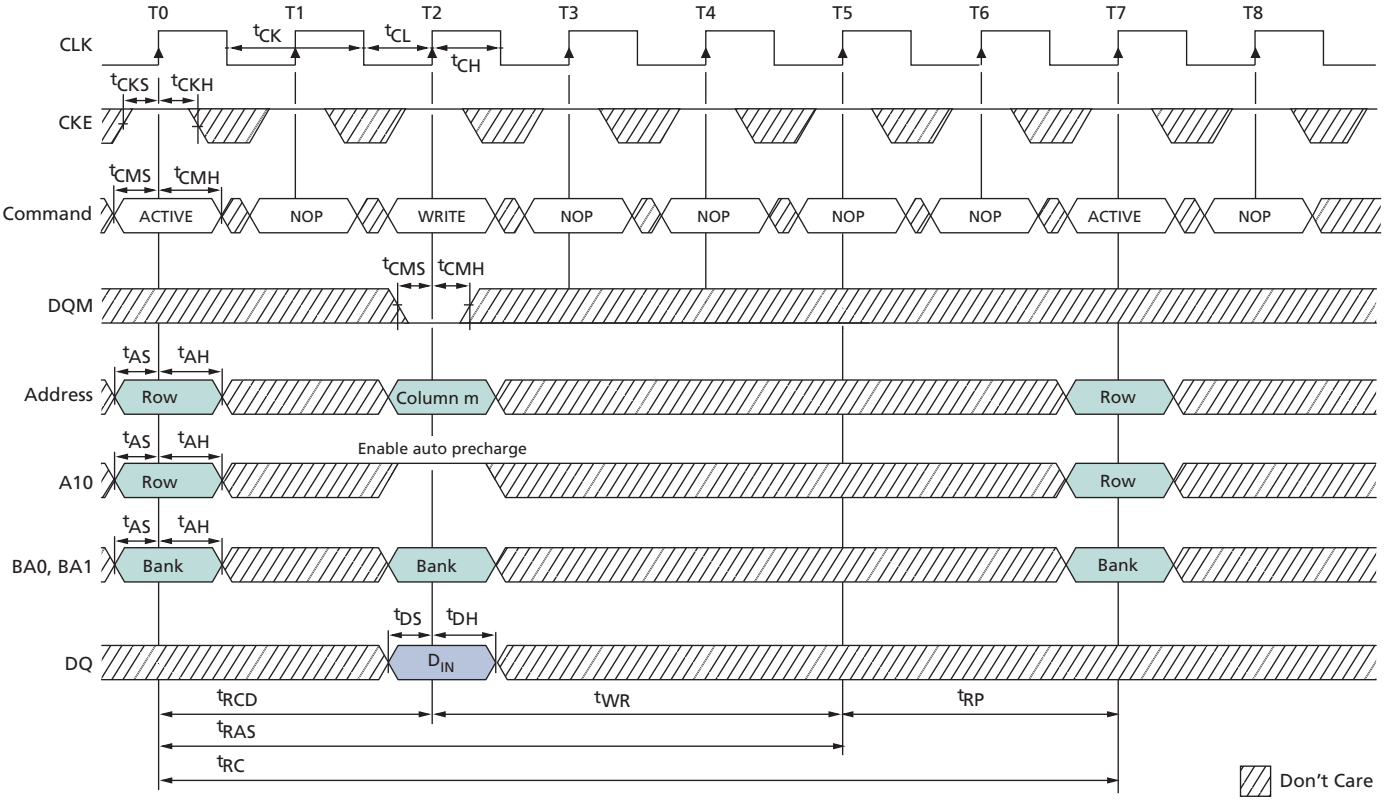
Note: 1. For this example, BL = 4.

Figure 42: WRITE Without Auto Precharge



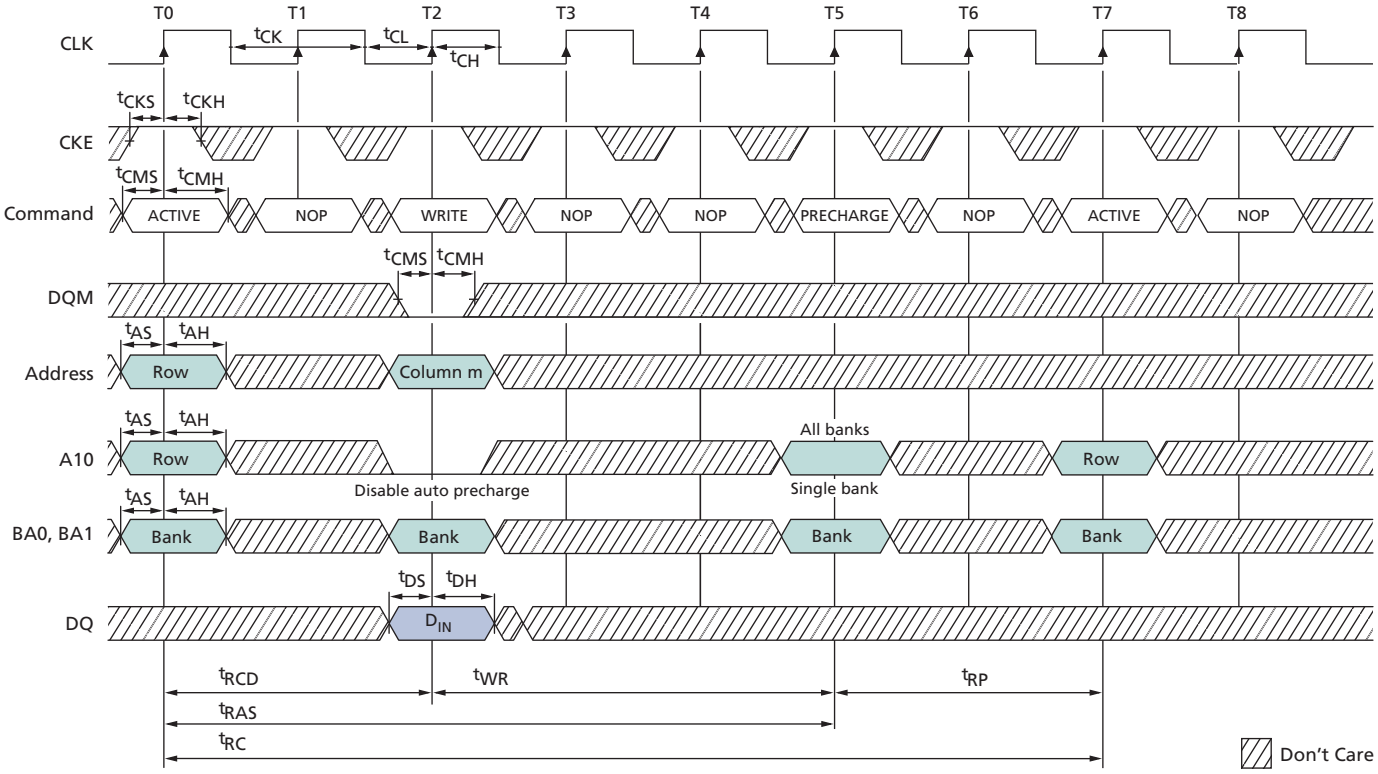
Note: 1. For this example, BL = 4 and the WRITE burst is followed by a manual PRECHARGE.

Figure 43: Single WRITE With Auto Precharge



Note: 1. For this example, BL = 1.

Figure 44: Single WRITE Without Auto Precharge



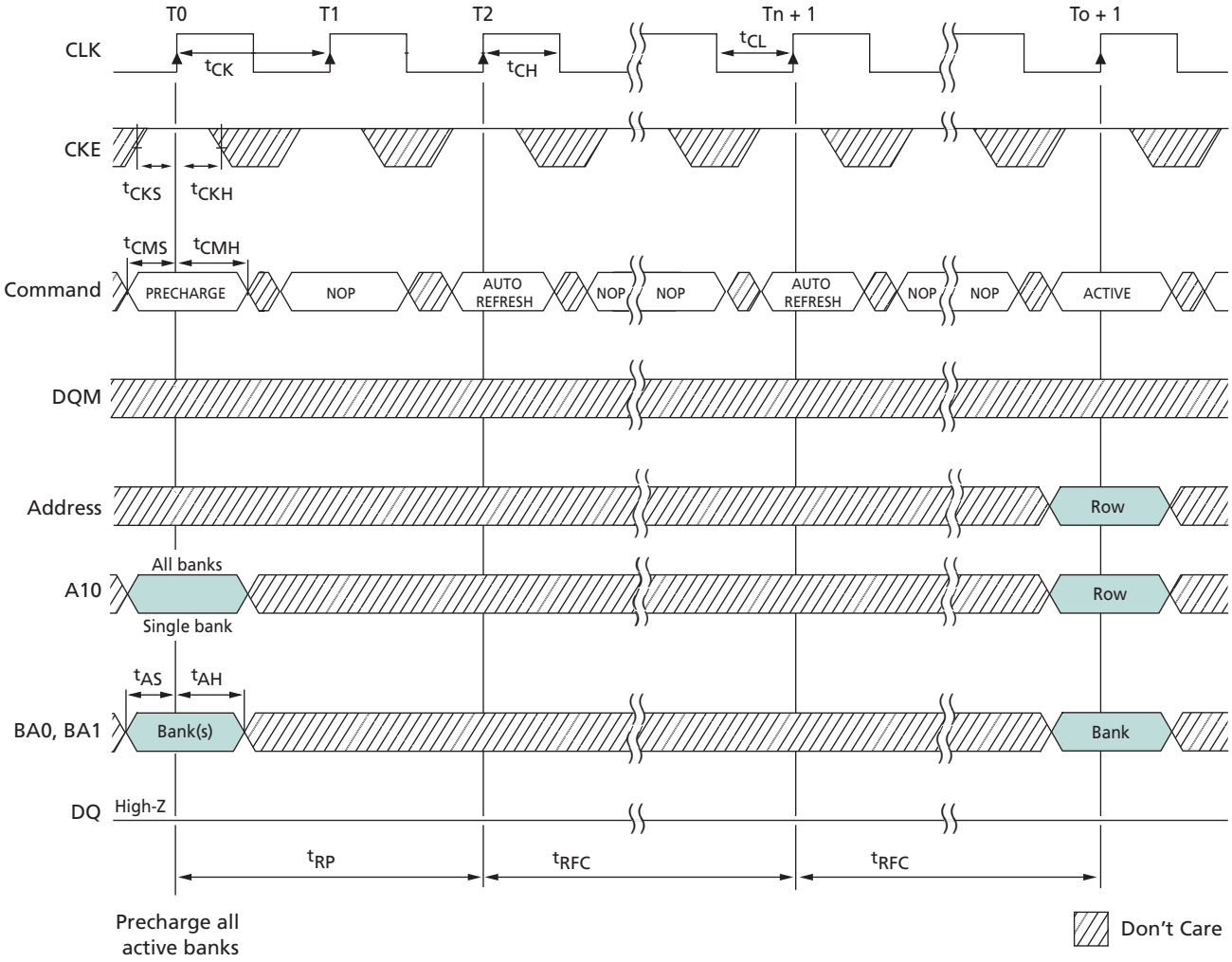
Note: 1. For this example, BL = 1 and the WRITE burst is followed by a manual PRECHARGE.

AUTO REFRESH Operation

The AUTO REFRESH command is used during normal operation of the device to refresh the contents of the array. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP is met following the PRECHARGE command. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

After the AUTO REFRESH command is initiated, it must not be interrupted by any executable command until ^{t}RFC has been met. During ^{t}RFC time, COMMAND INHIBIT or NOP commands must be issued on each positive edge of the clock. The SDRAM requires that every row be refreshed each ^{t}REF period. Providing a distributed AUTO REFRESH command—calculated by dividing the refresh period (^{t}REF) by the number of rows to be refreshed—meets the timing requirement and ensures that each row is refreshed. Alternatively, to satisfy the refresh requirement a burst refresh can be employed after every ^{t}REF period by issuing consecutive AUTO REFRESH commands for the number of rows to be refreshed at the minimum cycle rate (^{t}RFC).

Figure 45: Auto Refresh Mode



Note: 1. Back-to-back AUTO REFRESH commands are not required.

SELF REFRESH Operation

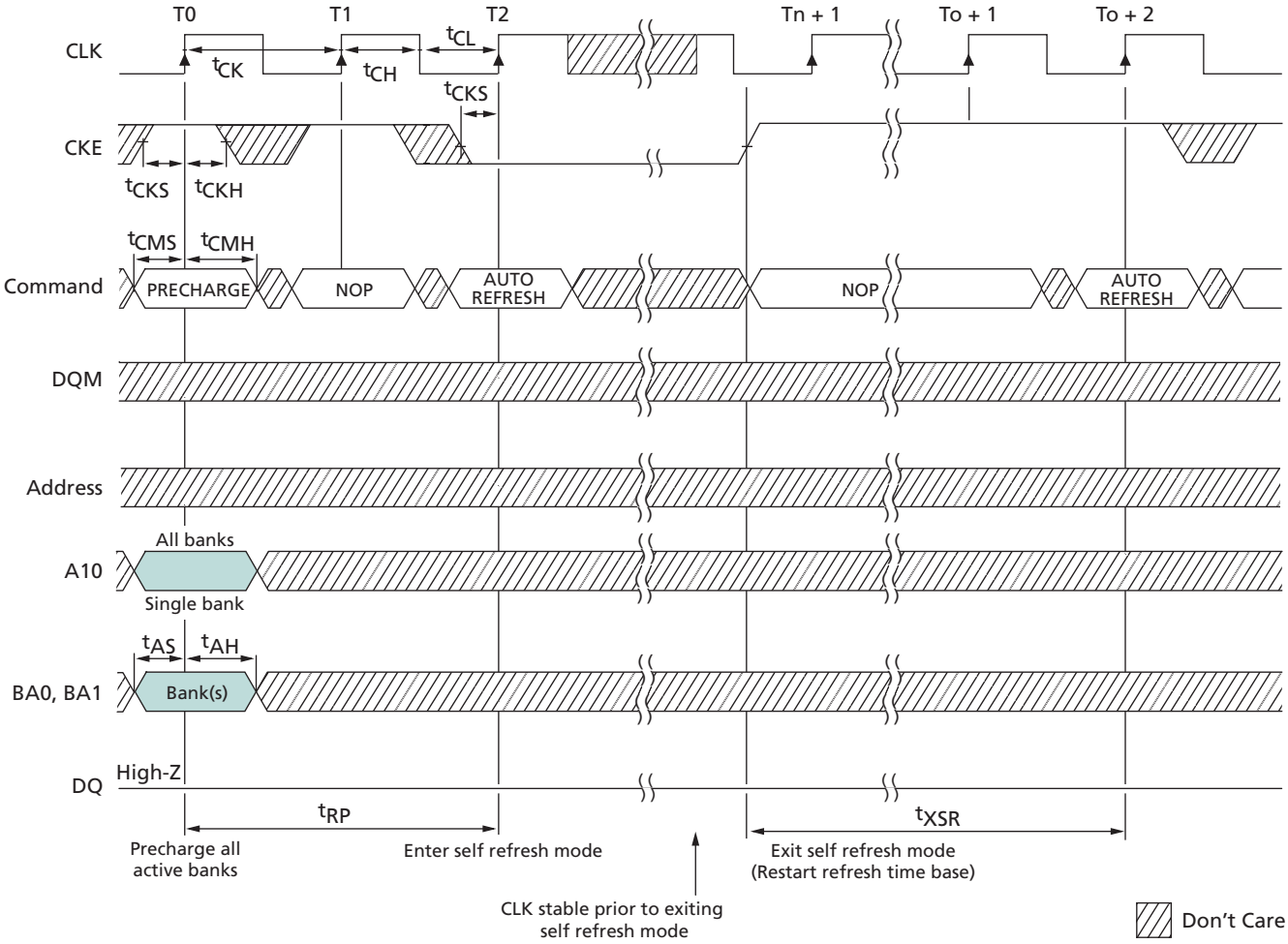
The self refresh mode can be used to retain data in the device, even when the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the device become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the device provides its own internal clocking, enabling it to perform its own AUTO REFRESH cycles. The device must remain in self refresh mode for a minimum period equal to ^{t}RAS and remains in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. (Stable clock is defined as a signal cycling within timing constraints specified for the clock ball.) After CKE is HIGH, the device must have NOP commands issued for a minimum of two clocks for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued according to the distributed refresh rate (^{t}REF/refresh row count) as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Figure 46: Self Refresh Mode



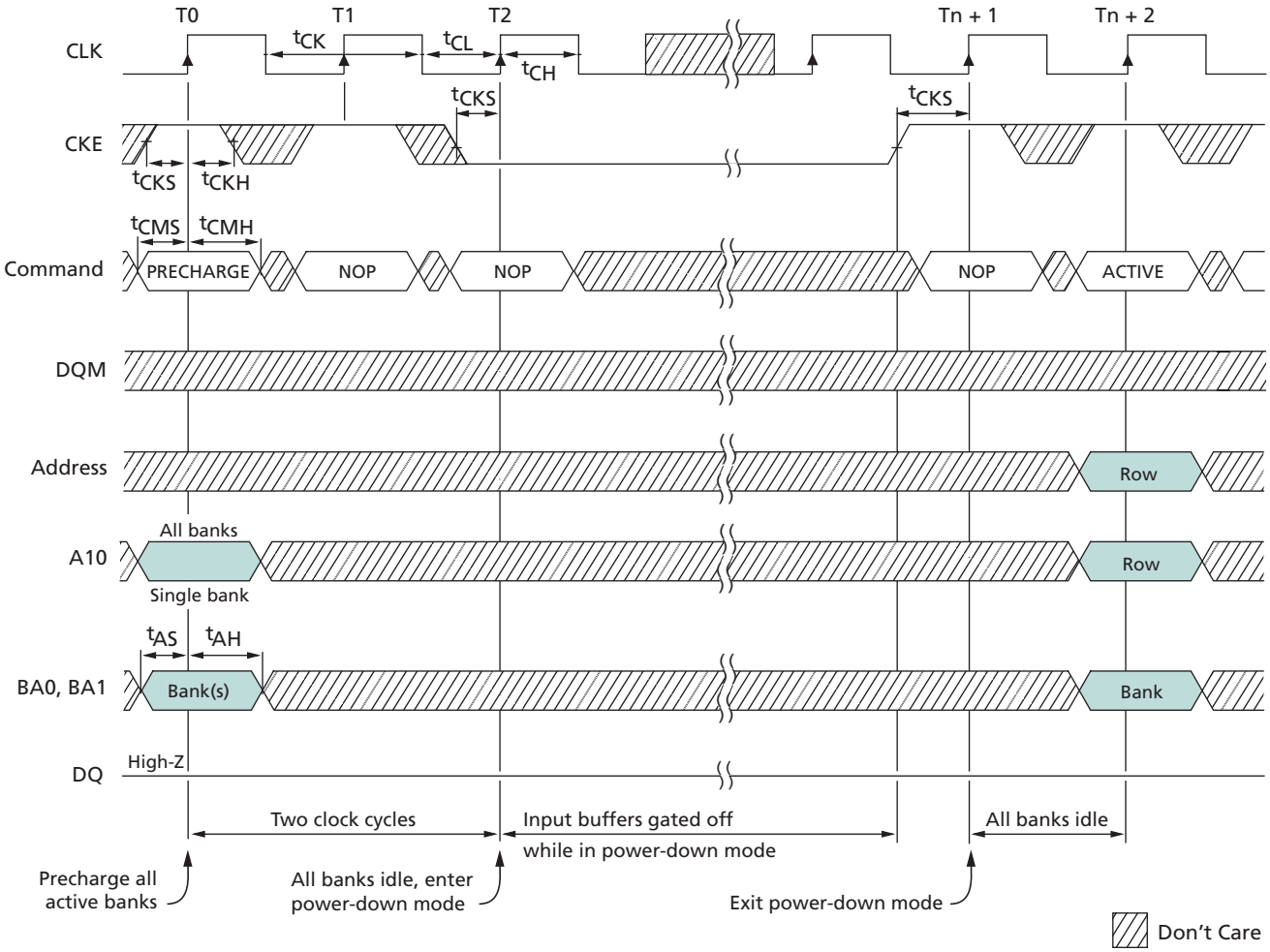
Note: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.

Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device cannot remain in the power-down state longer than the refresh period (64ms) because no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT with CKE HIGH at the desired clock edge (meeting ^{t}CKS).

Figure 47: Power-Down Mode



Note: 1. Violating refresh requirements during power-down may result in a loss of data.

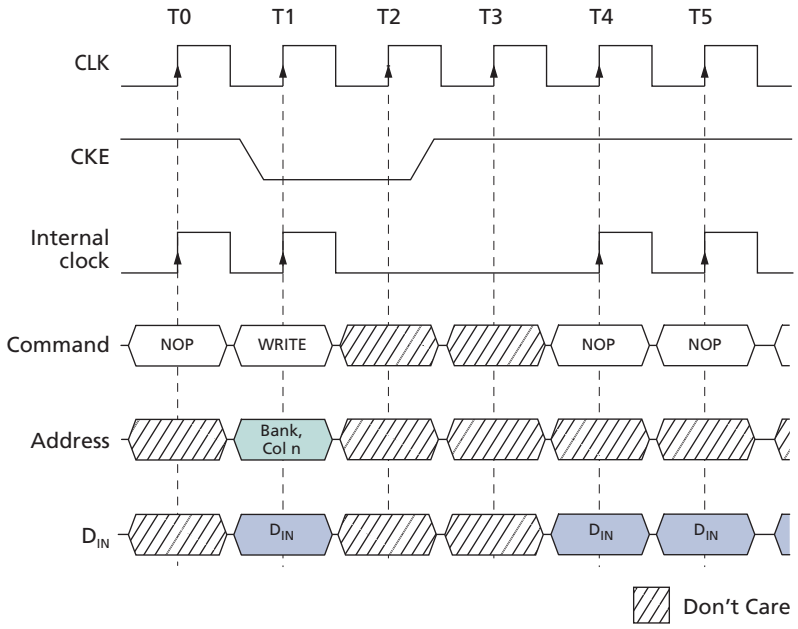
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, freezing the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls when an internal clock edge is suspended will be ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended.

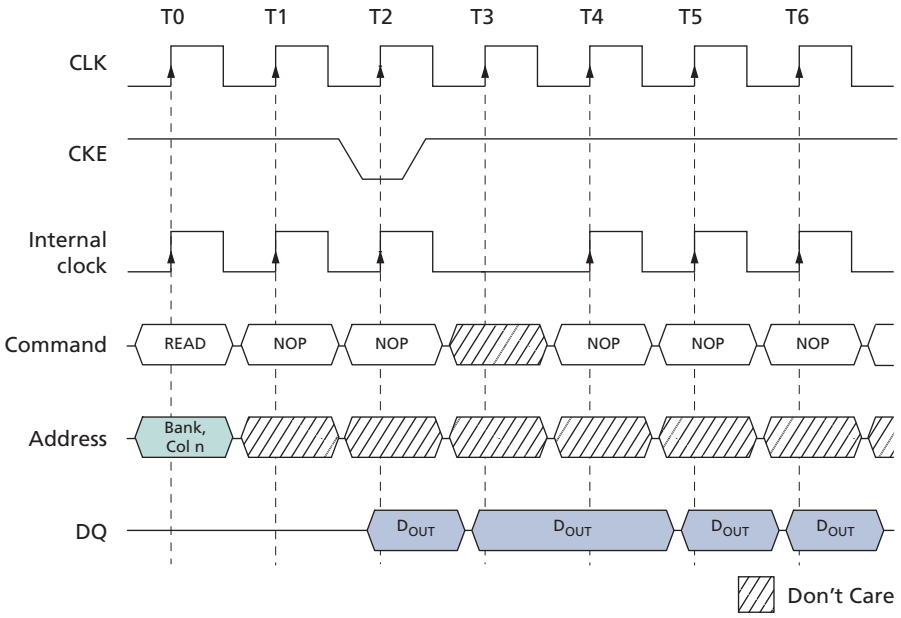
Exit clock suspend mode by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 48: Clock Suspend During WRITE Burst



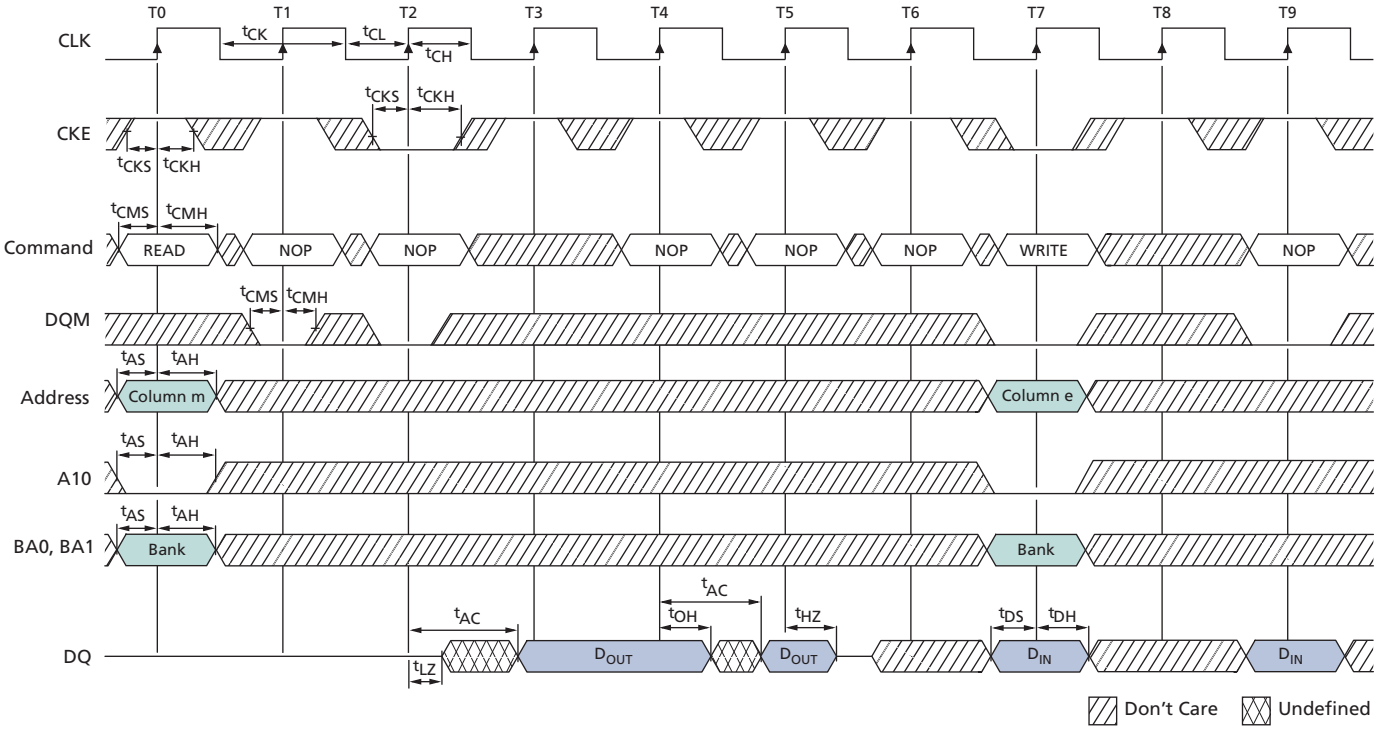
Note: 1. For this example, BL = 4 or greater, and DQM is LOW.

Figure 49: Clock Suspend During READ Burst



Note: 1. For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

Figure 50: Clock Suspend Mode



Note: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
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