

TOSHIBA Diode Silicon Epitaxial Planar Type

# 1SS361FV

Ultra-High-Speed Switching Applications

- Small package
- Excellent in forward current and forward voltage characteristics :  $V_F(3) = 0.9\text{ V (typ.)}$
- Fast reverse recovery time :  $t_{rr} = 1.6\text{ ns (typ.)}$
- Small total capacitance :  $C_T = 0.9\text{ pF (typ.)}$

### Absolute Maximum Ratings (Ta = 25°C)

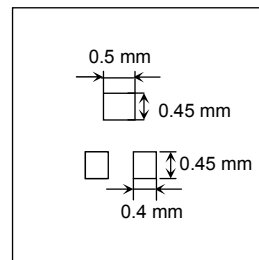
Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	85	V
Reverse voltage	$V_R$	80	V
Maximum (peak) forward current	$I_{FM}$	300 *	mA
Average forward current	$I_O$	100 *	mA
Surge current (10 ms)	$I_{FSM}$	2 *	A
Power dissipation	P	150 **	mW
Junction temperature	$T_j$	150	°C
Storage temperature range	$T_{stg}$	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

\*: Unit rating. Total rating = unit rating × 1.5

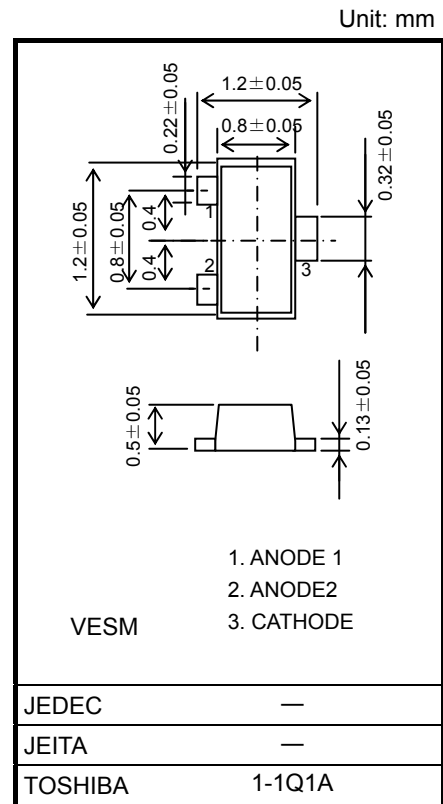
\*\* : Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm)



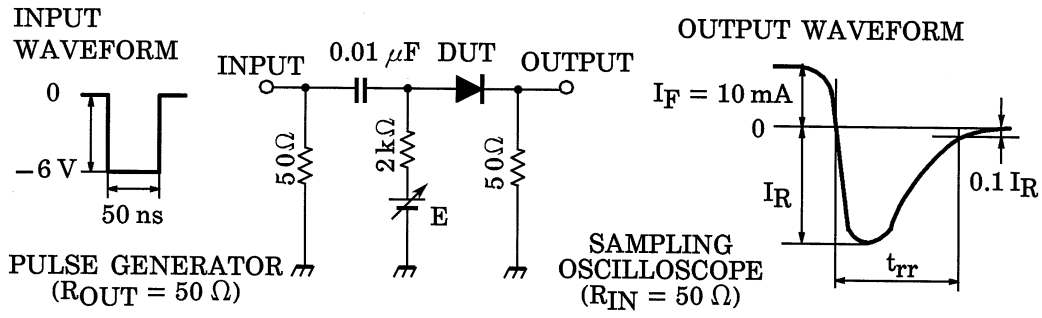
### Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	$I_F = 1\text{ mA}$	—	0.60	—	V
	$V_F(2)$	$I_F = 10\text{ mA}$	—	0.72	—	
	$V_F(3)$	$I_F = 100\text{ mA}$	—	0.90	1.2	
Reverse current	$I_R(1)$	$V_R = 30\text{ V}$	—	—	0.1	μA
	$I_R(2)$	$V_R = 80\text{ V}$	—	—	0.5	
Total capacitance	$C_T$	$V_R = 0\text{ V}, f = 1\text{ MHz}$	—	0.9	—	pF
Reverse recovery time	$t_{rr}$	$I_F = 10\text{ mA}$ (Fig. 1)	—	1.6	4.0	ns

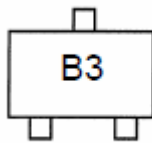
Start of commercial production  
2004-10



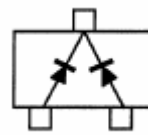
**Fig. 1 Reverse Recovery Time ( $t_{rr}$ ) Test Circuit**

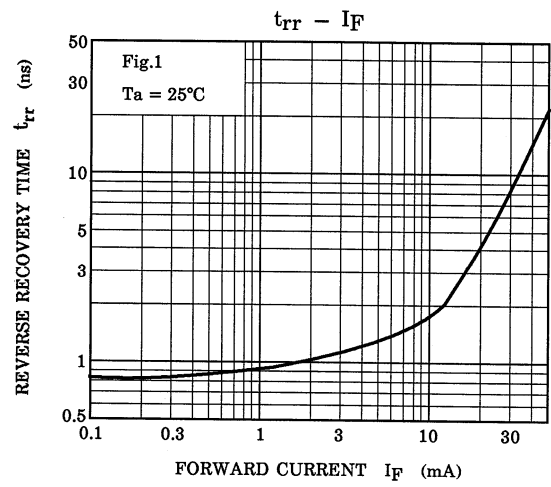
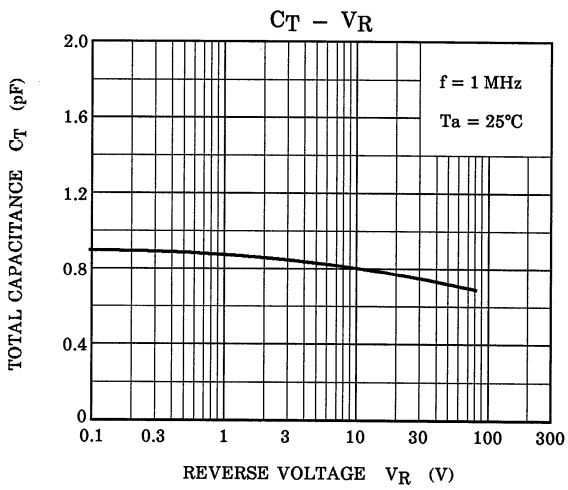
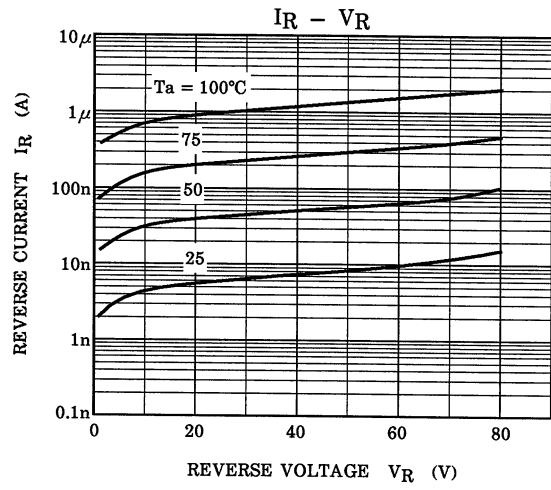
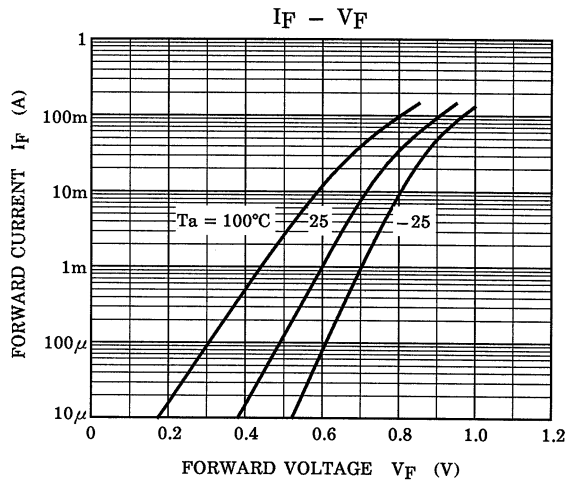


**Marking**



**Equivalent Circuit (Top View)**





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