Enpirion® Power Datasheet

ED8101 True Digital Single-Phase Single-Rail PWM controller

Description

The ED8101 is a configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies. It is optimally configured for use with the Altera ET4040 40A Power Train.

The ED8101 integrates a digital control loop that is optimized for maximum flexibility and stability as well as load step and steady-state performance. In addition, a rich set of protection functions is provided. On-chip, non-volatile memory (NVM) and an I^2C^{TM} interface facilitate configuration.

The PC-based Altera ED81xx Power Designer provides a user-friendly and easy-to-use interface to the device for communication and configuration. It can guide the user through the design of the digital compensator and offers intuitive configuration methods for additional features, such as protection and sequencing.

Reference solutions are available complete with layout recommendations, example circuit board layouts, complete bill of materials and more.

Features

- Programmable digital control loop.
- Advanced, digital control techniques
- Improved transient response and noise immunity
- Protection features
  - Over-current protection
  - Over-voltage protection (VIN, VOUT)
  - Under-voltage protection (VIN, VOUT)
  - Overloaded startup
  - Continuous retry (“hiccup”) mode for fault conditions
- Fuse-based one-time programmable (OTP) nonvolatile memory for improved reliability.
- Operation from a single 5V or 3.3V supply.
- Optional PMBus™ address selection without external resistors.

Physical Characteristics

- Operation temperature: -40°C to +85°C
- V_{OUT} max: 5V
- Lead free (RoHS compliant) 24-pin QFN package (4mm x 4mm)

Benefits

- Fast time-to-market using an off-the-shelf, optimally configured controller and power train.
- Fast configuration and design flexibility.
- FPGA designer-friendly solution.
- Simplified monitoring for system power and thermal management.
- Highest power density with smallest footprint.
- Higher energy efficiency across all output loading conditions.

Applications

- FPGA Designs
- Single-Rail/Single-Phase supplies for FPGA’s, Processors, ASIC’s, DSP’s, etc.
- Servers and Storage
- Base Stations
- Network Routers
- Industrial Applications
- Telecommunications

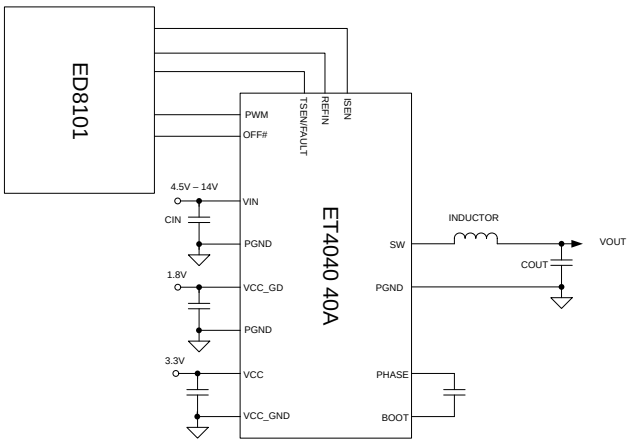

Figure 1: Simplified Applications Circuit

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
ED8101P00QI	81010	-40°C to +85°C	24-pin (4mm x 4mm x 0.95mm) QFN T&R
EVB-ED8101P00QI	Standalone 40A system evaluation board with ET4040 power train and pre-configured ED8101 digital controller.		
EVI-ED8100COMMIF	Computer communication interface		
EVK-ED8101P00QI	Evaluation Kit including the evaluation board with computer communication interface and design GUI software		

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

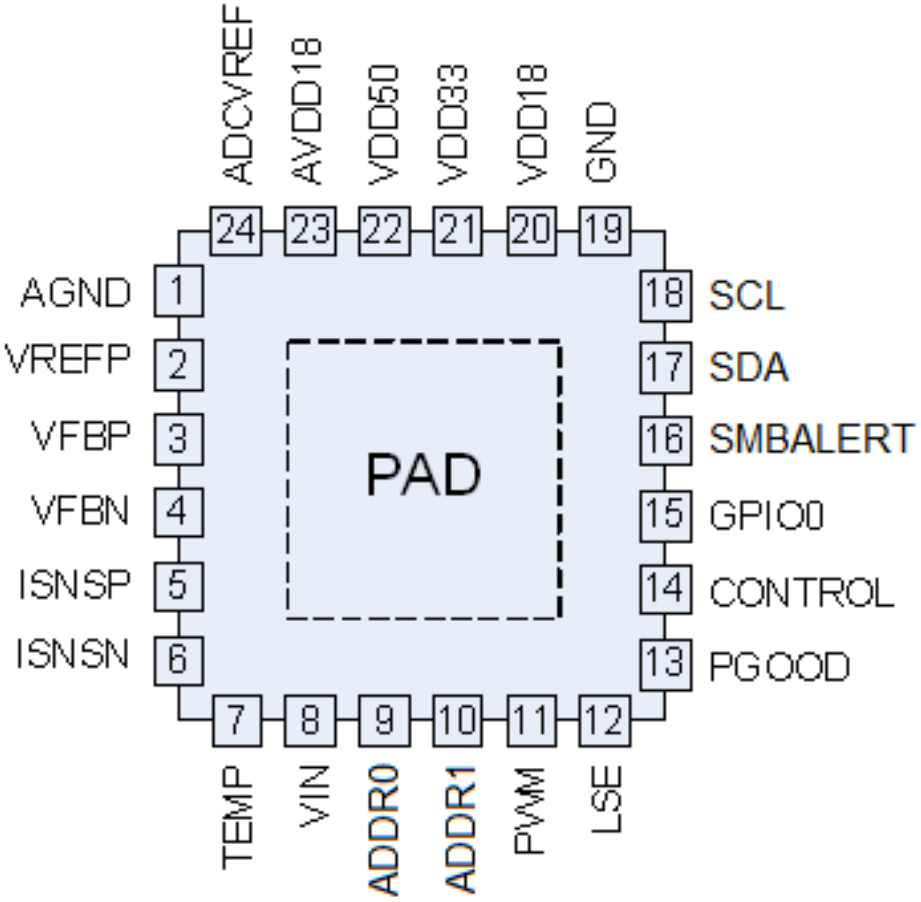

Figure 2: Pin Out Diagram (Top View)

Pin Description

Pin	Name	Direction	Type	Description
1	AGND	Input	Supply	Analog Reference Ground
2	VREFP	Output	Supply	Reference Terminal
3	VFBP	Input	Analog	Positive Input of Differential Feedback Voltage Sensing
4	VFBN	Input	Analog	Negative Input of Differential Feedback Voltage Sensing
5	ISNSP	Input	Analog	Positive Input of Differential Current Sensing
6	ISNSN	Input	Analog	Negative Input of Differential Current Sensing
7	TEMP	Input	Analog	Connection to External Temperature Sensing Element
8	VIN	Input	Analog	Power Supply Input Voltage Sensing
9	ADDR0	Input	Analog	SMBus Address Selection 0
10	CONFIG1	Input	Analog	SMBus Address Selection 1
11	PWM	Output	Digital	High-Side FET Control Signal
12	LSE	Output	Digital	Low-Side FET Control Signal
13	PGOOD	Output	Digital	PGOOD Output (Internal Pull-Down)
14	CONTROL	Input	Digital	Control Input – Active High
15	GPIO0	Input/Output	Digital	General Purpose Input/Output Pin
16	SMBALERT	Input/Output	Digital	SMBus Alert Output
17	SDA	Input/Output	Digital	SMBus Shift Data I/O
18	SCL	Input/Output	Digital	SMBus Shift Clock Input (Slave-only)
19	GND	Input	Supply	Digital Reference Ground
20	VDD18	Output	Supply	Internal 1.8 V Digital Supply Terminal
21	VDD33	Input/Output	Supply	3.3 V Supply Voltage Terminal
22	VDD50	Input	Supply	5.0 V Supply Voltage Terminal
23	AVDD18	Output	Supply	Internal 1.8 V Analog Supply Terminal
24	ADCVREF	Input	Analog	Analog-to-Digital Converter (ADC) Reference Terminal
PAD	PAD	Input	Analog	Exposed Pad, Digital Ground

IC Characteristics

Note: The absolute maximum ratings are stress ratings only. The ED8101 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. Altera does not recommend designing to the “Absolute Maximum Ratings.”

Absolute Maximum Ratings

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50	dV/dt < 0.15V/µs	-0.3		5.5	V
Maximum slew rate					0.15	V/µs
3.3 V supply voltage	VDD33		-0.3		3.6	V
1.8 V supply voltage	VDD18 AVDD18		-0.3		2.0	V
Digital pins						
Digital I/O pins	SCL SDA SMBALERT GPIO0 CONTROL PGOOD LSE PWM		-0.3		5.5	V
Analog pins						
Current sensing	ISNSP ISNSN		-0.3		5.5	V
Voltage feedback	VFBP VFBN		-0.3		2.0	V
All other analog pins	ADCVREF VREFP TEMP VIN ADDR0 ADDR1		-0.3		2.0	V
Ambient conditions						
Storage temperature	T_{STOR}		-40		150	°C
Electrostatic discharge – Human Body Model [1)]					+/-2k	V
Electrostatic discharge – Charge Device Model [1)]					+/- 500	V
Note 1: ESD testing is performed according to the respective JESD22 JEDEC standard.						

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient conditions						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operation temperature	T_{AMB}		-40		85	°C
Thermal resistance junction to ambient	θ_{JA}			40		K/W

Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage (VDD50 pin)	V_{VDD50}		4.75	5.0	5.25	V
5 V supply current	I_{VDD50}	VDD50=5.0 V		23		mA
3.3 V supply voltage	V_{VDD33}	Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used.	3.0	3.3	3.6	V
3.3 V supply current	I_{VDD33}	VDD50=VDD33=3.3 V		23		mA
Internally generated supply voltages						
3.3 V supply voltage (VDD33 pin)	V_{VDD33}	VDD50=5.0 V	3.0	3.3	3.6	V
3.3 V output current	I_{VDD33}	VDD50=5.0 V			2.0	mA
1.8 V supply voltages (AVDD18 and VDD18 pins)	V_{AVDD18} V_{VDD18}	VDD50=5.0 V	1.72	1.80	1.98	V
1.8 V output current					0	mA
Power-on reset threshold for VDD33 pin – on	$V_{TH\_POR\_ON}$			3.0		V
Power-on reset threshold for VDD33 pin – off	$V_{TH\_POR\_OFF}$			2.8		V
Digital IO pins (GPIO0, CONTROL, PGOOD)						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Input leakage current					±1	µA
Output current - high					2.0	mA
Output current - low					2.0	mA
Digital IO pins with tri-state capability (LSE, PWM)						
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Output current - high					2.0	mA
Output current - low					2.0	mA
Tri-state leakage current					±1.0	µA
SMBus pins (SCL, SDA, SMBALERT) – open drain						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input high voltage		VDD33=3.3V	2.0			V
Input low voltage		VDD33=3.3V			0.8	V
Maximum bus voltage					5.25	V
Output current – low					2.0	V
Output voltage (without external feedback divider)						
Set-point voltage			0		1.4	V
Set-point resolution				1.4		mV
Set-point accuracy		VOUT=1.2 V		1		%
Inductor current measurement						
Common mode voltage -	ISNSP ISNSN		0		5.0	V
Differential voltage range across ISNSP and ISNSN pins					±100	mV
Accuracy				5		%
Digital pulse width modulator						
Switching frequency	f_{SW}		500		1000	kHz
Resolution				163		ps
Frequency accuracy				2.0		%
Duty Cycle			2.5		100	%
Over-voltage protection						
Reference DAC						
Set-point voltage			0		1.58	V
Resolution				25		mV
Set point accuracy				2		%
Comparator						
Hysteresis				35		mV
Housekeeping analog-to-digital converter (HKADC) input pins						
Input voltage	TEMP VIN ADDR0 ADDR1		0		1.44	V
Source impedance Vin sensing					3	kΩ
ADC resolution				0.7		mV
External temperature measurement (PN-junction, voltage input with positive/negative temperature coefficient sense elements are supported)						
Bias currents for external temperature sensing	TEMP	Use PN-junction		60		µA
Bias currents for external temperature sensing	TEMP	Use voltage input		0		µA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	TEMP			0.32		K
Accuracy of measurement	TEMP			±5.0		K
Internal temperature measurement						
Resolution				0.22		K
Accuracy of measurement				±5.0		K

Functional Block Diagram

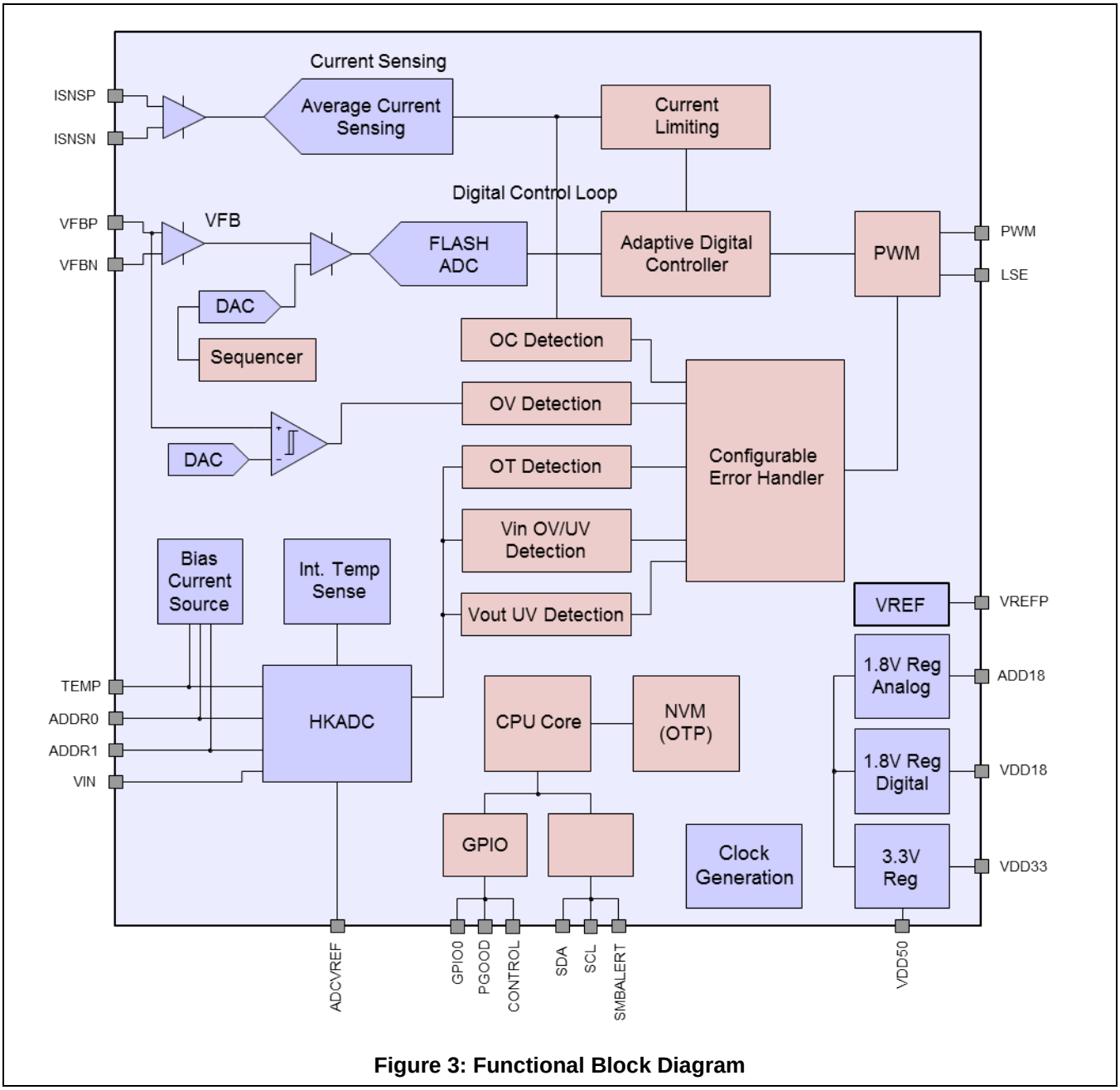

Figure 3: Functional Block Diagram

Functional Description

Overview

The ED8101 is configurable true-digital single-phase PWM controller for high-current, non-isolated DC/DC supplies supporting switching frequencies up to 1 MHz. It is optimally configured for use with the Altera Power Solutions 40A Power Train ET4040. The ED8101 offers a PMBus™ configurable digital power control loop incorporating output voltage sensing, average inductor current sensing, and extensive fault monitoring and handling features. Several different functional units are integrated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature.

An application-specific, low-energy integrated microcontroller is used to control the overall system. It manages configuration of the various logic units and handles the PMBus™ communication protocol. A PMBus™/SMBus/I²C™ interface is incorporated to connect with the outside world; supported by control and power-good signals.

A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Power Supply Circuitry, Reference Decoupling, and Grounding

The ED8101 incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator should be used. If the internal 3.3V regulator is not used, 3.3V must be supplied to the 3.3V and 5V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e., the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example.

The reference voltages required for the analog-to-digital converters are generated within the ED8101. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7µF capacitor is required at the VREFP pin, and a 100nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections (the pad, AGND pin, and GND pin) are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

Reset/Start-up Behavior

The ED8101 employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage, the ED8101 begins the internal start-up process. Upon its completion, the device is ready for operation.

Digital Power Control

Overview

The digital power control loop consists of the integral parts required for the control functionality of the ED8101. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM that controls the drive signals to the power stage.

Switching Frequency

The ED8101 supports the switching frequencies listed in Table 1.

Table 1: Supported Switching Frequencies

1000 kHz	666.6 kHz
888 kHz	571.4 kHz
800 kHz	500.0 kHz

Output Voltage Feedback

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is

differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

Although the reference DAC generates a voltage up to 1.44V, keeping the voltage on the feedback pin (VFBP) at approximately 1.20V is recommended to guarantee sufficient headroom. If a larger output voltage is required, an external feedback divider is required.

Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. This digital control loop works as a voltage-mode controller using PID-type compensation. The basic structure of the controller is shown in Figure 4. The controller features two parallel compensators, steady-state operation, and fast transient operation. The ED8101 implements fast, reliable switching between the different compensation modes in order to ensure good transient performance and quiet steady state. This has been utilized to tune the compensators individually for the respective needs; i.e. quiet steady-state and fast transient performance.

Three different techniques are used to improve transient performance further:

- Phase-lag reducing sampling technology is used to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any change in output voltage.
- The technique to drive the DPWM asynchronously during load transients, allows limiting the maximum deviation of the output voltage and recharging the output capacitors faster.
- A nonlinear gain adjustment is used during large load transients to boost the loop gain and reduce the settling time.

Power Sequencing and the CONTROL Pin

The ED8101 supports power-sequencing features such as programmable ramp up/down and delays. The typical sequence of events is shown in Figure 5. The CONTROL pin is configured for active high operation.

The ED8101 features a power good (PGOOD) output, which can be used to indicate the state of the power rail. If the output voltage level is above the power good ON threshold, the pin is set to active, indicating a stable output voltage on the rail. Different levels for turn-on and turn-off are used to enable the use of a hysteresis if desired. Note that the power good thresholds are stored in the device as factors relative to the nominal output voltage. Hence, using the strapping options to change the output voltage level also changes the PGOOD thresholds.

Pre-biased Start-up and Soft-Off

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

ED8101 also supports pre-biased off, i.e. the output voltage is not ramped down to zero and instead remains at a predefined level (V_{OFF_nom}). This value can be configured via the ED81xx Power Designer. After receiving the shutdown command, via PMBusTM or the CONTROL pin, the ED8101 will execute the soft-off sequence. The soft-off sequence will ramp down the output voltage to the predefined value. Once the value is reached, the PWM will be turned off in order to put the output driver into tri-state mode.

Current Sensing

The ED8101 offers cycle-by-cycle average current sensing with configurable over-current protection. A dedicated ADC is used to provide fast and accurate current information over the switching period. The acquired information is compared with the configurable current thresholds to report warning and error levels to the user. DCR current sensing across the inductor and dedicated shunt resistors are supported. This part works the best with ET4040 which provides a voltage based replica of the dynamic inductor current waveform (ISEN). Additionally, this ISEN signal is internally temperature compensated, allowing the ISEN indication to correctly track output current even as internal junction temperature changes due to self-heating and due to changes in ambient temperature. Figure 6 shows the current sensing circuit with ET4040.

End-of-line calibration is supported so that the ED8101 can achieve improved accuracy over the full output current range. The full calibration method is detailed in the appropriate application note.

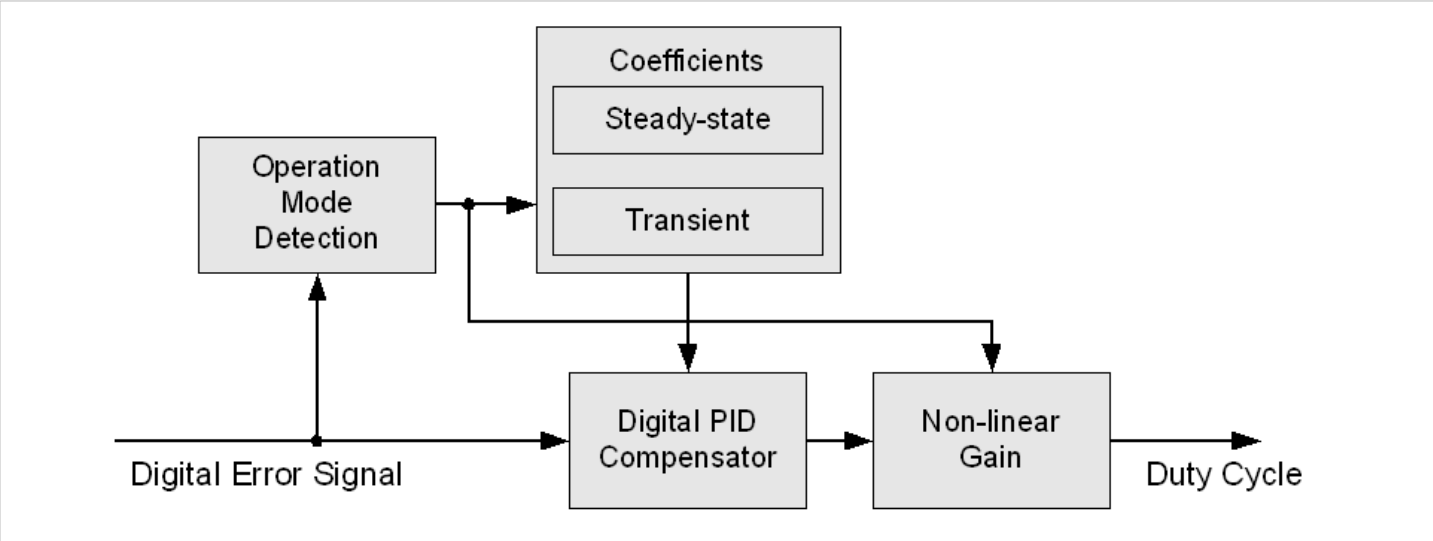

Figure 4: Simplified Block Diagram for the Digital Compensation

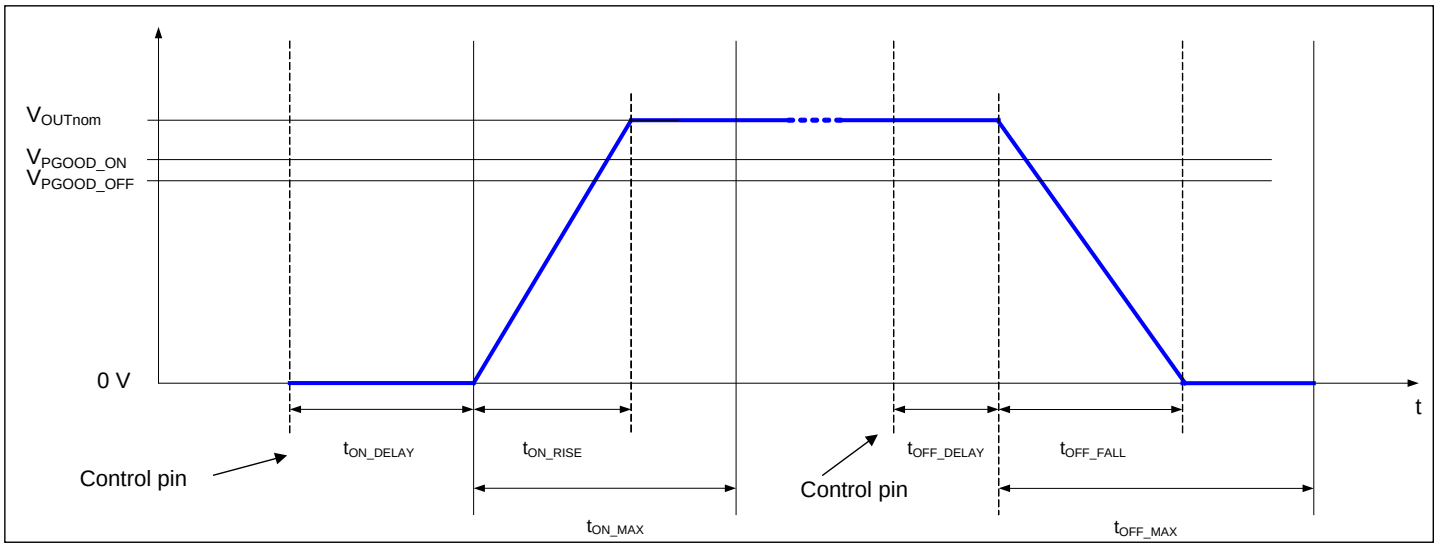

Figure 5: Power Sequencing

Temperature Measurement

The ED8101 features two independent temperature measurement units. The internal temperature sensing measures the temperature inside the IC; the external temperature sensing measures the voltage on the TEMP pin, which is coming from the TSEN temperature monitoring signal of Altera power train ET4040. This signal provides a thermal monitor that indicates the internal junction temperature of the ET4040. A temperature calibration is highly recommended.

Fault Monitoring and Response Generation

The ED8101 monitors various signals for possible fault conditions during operation, it can respond to events generated by these signals. A wide range of options is configurable via the ED81xx Power Designer. Typical monitoring within the ED8101 is a three step process. First, an event is generated by a configurable set of thresholds. This event is then digitally filtered before the ED8101 reacts with a response. For most monitored signals, a warning and a fault threshold can be configured. A warning typically sets a status flag, but does not trigger a response, whereas a fault also generates a response. The fault responses of the ED8101 controller are given in Table 2.

Each warning and fault event can be individually enabled. Also the assertion of the SMBALERT signal can be configured to individual needs. The

controller fault handling will infinitely try to restart the converter on some of the fault conditions. In analog controllers, this infinite re-try feature is also known as “hiccup mode.”

Output Over/Under Voltage

To prevent damage to the load, the ED8101 utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM output is set to low. The voltage fault level is generated by a 6-bit DAC with a reference voltage of 1.60V resulting in 25mV resolution.

The ED8101 also monitors the output voltage with a lower threshold. If the output voltage falls below the under-voltage fault level, a fault event is generated and the PWM output is set to tri-state condition.

Table 2: Fault Configuration Overview

Fault	Retries	Response
Output Over-Voltage	None	Low
Output Under-Voltage	Infinity	High-Z
Input Over-Voltage	Infinity	High-Z
Input Under-Voltage	Infinity	High-Z
Over-Current	Infinity	High-Z
External Over-Temperature	Infinity	Soft-off
Internal Over-Temperature	Infinity	Soft-off

Output Current Protection

The ED8101 continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current.

Over-Temperature Protection

The ED8101 monitors internal and external temperature. For each, a warning and a fault level can be configured and an appropriate response can be enabled. For the temperature fault conditions a soft-off sequence is started. The soft-off sequence will ramp down the output voltage to 0V and set the PWM output in a tri-state condition.

Configuration and Engineering Mode

The ED8101 incorporates two different sets of configuration parameters. The first set of configuration parameters can be configured during design time and cannot be changed during run-time. The second set of configuration parameters can be configured during design time, but can also be reconfigured during run-time using the appropriate PMBus™ command. Note that these reconfigured values not stored in the OTP memory, so they are lost during power cycling the device.

In order to evaluate the device and its configuration on the bench, a special engineering mode is supported by the device and the ED81xx Power Designer. In this mode, the device can be reconfigured multiple-times without writing the configuration into the OTP. During this “engineering mode”, the device starts up after power-on reset in an unfigured state or a configured state if the OTP has already been configured. The ED81xx Power Designer then provides the configuration to the ED8101 enabling full operation without actually configuring the OTP. The user can use this mode to evaluate the configuration on the bench. However, the configuration will be lost upon power-on-reset.

After the user has determined the final configuration options, a configuration file or OTP image can be created that is then written into the ED8101. This can be either on the bench using the ED81xx Power Designer or in end-of-line testing during mass production.

PMBus™ Functionality

Introduction

The ED8101 supports the PMBus™ protocol to enable the use of configuration, monitoring and fault management during run-time.

The PMBus™ host controller is connected to the ED8101 via the PMBus™ pins. A dedicated SMBALERT pin is provided to notify the host that new status information is present.

The ED8101 supports packet error correction (PEC) according to the PMBus™ specification.

Timing and Bus Specification

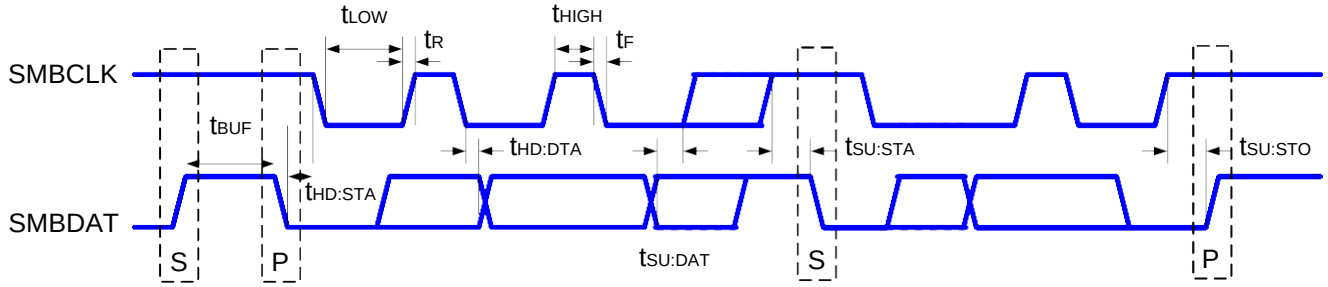

Figure 6: PMBus™ Timing Diagram

Table 3: PMBus™ Timing Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus operation frequency	f_{SMB}		10	400	500	kHz
Bus free time between start and stop	t_{BUF}		1.3			µs
Hold time after start condition	$t_{HD:STA}$		0.6			µs
Repeat start condition setup time	$t_{SU:STA}$		0.6			µs
Stop condition setup time	$t_{SU:STO}$		0.6			µs
Data hold time	$t_{HD:DAT}$		300			ns
Data setup time	$t_{SU:DAT}$		100			ns
Clock low time-out	$t_{TIMEOUT}$			25	35	µs
Clock low period	t_{LOW}		1.3			µs
Clock high period	t_{HIGH}		0.6			µs
Cumulative clock low extend time	$t_{LOW:SEXT}$				1	ms
Clock or data fall time	t_F				300	ns
Clock or data rise time	t_R				300	ns

Address Selection via External Resistors

PMBus™ uses a 7-bit device address to identify different devices connected to the bus. This address can be selected via external resistors connected to the ADDRx pins.

The resistor values are sensed using the internal ADC during the initialization phase and the appropriate PMBus™ address is selected. Note that the respective circuitry is only active during the initialization phase; hence no DC voltage can be measured at the pins. The supported PMBus™ addresses and the values of the respective required resistors are listed in Table 4.

If only four devices are used in a system, their respective addresses can alternatively be configured without resistors by connecting the pins to GND or AVDD18 pin. The PMBus™ addresses selectable in this fashion are listed in Table 5.

Table 4: Supported Resistor Values for PMBus™ Address Selection

Address (Hex)	ADDR1 Ω	ADDR0 Ω	Address (Hex)	ADDR1 Ω	ADDR 0 Ω	Address (Hex)	ADDR1 Ω	ADDR 0 Ω	Address (Hex)	ADDR1 Ω	ADDR0 Ω
0x40	0	0	0x20	3.3 k	0	0x40	8.2 k	0	0x60	15.0 k	0
0x02*	0	1.5 k	0x22	3.3 k	1.5 k	0x42	8.2 k	1.5 k	0x62	15.0 k	1.5 k
0x04*	0	3.3 k	0x24	3.3 k	3.3 k	0x44	8.2 k	3.3 k	0x64	15.0 k	3.3 k
0x06*	0	5.6 k	0x26	3.3 k	5.6 k	0x46	8.2 k	5.6 k	0x66	15.0 k	5.6 k
0x08*	0	8.2 k	0x28*	3.3 k	8.2 k	0x48	8.2 k	8.2 k	0x68	15.0 k	8.2 k
0x0A	0	12.0 k	0x2A	3.3 k	12.0 k	0x4A	8.2 k	12.0 k	0x6A	15.0 k	12.0 k
0x0C*	0	15.0 k	0x2C	3.3 k	15.0 k	0x4C	8.2 k	15.0 k	0x6C	15.0 k	15.0 k
0x0E	0	22.0 k	0x2E	3.3 k	22.0 k	0x4E	8.2 k	22.0 k	0x6E	15.0 k	22.0 k
0x10	1.5 k	0	0x30	5.6 k	0	0x50	12.0 k	0	0x70	22.0 k	0
0x12	1.5 k	1.5 k	0x32	5.6 k	1.5 k	0x52	12.0 k	1.5 k	0x72	22.0 k	1.5 k
0x14	1.5 k	3.3 k	0x34	5.6 k	3.3 k	0x54	12.0 k	3.3 k	0x74	22.0 k	3.3 k
0x16	1.5 k	5.6 k	0x36	5.6 k	5.6 k	0x56	12.0 k	5.6 k	0x76	22.0 k	5.6 k
0x18	1.5 k	8.2 k	0x38	5.6 k	8.2 k	0x58	12.0 k	8.2 k	0x78*	22.0 k	8.2 k
0x1A	1.5 k	12.0 k	0x3A	5.6 k	12.0 k	0x5A	12.0 k	12.0 k	0x7A*	22.0 k	12.0 k
0x1C	1.5 k	15.0 k	0x3C	5.6 k	15.0 k	0x5C	12.0 k	15.0 k	0x7C*	22.0 k	15.0 k
0x1E	1.5 k	22.0 k	0x3E	5.6 k	22.0 k	0x5E	12.0 k	22.0 k	0x7E*	22.0 k	22.0 k

Note: * These addresses are reserved by the SMBus specification.

Table 5: PMBus™ Address Selection without Resistors

Address	ADDR1	ADDR0
0x0E	GND	AVDD18
0x70	AVDD18	GND
0x0F	AVDD18	AVDD18
0x40	GND	GND

Configuration

Two different sets of configuration parameters are supported by the ED8101. The first set of parameters can only be configured during the configuration phase of the ED8101. These values are written into the OTP memory and cannot be changed using PMBus™ commands during run-time. A second set of parameters can also be configured also during run-time using the appropriate PMBus™ commands. The two groups are classified in the PMBus™ configuration table (Table 6).

The ED8101 supports the LINEAR data format according to the PMBus™ specification. Note that in accordance with the PMBus™ specification, all commands related to the output voltage are subject to the VOUT_MODE settings. Note that VOUT_MODE is read-only for the ED8101.

Table 6: List of Supported PMBus™ Configuration Registers

PMBus™ Parameter	Description	Data Format	Classification
Output Voltage			
ON_OFF_CONFIG	On/off configuration	N/A	OTP
VOUT_MODE	Exponent of the VOUT_COMMAND value	N/A	Read only
VOUT_COMMAND	Set output voltage	LINEAR (1)	PMBus™
VOUT_OV_FAULT_LIMIT	Over-voltage fault limit	N/A	OTP
VOUT_OV_FAULT_RESPONSE	Over-voltage fault response	N/A	OTP
VOUT_OV_WARN_LIMIT	Over-voltage warning level	N/A	OTP
VOUT_UV_WARN_LIMIT	Under-voltage warning level	N/A	OTP
VOUT_UV_FAULT_LIMIT	Under-voltage fault level	N/A	OTP
VOUT_UV_FAULT_RESPONSE	Under-voltage fault response	N/A	OTP
Output Current			
IOUT_OC_FAULT_LIMIT	Over-current fault limit	N/A	OTP
IOUT_OC_FAULT_RESPONSE	Over-current fault response	N/A	OTP
IOUT_OC_LV_FAULT_LIMIT	Voltage threshold during constant-current mode	N/A	OTP
IOUT_OC_WARN_LIMIT	Over-current warning level	N/A	OTP
Temperature - External			
OT_FAULT_LIMIT	Over-temperature fault level	N/A	OTP
OT_FAULT_RESPONSE	Over-temperature fault response	N/A	OTP
OT_WARN_LIMIT	Over-temperature warning level	N/A	OTP
Temperature - Internal			
IOT_FAULT_LIMIT	Over-temperature fault level	N/A	OTP
IOT_FAULT_RESPONSE	Over-temperature fault response	N/A	OTP
IOT_WARN_LIMIT	Over-temperature warning level	N/A	OTP
Input Voltage			
VIN_OV_FAULT_LIMIT	Over-voltage fault limit	N/A	OTP
VIN_OV_FAULT_RESPONSE	Over-voltage fault response	N/A	OTP
VIN_OV_WARN_LIMIT	Over-voltage warning level	N/A	OTP
VIN_UV_WARN_LIMIT	Under-voltage warning level	N/A	OTP
VIN_UV_FAULT_LIMIT	Under-voltage fault level	N/A	OTP

VIN_UV_FAULT_RESPONSE	Under-voltage fault response	N/A	OTP
Start-up Behavior / Power Sequencing			
POWER_GOOD_ON	Power good on threshold	N/A	OTP
POWER_GOOD_OFF	Power good off threshold	N/A	OTP
Output Voltage Sequencing			
TON_DELAY	Turn-on delay	N/A	OTP
TON_RISE	Turn-on rise time	N/A	OTP
TON_FAULT_MAX	Turn-on maximum fault time	N/A	OTP
TOFF_DELAY	Turn-off delay	N/A	OTP
TOFF_FALL	Turn-off fall time	N/A	OTP
TOFF_WARN_MAX	Turn-off maximum warning time	N/A	OTP
VOFF_NOM	Soft-stop off value	N/A	OTP
Notes1. VOUT_MODE is read-only for this device.			

Monitoring

The ED8101 has a dedicated set of PMBus™ registers to enable advanced power management using extensive monitoring features. Different warning and error flags can be read by the PMBus™ master to ensure proper operation of the power converter or monitor the converters over its life time.

Table 7: List of Supported PMBus™ Status Register

PMBus™ Command	Description	Data Format
CLEAR_FAULTS	Clear status information	
STATUS_BYTE	Unit status byte	
STATUS_WORD	Unit status word	
STATUS_VOUT	Output voltage status	
STATUS_IOUT	Output current status	
STATUS_INPUT	Input status	
STATUS_TEMPERATURE	Temperature status	
STATUS_CML	Communication and memory status	
READ_VIN	Input voltage read back	LINEAR
READ_VOUT	Output voltage read back	LINEAR
READ_IOUT	Output current read back	LINEAR
READ_TEMPERATURE_1	External temperature read back	LINEAR
READ_TEMPERATURE_2	Internal temperature read back	LINEAR

PMBus™ Command	Description	Data Length (Byte)	Values
PMBUS_REVISION	PMBus™ revision	1	0x11
MFR_ID	Manufacturer ID	4	“ALTR” (0x41, 0x4C, 0x54, 0x52)
MFR_MODEL	Manufacturer model identifier	4	“8101” (0x38, 0x31, 0x30, 0x31)
MFR_REVISION	Manufacturer product revision	4	
MFR_SERIAL	Serial number	12	

Detailed Description of the Supported PMBus™ Commands

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the CONTROL pin. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the CONTROL pin instructs the device to change to another mode. The supported operation modes are listed in Table 8.

Table 8: Supported PMBus™ Operation Modes

OPERATION (read/write)					
Bits[7:6]	**Bits[5:4]**	**Bits[3:2]**	**Bits[1:0]**	**Unit On or Off**	**Margin State**
01	XX	XX	XX	Soft Off (With Sequencing)	N/A
10	00	XX	XX	On	Off

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set in the status registers. Additionally, the SMBALERT signal is cleared if it was previously asserted. Note that the device resumes operation with the currently configured state after a CLEAR_FAULTS command has been issued. If a fault/warning is still present, the respective bit is set immediately again.

VOUT_MODE

The VOUT_MODE command is used to retrieve information about the data format for all output voltage related commands. Note that this is a read-only value.

VOUT_MODE (read only)		
Bits	**Name**	**Description**
[4:0]	PARAMETER	2's complement of the exponent
[7:5]	MODE	000: Linear data format

VOUT_COMMAND

The VOUT_COMMAND is used to set the output voltage during run-time.

VOUT_COMMAND (read/write)		
Bits	**Name**	**Description**
[15:0]	MANTISSA	Unsigned mantissa of output voltage in V. Exponent can be retrieved via VOUT_MODE command.

STATUS_BYTE

The STATUS_BYTE command returns a summary of the most critical faults in one byte.

STATUS_BYTE (read only)		
Bits	**Name**	**Description**
[0]	NONE OF THE ABOVE	A fault not listed in bits [7:1] has occurred.
[1]	CML	A communication fault as occurred.
[2]	TEMPERATURE	A temperature fault or warning has occurred.
[3]	VIN_UV	An input under-voltage fault has occurred.

[4]	IOUT_OC	An output over-current fault has occurred.
[5]	VOUT_OV	An output over-voltage fault has occurred.
[6]	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
[7]	BUSY	Not supported.

STATUS_WORD

The STATUS_WORD command returns a summary of the device status information in two data bytes.

STATUS_WORD (read only)		
Bits	**Name**	**Description**
[7:0]	STATUS_BYTE	See status byte (section 4.7.5).
[8]	UNKNOWN	Not supported
[9]	OTHER	Not supported
[10]	FANS	No supported
[11]	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
[12]	MFR	A manufacturer specific fault or warning has occurred.
[13]	INPUT	An input related warning or fault has occurred.
[14]	IOUT/POUT	An output current or output power warning or fault has occurred.
[15]	VOUT	An output voltage related warning or fault has occurred.

STATUS_VOUT

STATUS_VOUT (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]		Not supported.
[2]		Not supported.
[3]		Not supported.
[4]	VOUT_UV_FLT	An output voltage under-voltage fault has occurred.
[5]	VOUT_UV_WARN	An output voltage under-voltage warning has occurred.
[6]	VOUT_OV_WARN	An output voltage over-voltage warning has occurred.
[7]	VOUT_OV_FLT	An output voltage over-voltage fault has occurred.

STATUS_IOUT

STATUS_IOUT (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]		Not supported.
[2]		Not supported.
[3]		Not supported.
[4]		Not supported.
[5]	IOUT_OC_WARN	An over-current warning has occurred.
[6]	ICOUT_OC_LV_FLT	An over-current low-voltage shutdown fault has occurred.
[7]	IOUT_OC_FLT	An over-current fault has occurred.

STATUS_INPUT

STATUS_INPUT (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]		Not supported.
[2]		Not supported.
[3]		Not supported.
[4]	VIN_UV_FLT	An input voltage under-voltage fault has occurred.
[5]	VIN_UV_WARN	An input voltage under-voltage warning has occurred.
[6]	VIN_OV_WARN	An input voltage over-voltage warning has occurred.
[7]	VIN_OV_FLT	An input voltage over-voltage fault has occurred.

STATUS_TEMPERATURE

STATUS_TEMPERATURE (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]		Not supported.
[2]		Not supported.
[3]		Not supported.
[4]		Not supported.
[5]		Not supported.
[6]	TEMP_OV_WARN	An (external) over-temperature warning has occurred.
[7]	TEMP_OV_FLT	An (external) over-temperature fault has occurred.

STATUS_CML

STATUS_CML (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]	SMBUS_FLT	SMBus™ timeout or a format error has occurred.
[2]		Not supported.
[3]		Not supported.
[4]		Not supported.
[5]	PEC_FLT	A packet error check fault has occurred.
[6]		Not supported.
[7]	CMD_FLT	An invalid or an unsupported command has been received.

STATUS_MFR_SPECIFIC

STATUS_MFR_SPECIFIC (read only)		
Bits	**Name**	**Description**
[0]		Not supported.
[1]		Not supported.
[2]		Not supported.
[3]		Not supported.

[4]		Not supported.
[5]		Not supported.
[6]	ITEMP_OV_WARN	An (internal) over-temperature warning has occurred.
[7]	ITEMP_OV_FLT	An (internal) over-temperature fault has occurred.

READ_VIN

READ_VIN (read only)		
Bits	**Name**	**Description**
[15:0]	VIN	Input voltage in V (linear data format).

READ_VOUT

READ_VOUT (read only)		
Bits	**Name**	**Description**
[15:0]	VOUT	Output voltage in V (linear data format). Note that this command is mantissa only.

READ_IOUT

READ_IOUT (read only)		
Bits	**Name**	**Description**
[15:0]	IOUT	Output current in A (linear data format).

READ_TEMPERATURE1

READ_TEMPERATURE1 (read only)		
Bits	**Name**	**Description**
[15:0]	TEMP1	External temperature in °C (linear data format).

READ_TEMPERATURE2

READ_TEMPERATURE2 (read only)		
Bits	**Name**	**Description**
[15:0]	TEMP2	Internal temperature in °C (linear data format).

External Component Selection

Output Voltage Feedback Components

The ED8101 supports direct output voltage feedback without external components up to an output voltage of 1.4 V. However, adding a high-frequency low-pass filter in the sense path is highly recommended to remove high- frequency disturbances from the sense signals. Placing these components as close as possible to the ED8101 is recommended. For larger output voltages, a feedback divider is required. Using resistors with small tolerances is recommended to guarantee good output voltage accuracy. Table 9 lists the required component values as a function of the maximum supportable output voltage. It is mandatory that the selected resistors values are configured in the Altera ED81xx Power Designer so that they can be taken into account for the configuration of the device.

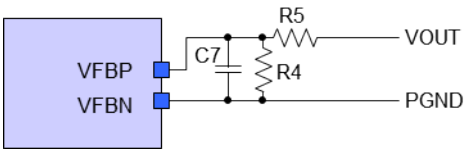

Figure 7: Output Voltage Sense Circuitry

Table 9: Output Voltage Feedback Component Overview

Nominal Output Voltage	Maximum Output Voltage	R4	R5	C7
1.30 V	1.40 V	open	1.0 kΩ	22 pF
1.80 V	2.1 V	1.5 kΩ	750Ω	47 pF
2.50 V	2.80 V	1.0 kΩ	1.0 kΩ	47 pF
3.30 V	4.25 V	1.0 kΩ	2.2 kΩ	33 pF
5.00 V	5.00 V	1.0 kΩ	3.3 kΩ	33 pF

Input Voltage Sensing

The ED8101 supports input voltage sensing for protection and monitoring. Therefore a voltage divider between the input voltage and the VIN pin is required. The recommended resistors values for different input voltage ranges can be found in Table 10. For different nominal input voltages, the respective component values with the maximum supported input voltage are listed. To ensure proper operation and high accuracy, a capacitor must not be connected to the VIN pin. Digital filtering is provided inside the ICs.

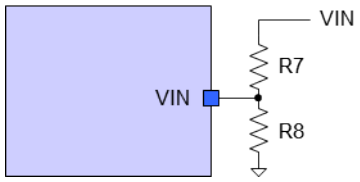

Figure 8: Input Voltage Sense Circuitry

Table 10: Input Voltage Sense Component Overview

Nominal Input Voltage	Maximum Input Voltage	R9	R8
12 V	14.5 V	20 kΩ	2.2 kΩ
8.0 V	9.0 V	12 kΩ	2.2 kΩ
5.0 V	6.5 V	8.2 kΩ	2.2 kΩ

Application Information

The ED8101 controllers have been designed operate with the Altera ET4040 Power Train, which is a complete point-of-load solution for 40A output currents. This section includes information about the typical application circuits and recommended component values.

Typical Application Circuit

The schematic for the typical application circuits for the ED8101 is shown in Figure 9. A list of recommended component values for the passive components can be found in Table 11.

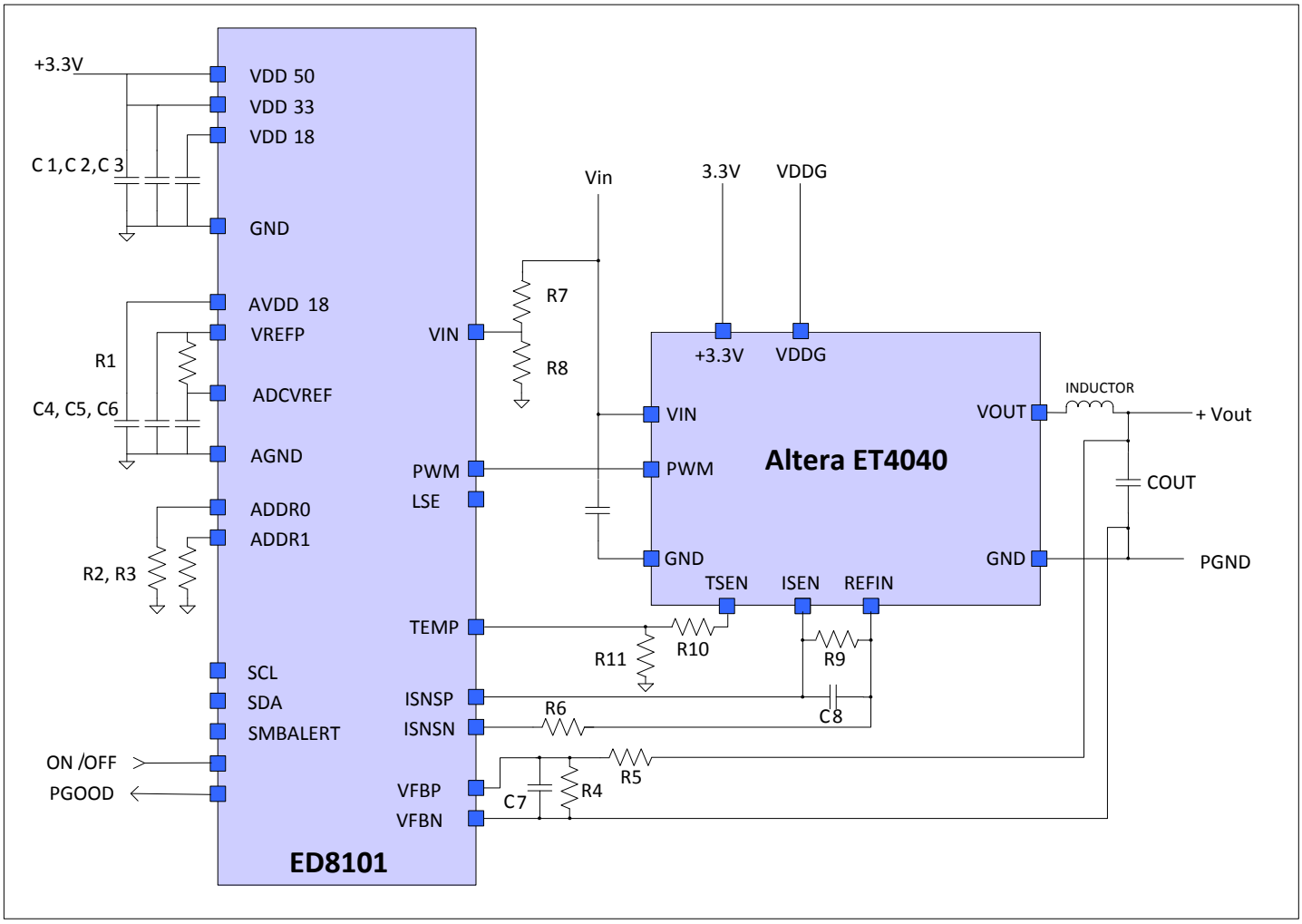

Figure 9: Application Circuit with a 3.3V Supply Voltage

Table 11: Passive Component Values for the Application Circuits

Reference Designator	Component value	Description
C1	1.0µF	Ceramic capacitor.
C2	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C3	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C4	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C5	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C6	100nF	

Reference Designator	Component value	Description
C7	22pF	Output voltage sense filtering capacitor. Recommended 22pF; maximum 1nF.
C8	0.1 µF	Current-sense filter capacitor.
CIN		Input filters capacitors. Can be a combination of ceramic and electrolytic capacitors.
COUT		Output filter capacitors
R1	51Ω	
R2, R3		PMBus™ address selection resistors.
R4	1.0kΩ	Output voltage feedback divider bottom resistor. Connect between the VFBP and VFBN pins.
R5	1.69kΩ	Output voltage feedback divider top resistor. Connect between the output terminal and the VFBP pin.
R6	1.5kΩ	Current sense resistor, should be exactly the same value with R9
R7	9.1kΩ	Input voltage divider top resistor. Connect between the main power input and the VIN pin of the ED8101.
R8	1.0kΩ	Input voltage divider bottom resistor. Connect between the VIN and AGND pins of the ED8101.
R9	1.5kΩ	Current sense resistor.
R10	10kΩ	
R11	20kΩ	

Mechanical Specifications

Based on JEDEC MO-220, all dimensions are in millimeters.

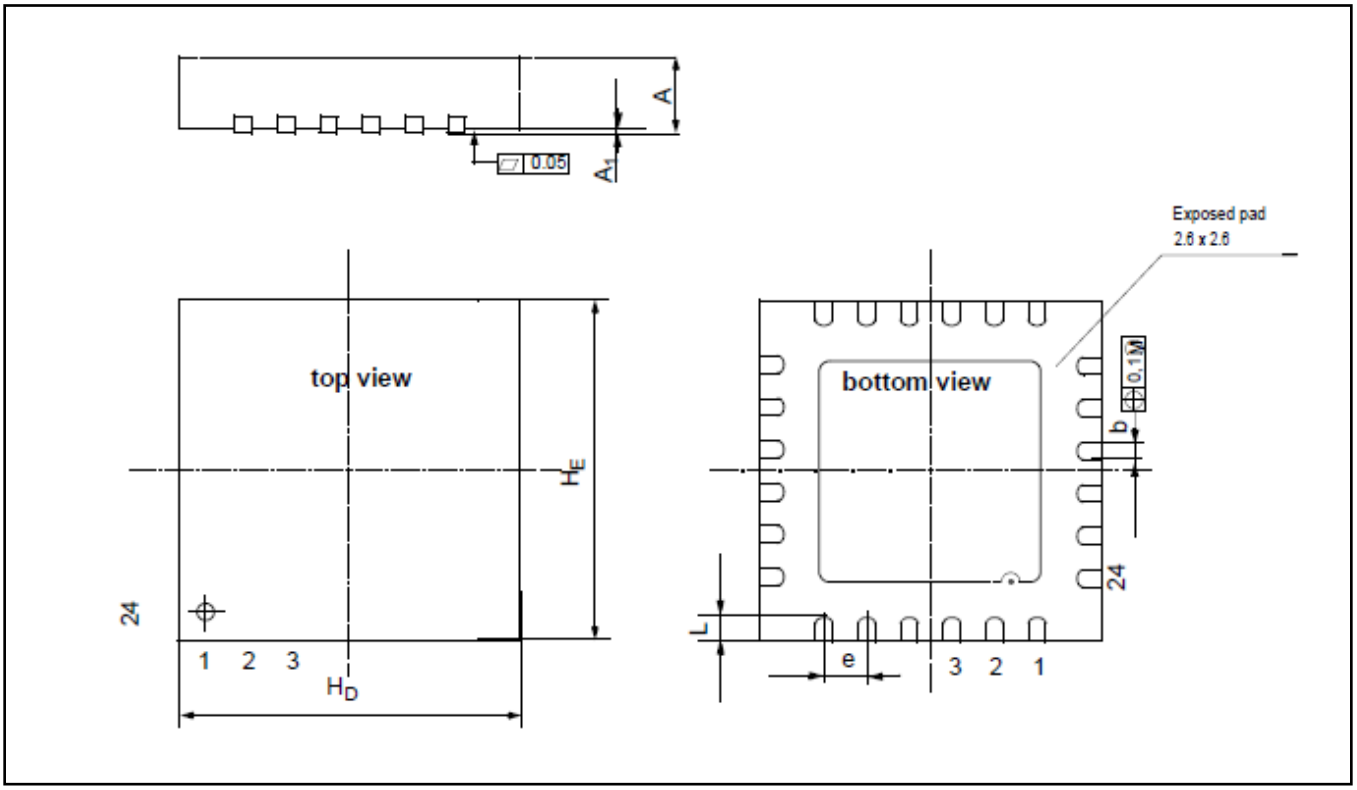

Figure 10: 24-pin QFN Package Drawing

Dimension	Min (mm)	Max (mm)
A	0.8	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0.5 nominal	
H_D	3.90	4.1
H_E	3.90	4.1
L	0.35	0.45

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